School of Electrical Engineering and Computing
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Modelling, Simulation and Real time Implementation of A Three Phase AC to AC Matrix Converter

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Dedicated to the

Loving Memory of my Parents

Late Prof. P.K. Ramanatha Iyer

and

Late Smt. P.N. Kavery Ammal

Declaration

To the best of my knowledge and belief this thesis contains no material previously published by any other person except where due acknowledgment has been made.

This thesis contains no material which has been accepted for the award of any other degree or diploma in any university.

Signature: P. R. Narayana Swamy

Date: October 2011

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ABSTRACT

Matrix converters (MCs) are essentially forced commutated cycloconverters with inherent four quadrant operation consisting of a matrix of bidirectional switches such that there is a switch for each possible connection between the input and output lines. Matrix converter directly converts the AC input voltage at any given frequency to AC output voltage with arbitrary amplitude at any unrestricted frequency without the need for a dc link capacitor storage element at the input side.

The introduction of bidirectional switches using power transistors and IGBTs made easy realization of the matrix converter. The real development of the matrix converter starts with the work of Venturini and Alesina who proposed a mathematical analysis and introduced the Low-Frequency Modulation Matrix concept to describe the low frequency behavior of the matrix converter [1-3]. In this, the output voltages are obtained by multiplication of the modulation matrix or transfer matrix with the input voltages. One of the essential requirements for switching three phase AC to three phase AC MC is that two or more bidirectional switches connected to any one output phase should NOT be closed simultaneously, as this will cause dangerously high short circuit current. Similarly any one bidirectional switch connected to each output phase should remain closed to provide a current path with inductive load.

This thesis mainly provides an account of the three phase AC to three phase AC MC modelling concept with SIMULINK software using fundamental Venturini and Optimum Venturini modulation algorithm [1-8], advanced modulation algorithm such as that proposed by Sunter-Clare [11-12] and by Ned Mohan [13-14, 16-17], application of these algorithms for the Vector control of three phase Induction Motor (IM) drive [15], real time hardware in the loop simulation [51,54-55] for a three phase AC to single phase AC MC, three phase AC to three phase AC Multilevel MC (MMC) with three [18-19] and six flying capacitors per output phase using PSCAD software (as SIMULINK started shooting trouble), Indirect (ISVM) [25-30] and Direct (DASVM, DSSVM, CZASVM) [31-38] Space Vector Modulation, newly discovered dual programmable AC to DC rectifier concept using three phase AC to three phase AC MC [43-45], Delta-Sigma Modulated MC [46-49] and single phase AC to three phase AC MC [50]. In addition a novel concept of a single phase / three phase AC to single phase / three phase AC converter using a DC link, complementary N and P MOSFETs and IGBTs is presented. A chapter on model verification is also presented where selected SIMULINK models from various chapters have been verified by using either PSCAD or PSIM software. An appendix on PIC microcontroller PIC16F84A application to saw-tooth carrier waveform generation and switching three phase AC to three phase AC converters using a DC link is added. Another appendix on speed control and brake by plugging of three phase induction motor fed by matrix converter is presented. List of publications from this thesis is presented on third appendix.

LIST OF ABBREVIATIONS

Symbols:

A,B,C	Input phase
a,b,c	Output phase
C	Capacitor
Cf	Filter capacitor
D	damping constant
f	Frequency
fc	Carrier frequency
fo	Output frequency
f_{SW}	Switching Frequency
i	Instantaneous Current
io	Instantaneous Output Current
J	Moment of Inertia
k	Modulation index
kp, ki	Proprotional and Integral constant
L	Inductor
Lf	Filter inductor
M	Modulation Function
P	Number of Poles
q	Modulation Index
R	Resistance
RL	Load resistance
S	Switch position or Switch Function
SI, S_I	Input Current Sector
SV, S_V	Output Voltage Sector
T	Period
Tc	Carrier period
Tem	Electromagnetic torque
T_S	Sample time
Tsw	Switching period
v	Instantaneous voltage
V_{DC}	DC Link Voltage
vi	Instantaneous input voltage
Vim	Maximum line to neutral input Voltage
vo	Instantaneous output voltage
Vsaw	Saw-tooth carrier Voltage
Vtri	Triangle Carrier Voltage

δ, d	Duty-cycle or Duty-ratio
λ	Flux linkage
σ	Leakage factor
φi	Input power factor angle
φo	Output power factor angle
ωi	Input angular frequency
ωo	Output angular frequency

Suffix:

a,b,c	Output phase quantities
A,B,C	Input phase quantities
d,q	d-axis and q-axis quantities
i	Input
l	Leakage
m	Mutual
o	Output
r	Rotor quantities
s	Stator quantities
c	Carrier
sw	Switching

Superfix:

I, II, III, IV	Four Switching configurations
0	Zero switching configuration

Acronym:

AC	Alternating current
ASVM	Asymmetrical Space Vector Modulation
CMC	Conventional Matrix Converter
CZASVM	Centre Zero Asymmetrical Space Vector Modulation
DASVM	Direct Asymmetrical Space Vector Modulation
DC	Direct current
DSVM	Direct Space Vector Modulation
FC	Flying Capacitor
HEV	Hybrid Electric Vehicle
HIL	Hardware in the Loop
IGBT	Insulated Gate Bipolar Transistor

IM	Induction Motor
ISVM	Indirect Space Vector Modulation
KVL	Kirchhoff's Voltage Law
MC	Matrix Converter
MMC	Multilevel Matrix Converter
PH1	Single phase
PH3	Three phase
PWM	Pulse Width Modulation
ssf, SSF	Sector Switch Function
SSVM	Symmetrical Space Vector Modulation
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
ZCC	Zero Crossing Comparator

CONTENTS

Chapter I
Introduction

1.1 BACKGROUND: The most desirable features of the power electronic frequency converters are: a) Simple and Compact Power Circuit. b) Variable output voltage magnitude and frequency. c) Sinusoidal input and output currents. d) Unity Power Factor operation for any type of load. e) Regeneration capability. Matrix converter (MC) fulfills all these requirements and is the most sought after converter for industrial drives application. Matrix converters are essentially forced commutated cycloconverters with inherent four quadrant operation consisting of a matrix of bidirectional switches such that there is a switch for each possible connection between the input and output lines. Matrix converter directly converts the AC input voltage at any given frequency to AC output voltage with arbitrary amplitude at any unrestricted frequency without the need for a DC link capacitor storage element at the input side.

The early work, prior to the development of Matrix Converter using bidirectional semiconductor switches, was the cycloconverters using thyristors with forced commutation circuits which act as bidirectional switches. But the power circuit of these thyristor cycloconverters were too bulky and the performance was poor. The introduction of bidirectional switch using power transistors and IGBTs made easy realization of the matrix converter. The real development of the matrix converter starts with the work of Venturini and Alesina who proposed a mathematical analysis and introduced the Low-Frequency Modulation Matrix concept to describe the low frequency behavior of the matrix converter [1-3]. In this, the output voltages are obtained by multiplication of the modulation matrix or transfer matrix with the input voltages. One limitation of the matrix converter is that the maximum output voltage available is limited to 86.6 % of the input voltage in the linear modulation range.

As mentioned, it is the development of the bidirectional switches using semiconductor components that makes matrix converter really attractive. Although number of topologies for bidirectional switches are available, the common emitter IGBT topology is used here in this thesis work. Some of the IGBT topologies used as bidirectional switches are shown in Fig. 1.1. These topologies are respectively a) Diode-Embedded b) Common-Emitter c) Common-Collector d) Antiparallel in series with Diodes and e) Reverse Blocking or R-B IGBT.

The correct method of applying gate pulse to a common-emitter IGBT bidirectional switch is shown in Fig. 1.2(A). The sinusoidal voltage input, the pulse width modulated output voltage across the load and the gate switching pulses are shown in Fig. 1.2(B), (C) and (D) respectively. A three phase AC to three phase AC MC consists of nine bidirectional switches (eighteen IGBTs each with a diode in parallel as in Fig. 1.1(b)). The topology of the three phase AC to three phase AC MC is shown in Fig. 1.3. The three phase input voltage terminals are marked A, B and C and the corresponding three phase AC output voltage terminals are marked a, b and c respectively. The bidirectional switches are

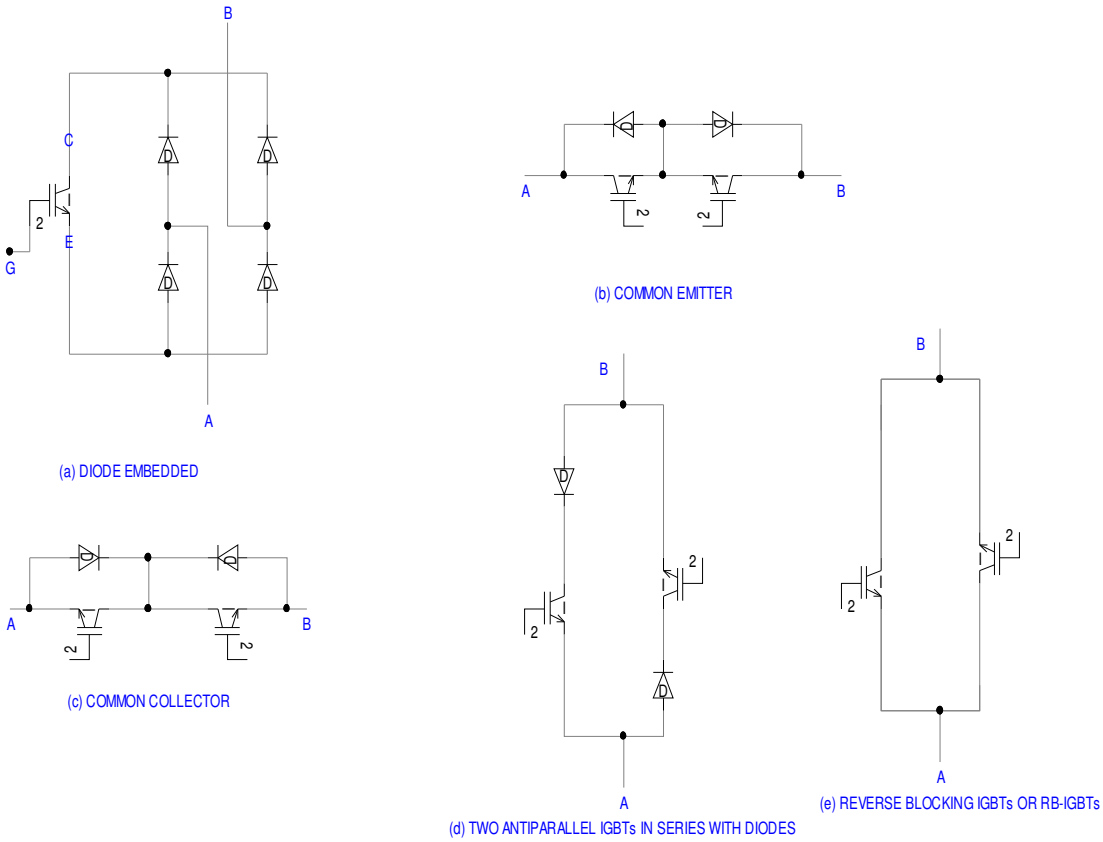


FIG. 1.1: BIDIRECTIONAL SWITCH TOPOLOGY

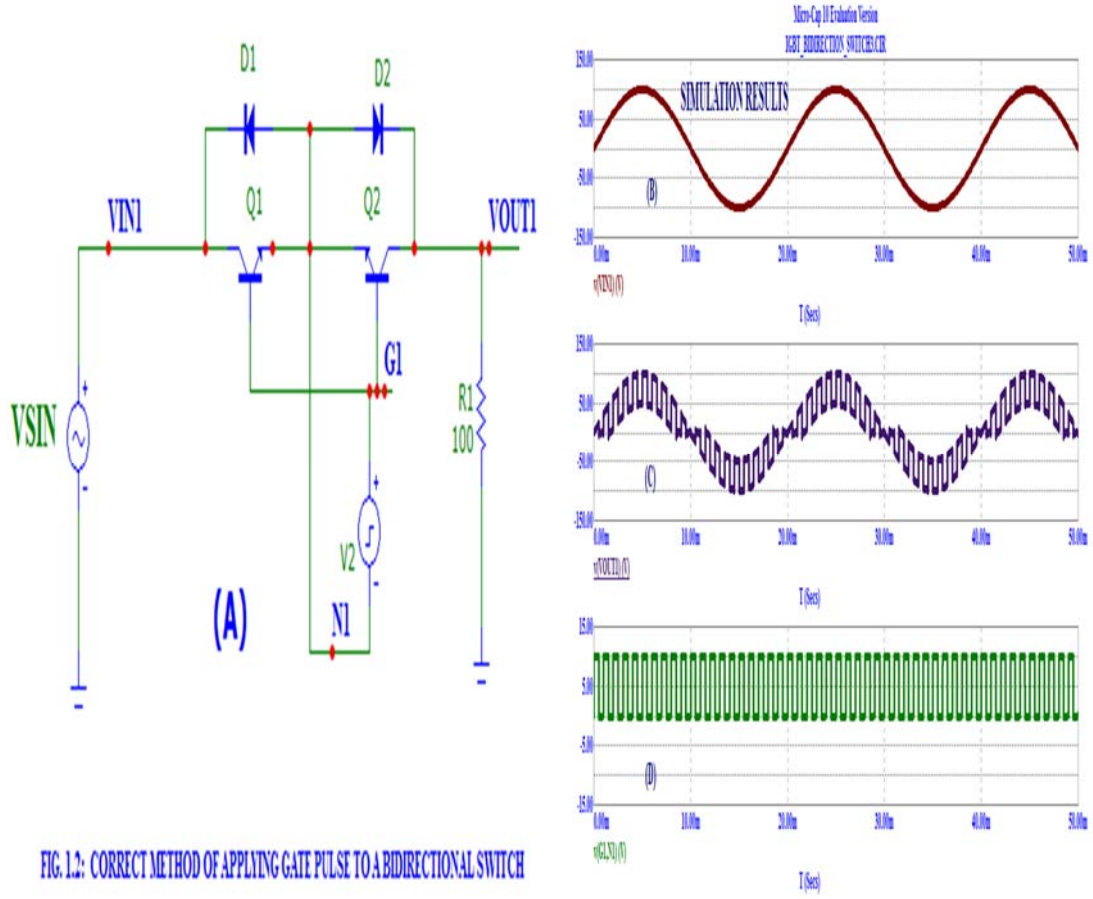


FIG. 1.2: CORRECT METHOD OF APPLYING GATE PULSE TO A BIDIRECTIONAL SWITCH

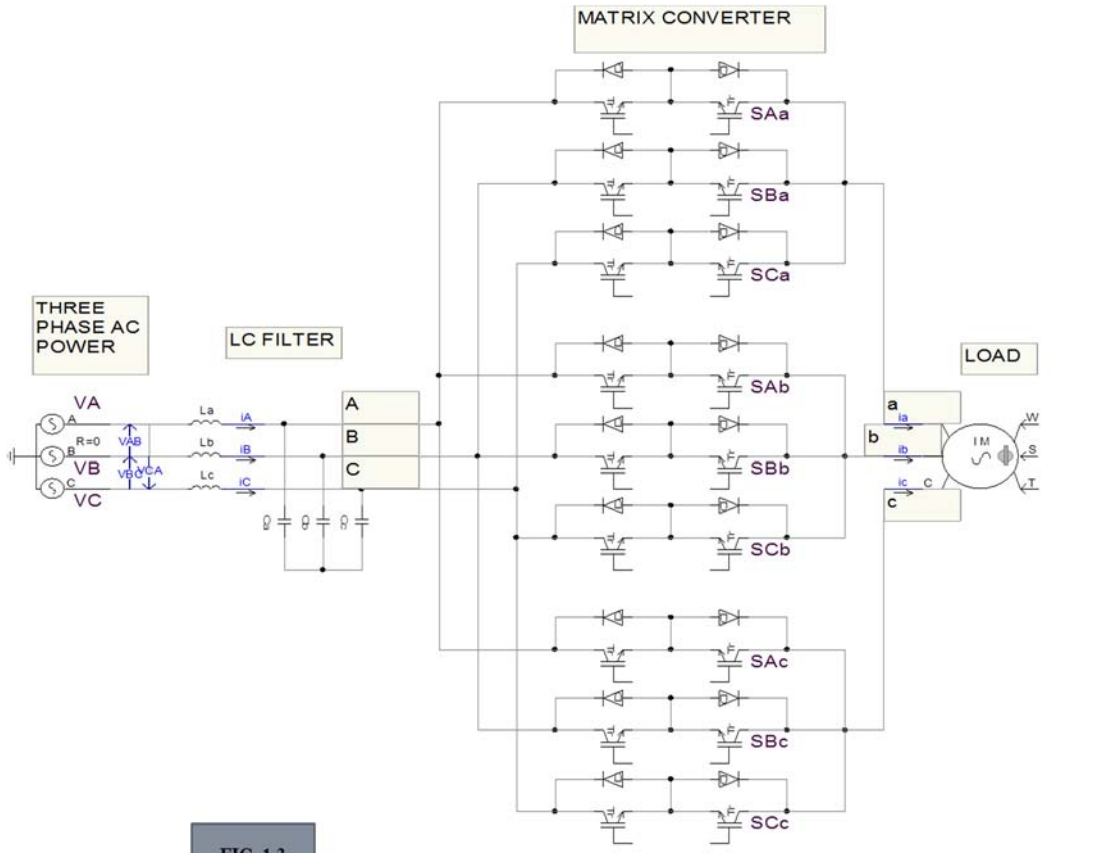


FIG. 1.3 THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER

represented as S_{Kj} where K ϵ A, B, C and j ϵ a, b, c respectively. Thus a three phase AC to three phase AC MC can be represented as 3 X 3 MC. A 3 X 3 MC has twenty seven switching combinations as shown in Table 1.1 below.

TABLE 1.1: PH3 AC to PH3 AC MC Switching Combinations

Group	a	b	c	vab	vbc	vca	iA	iB	iC	SAa	SBa	SCa	SAb	SBb	SCb	SAc	SBc	SCc
I	A	B	C	vAB	vBC	vCA	Ia	ib	ic	1	0	0	0	1	0	0	0	1
I	A	C	B	-vCA	-vBC	-vAB	Ia	ic	ib	1	0	0	0	0	1	0	1	0
I	B	A	C	-vAB	-vCA	-vBC	Ib	ia	ic	0	1	0	1	0	0	0	0	1
I	B	C	A	vBC	vCA	vAB	Ib	ic	ia	0	1	0	0	0	1	1	0	0
I	C	A	B	vCA	vAB	vBC	Ic	ia	ib	0	0	1	1	0	0	0	1	0
I	C	B	A	-vBC	-vAB	-vCA	Ic	ib	ia	0	0	1	0	1	0	1	0	0
II-a	A	C	C	-vCA	0	vCA	Ia	0	-ia	1	0	0	0	0	1	0	0	1
II-a	B	C	C	vBC	0	-vBC	0	ia	-ia	0	1	0	0	0	1	0	0	1
II-a	B	A	A	-vAB	0	vAB	-ia	ia	0	0	1	0	1	0	0	1	0	0
II-a	C	A	A	vCA	0	-vCA	-ia	0	ia	0	0	1	1	0	0	1	0	0
II-a	C	B	B	-vBC	0	vBC	0	-ia	ia	0	0	1	0	1	0	0	1	0
II-a	A	B	B	vAB	0	-vAB	Ia	-ia	0	1	0	0	0	1	0	0	1	0
II-b	C	A	C	vCA	-vCA	0	Ib	0	-ib	0	0	1	1	0	0	0	0	1
II-b	C	B	C	-vBC	vBC	0	0	ib	-ib	0	0	1	0	1	0	0	0	1
II-b	A	B	A	vAB	-vAB	0	-ib	ib	0	1	0	0	0	1	0	1	0	0
II-b	A	C	A	-vCA	vCA	0	-ib	0	ib	1	0	0	0	0	1	1	0	0
II-b	B	C	B	vBC	-vBC	0	0	-ib	ib	0	1	0	0	0	1	0	1	0
II-b	B	A	B	-vAB	vAB	0	Ib	-ib	0	0	1	0	1	0	0	0	1	0
II-c	C	C	A	0	vCA	-vCA	Ic	0	-ic	0	0	1	0	0	1	1	0	0
II-c	C	C	B	0	-vBC	vBC	0	ic	-ic	0	0	1	0	0	1	0	1	0
II-c	A	A	B	0	vAB	-vAB	-ic	ic	0	1	0	0	1	0	0	0	1	0
II-c	A	A	C	0	-vCA	vCA	-ic	0	ic	1	0	0	1	0	0	0	0	1
II-c	B	B	C	0	vBC	-vBC	0	-ic	ic	0	1	0	0	1	0	0	0	1
II-c	B	B	A	0	-vAB	vAB	Ic	-ic	0	0	1	0	0	1	0	1	0	0
III	A	A	A	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0
III	B	B	B	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0
III	C	C	C	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1

In Table 1.1, corresponding to Group II-c, C C A means that the input phase C is connected to output phase a and b and input phase A is connected to output phase c. Referring to Fig.1.3, output phase to phase voltage vab, vbc and vca are respectively zero (VCC), VCA and VAC or –VCA. Also input current iA, iB and iC are the load currents ic, 0 and –ic respectively. This is illustrated diagrammatically for Group II-a of Table 1.1 below:

GROUP	a	b	c	vab	vbc	vca	iA	iB	iC
II-a	A	C	C	-vCA	0	vCA	ia	0	-ia

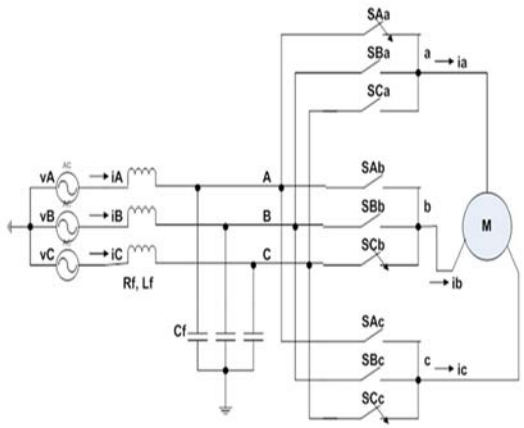


FIG. 1.4: THREE PHASE MATRIX CONVERTER DRIVING A THREE PHASE AC MOTOR LOAD

The position of the nine bidirectional switches corresponding to Group II-a in Table 1.1 is shown in Fig, 1.4. The switches SAa, SCb and SCc are closed and all others are open. Applying Kirchoff's law to Fig. 1.4, the following set of equations will result:

$$\left.\begin{aligned} v_{ab} &= v_{AC} = -v_{CA} \\ v_{bc} &= 0 \\ v_{ca} &= v_{CA} \end{aligned}\right\} \quad (1.1)$$

$$\left.\begin{aligned} i_A &= i_a \\ i_B &= 0 \\ i_C &= -i_a \end{aligned}\right\} \quad (1.2)$$

Also in Fig. 1.4, assigning closed switch as logic 1 and open switch as logic 0, switches SAa to SCc in order can be assigned the position: 1 0 0 0 0 1 0 0 1.

Referring to Fig. 1.3, in terms of the switch position the output voltage corresponding to phase a and the input current corresponding to phase A can be expressed as follows:

$$v_a = S_{Aa} * v_A + S_{Ba} * v_B + S_{Ca} * v_C \quad (1.3)$$

$$i_A = S_{Aa} * i_a + S_{Ab} * i_b + S_{Ac} * i_c \quad (1.4)$$

One of the essential requirements for switching three phase AC to three phase AC MC is that two or more bidirectional switches connected to any one output phase should NOT be closed simultaneously, as this will cause dangerously high short circuit current. Similarly any one bidirectional switch connected to each output phase should remain closed to provide a current path with inductive load. This necessitates saw-tooth carrier signal to be compared with modulation functions for each of the bidirectional switches in a comparator and the resulting output is given to logic gates in such a manner that the gate pulses to the three bidirectional switches connected to any one output phase occur in sequence or one after the other.

1.2 OBJECTIVE: The following are the objective of this thesis:

- Develop models for MC

  -To develop models for three phase AC to three phase AC Conventional MC topology connected to R-L load and Vector Controlled Induction Motor drive, using Venturini, Optimum Venturini and other Advanced Modulation algorithms.

  -To develop models for three phase AC to three phase AC Multilevel MC topology with three and six Flying capacitors per output phase, using Venturini algorithm.

  -To develop models for Direct and Indirect Space Vector Modulated three phase AC to three phase AC MC topology.

-To develop model for the newly discovered Dual Programmable AC to DC Rectifier using Three Phase AC to Three Phase AC MC topology.

-To develop models for three phase AC to three phase AC MC when switching is carried out by sample time based modulation technique also known as Delta-Sigma Modulation.

-To develop model for single phase AC to three phase AC MC topology.

-To develop models for a single phase/three phase AC to single phase/three phase AC converter topology using a DC link voltage.

- Hardware implementation

  -To implement in real time, a three phase AC to single phase AC MC using dSPACE DS1104 Hardware Controller Board.

- Explore applications

  -Applications of three phase AC to three phase AC MC for Industrial AC Drives [6-7, 14, 40-41, 56], Wind Energy Conversion [57-59], Aircraft Control Applications [60-61] and Railway Electric Traction Power Supply [62] are already reported in the literature. In this thesis additional applications for the speed control and brake by plugging of two separately excited DC motors fed by the newly discovered Dual Programmable AC to DC Rectifier suitable for Hybrid Electric Vehicle and Electric traction is presented. In addition another application of three phase AC to three phase AC MC for the speed control and brake by plugging or by reversing the phase sequence of three phase Induction Motor is presented.

1.3 RESEARCH METHODOLOGY: The following are the research methods used:

- Develop Models for MC

  - Software approach
    - SIMULINK [51]
    - PSIM [52]
    - PSCAD [53]

  - Hardware implementation
    - Real time Hardware using dSPACE [54]

1.4 THESIS OUTLINE AND NOVELTY: This thesis mainly provides an account of the three phase AC to three phase AC MC modelling using the software SIMULINK. Unless specified otherwise the term **model** in this thesis refers to **SIMULINK model**. The outline and novelty of each chapter in this thesis is discussed below:

Many literature references have been referred for developing the model presented in this thesis. The literature review in Chapter II provides the brief account of the work and the literatures referred relevant to the particular chapter.

The three phase AC to three phase AC matrix converter low frequency modulation matrix concept was first developed by Alesina and Venturini [1-3]. Chapter III presents an overview of this Venturini

and Optimum Venturini modulation algorithm and models of three phase AC to three phase AC MC based on these algorithms. An appendix is provided in this chapter to prove that Venturini algorithm works well with both three phase sine wave and cosine wave input voltages.

Advanced Modulation algorithm for three phase AC to three phase AC MC such as that proposed by Sunter-Clare [11-12] and that by Ned Mohan [13-14, 16-17] is presented in Chapter IV along with model simulation results. An appendix is provided in this chapter to prove the validity of Advanced Modulation algorithm proposed by Ned Mohan for both three phase sine wave and cosine wave input voltages.

Vector controlled three phase Induction Motor (IM) drive is reported in the literature [15]. Based on this reference, model for three phase AC to three phase AC MC driving a vector controlled IM drive presented in Chapter V using all of the above mentioned algorithms with simulation results. An appendix is provided to determine the PI controller parameters required for vector control using MATLAB source code.

Real time Hardware-in-the-Loop (HIL) simulation using SIMULINK model in conjunction with dSPACE modules and interfacing through a dSPACE ds1104 hardware controller board [51, 53-55] to the real three phase AC to single phase AC MC assembled using hardware IGBT components in the laboratory is presented in Chapter VI. Here a three phase square wave input voltage from a three phase inverter is used as the input and a single phase square wave output voltage is obtained from the above MC. The model uses Venturini algorithm for generating modulation functions to generate gate pulses for the bidirectional switches. A Hewlett-Packard saw-tooth carrier generator interfaced to the ADC input of the ds1104 hardware controller board is used to compare the modulation functions and generate gate pulses using logic circuit blocks in SIMULINK. This gate pulses from SIMULINK logic circuit block is interfaced to DAC outputs of ds1104 hardware controller board which is used for applying gate pulses to the MC. Real time simulation results are compared with model simulation results.

Based on three phase AC to three phase AC Multilevel Matrix Converter (MMC) with two and three Flying capacitors (FCs) [18-19], models have been developed using PSCAD [53] for three phase AC to three phase AC MMC with three and six FC per output phase. These are presented in Chapter VII. In this case SIMULINK models couldn't be developed as the model started shooting trouble. The model representation of three phase MMC with three FC using logic sates of the bidirectional switches is a novel feature. The model for three phase MMC with six FC is newly proposed. Simulation results using PSCAD are also presented. An appendix is provided to derive the operation of the three phase MMC with six FC for selected bidirectional switch combinations.

Models for Direct Asymmetrical (ASVM) and Direct Symmetrical (SSVM) Space Vector Modulation [31-38] of three phase AC to three phase AC MC is presented in Chapter VIII. A new Direct

Asymmetrical Centre Zero Space Vector Modulation (CZSVM) is proposed in this chapter. Simulation results are presented. Two appendices, one for calculating output voltage and input current from the state of the bidirectional switches and another for calculating the duty-cycle along the x-y axis are presented.

Indirect Space Vector Modulation (ISVM) [25-30] of three phase AC to three phase AC MC considers that the above MC is equivalent to a three phase AC to DC rectifier and a DC to three phase AC Inverter. Based on this technique model has been developed for three phase AC to three phase AC ISVM MC and are presented with simulation results in Chapter IX. Appendices are provided to derive the various equations and tables presented in this chapter.

Dual fixed AC to DC rectifier using three phase AC to three phase AC MC topology [43-45] is reported in the literature based on which Dual Programmable AC to DC rectifier using the above MC topology is presented in Chapter X. This Dual Programmable AC to DC rectifier is an outcome as a result of "Newtonian thought" by the author of this thesis to the first sentence in the first paragraph under the subheading "Using a Matrix Converter as an AC/DC Rectifier" in page 356 of reference 43 which reads thus: "To operate a matrix converter as an ac-dc rectifier, the output frequency is set to zero, and the output voltage phase angle is set to **30^{o}**". The "Newtonian thought" made by the author of this thesis is "Why 30 degree phase angle for output phase voltage; why NOT some other value"? This is considered by the author of this thesis as a fantastic breakthrough discovery and a greatest achievement in this research thesis having enormous industrial applications. Models have been developed for the dual programmable AC to DC rectifier using the above MC topology and simulation results are presented. Derivations for the dual DC output voltage magnitude have been presented using phasor diagrams which is an original contribution in this thesis. The application of this Dual Programmable AC to DC rectifier driving separately excited DC motor and Permanent Magnet DC motor suitable for Hybrid Electric Vehicle (HEVs) and Electric Traction is highlighted. At this stage, the author of this thesis is only able to dream future generation of at least one model of HEV and Bullet electric train/normal electric train running on the roadways and railways based on the method developed in Chapter X of this research thesis. An appendix is provided to derive suitability of the dual programmable AC to DC rectifier using three phase cosine wave input voltages.

Models based on sample time or discrete time based modulation technique also known as Delta-Sigma modulation technique [46-49] is reported in Chapter XI. This models use Z transform approach. Models have been presented for three phase AC to three phase AC MC with Delta-Sigma modulation using both Venturini algorithm and Advanced Modulation algorithm proposed by Ned Mohan for both R-L load and three phase IM load. The Delta-Sigma modulated MC using Advanced modulation algorithm is newly proposed in this thesis. Simulation results are presented.

Single phase AC to three phase AC MC topology, without the need for rectification and inversion, is reported in the literature [50] based on which model has been developed for single phase AC to three

phase AC MC. This is presented in Chapter XII. Simulation results are presented for both R-L load and three phase IM load.

A novel AC to AC converter using a DC link is a new idea or a new method developed by the author of this thesis. Here models and simulation results for both single phase/three phase AC voltages at supply frequency to single phase/three phase AC output voltages with a variable frequency and magnitude is presented using the software PSIM [51]. The model essentially consists of N-P MOSFET pairs driven by op.amplifier zero crossing comparator to produce single phase / three phase square wave AC output voltage at supply frequency which are given as input to IGBT bidirectional switches driven by counter and Multiplexer to produce variable frequency output voltage. Pulse Width Modulation is achieved by conventional technique. The model and simulation results are presented in Chapter XIII. An appendix is provided with simulation results to explain the operation of supply frequency N-P MOSFET inverter and that of the variable output frequency inverter using IGBT bidirectional switches.

Finally the selected SIMULINK models presented in various chapters of this thesis have been verified for performance, by simulation using either PSIM or PSCAD software. This verification report is presented in Chapter XIV of this thesis. This model verification may be considered as a written thesis defence.

Chapter XV presents the summary of contributions and conclusions derived from this research thesis work.

Appendix I presents the PIC microcontroller PIC16F84A approach for generating a 2 kHz saw-tooth carrier generator to replace the one discussed using IC NE555 in Chapter X and another gate drive for IGBT bidirectional switches in the three phase AC to three phase AC converter using a DC link presented in Chapter XIII, to replace the one presented using modulo six counter and multiplexer.

Appendix II presents the speed control and brake by plugging of three phase IM fed by matrix converter. This novel method of speed control and braking using the model implemented in real time using dSAPCE makes it suitable for Hybrid Electric Vehicles and Electric traction.

Appendix III presents the list of publications from this thesis work.

Chapter II
Literature Review

2.1 INTRODUCTION: This chapter provides the review of literature relating to modelling, simulation and experimental verification of Three Phase AC to AC Matrix Converter . The literature referred for this research work is given under References. Detailed chapter by chapter reference made is given below:

2.2 VENTURINI AND OPTIMUM VENTURINI MODULATION ALGORITHM: Chapter III deals with the modelling of MC using Venturini and Optimum Venturini Modulation algorithm [1-5]. The low frequency modulation matrix m(t) is defined and the matrix converter behaviour is modelled as $vo(t) = m(t)*v_i(t)$ and $i_i(t) = m^T(t)*i_o(t)$ where $v_o(t)$, $v_i(t)$, $i_i(t)$ and $i_o(t)$ are the output voltage, input voltage, input current and output current respectively. The solution of m(t) gives the nine modulation functions for the MC, given the angular frequency ωi and ωo of the three phase cosine wave input, output voltages and modulation index q [1-5]. The general solution is termed Venturini First method and the solution assuming Unity Input Phase Displacement Factor is termed Venturini second method in this thesis. In optimum Venturini method, the nine modulation functions are presented assuming that the three phase output voltage $v_o(t)$ contains the normal cosine wave component of voltages at frequency ωo added with third harmonic component of input voltage and from which subtracting third harmonic component of output voltage corresponding to their respective frequencies in appropriate proportions [4-5]. In Chapter III, the models are developed for MC using the Venturini First, Second and Optimum Venturini method, in SIMULINK and the simulation results are presented for R-L load [9-10, 51].

2.3 ADVANCED MODULATION ALGORITHMS: In Chapter IV, modelling of MC in SIMULINK using Advanced modulation algorithms such as proposed by Sunter-Clare [11-12] and that by Ned Mohan is presented [13-14, 16-17].

The Venturini modulation algorithm is suitable for synchronous operation of the input with the output [11]. This approach is unsuitable for closed loop applications where it is required to calculate the duty cycle every sampling period to achieve voltage control in which output frequency is continuously varying with time [11]. To overcome this problem the approach taken is to measure the input voltage at every sampling period and to determine voltage vector magnitude and ratio and position directly [11]. A simplified version of Venturini algorithm is defined in terms of the three phase input and output voltage at each sampling instant [11-12]. This allows the demand voltage ratio, output voltage magnitude and angle to be updated at every sampling period which is a requirement for closed loop control [11-12]. The simplified Venturini algorithm is used to develop the model of the three phase Matrix converter in SIMULINK [11-12, 51].

A novel carrier based modulation technique is used for modelling the three phase AC to three phase AC matrix converter [13-14, 16-17]. This method avoids the use of sector information and look-up table. In this method the output line to neutral voltage va of the matrix converter is expressed either in the form $v_a = (3/2).k.Vim.\cos(\varphi i).\cos(\omega o.t)$ or in the form $v_a = (3/2).k.Vim.\cos(\varphi i).\sin(\omega o.t)$, where k is the modulation index, Vim is the maximum line to neutral input voltage, φi is the input power factor angle and ωo is the output angular frequency. Further mathematical manipulations are done so that the duty ratios of the matrix converter switches lie in the range 0 to 1. The control duty ratio signals thus obtained are compared with a triangular carrier signal to obtain the gate pulse for the nine bidirectional switches of the matrix converter. Simulation results using SIMULINK are presented assuming unity input power factor [51].

2.4 VECTOR CONTROLLED THREE PHASE INDUCTION MOTOR DRIVE FED BY MATRIX CONVERTER: In chapter V, vector controlled three phase Induction Motor drive fed by Matrix converter is studied in detail by model simulation [13-15]. SIMULINK software is used for Model development [51]. The proposed scheme uses the carrier-based PWM scheme of MC for generation of PWM gate pulses based on various algorithms such as by Venturini, Sunter-Clare and Ned Mohan [1-8, 11-12, 13-15]. Carrier based Vector control scheme uses two PI controllers, one for the speed control loop and the other for the current control loop. The dq axis model of the three phase induction motor in synchronously rotating reference frame is used. Simulation results are presented.

2.5 HARDWARE IN THE LOOP SIMULATION OF A THREE PHASE AC TO SINGLE PHASE AC MATRIX CONVERTER: In chapter VI, Hardware-in-the-Loop simulation of a three phase AC to single phase AC matrix converter is presented. The dSPACE DS1104 hardware controller board is used for this experiment [54]. The input used is a three phase 50 Hz square wave AC voltage, having a line to neutral RMS voltage of 123 Volts. The single phase AC output voltage has a frequency of 50 Hz. The model is developed in SIMULINK [51]. Venturini algorithm assuming unity input phase displacement factor is used to generate gate pulse for the three bidirectional switches. Both simulation and hardware experimental results are presented.

2.6 MULTILEVEL MATRIX CONVERTER: The modelling and simulation of Three phase AC to three phase AC Multilevel Matrix Converter with three flying capacitors per output phase is presented in Chapter VII [18-19]. Three phase multilevel matrix converters are proposed for reducing the harmonic components of the line to neutral, line to line output voltages and the input current [18-19]. The model equations showing the relation between three phase input and output voltages as well as for input and output currents are presented. Venturini modulation algorithm for bidirectional switches is implemented using two saw-tooth carrier signals out of phase by 180 degrees or Tsw/2 seconds where Tsw is the period of the saw-tooth carrier signal. The model is extended for three phase AC to three phase AC multilevel matrix converter with six flying capacitors per output phase. Simulation results using PSCAD are presented.

2.7 DIRECT SPACE VECTOR MODULATION OF MATRIX CONVERTER: The direct Asymmetrical Space Vector Modulation and Symmetrical Space Vector Modulation (SSVM) for three phase AC to three phase AC Matrix Converter are presented in Chapter VIII [31-35]. The model of the three phase MC using ASVM and SSVM technique is developed in SIMULINK [36-38, 51]. In addition a new Centre Zero ASVM technique is also proposed in this chapter. The space-vector modulation technique, owing to the two degrees of freedom, represents the general solution of the modulation problem of matrix converters. This technique can be considered the best solution for the possibility to achieve the highest voltage transfer ratio and to optimize the switching pattern through a suitable use of the zero voltage vector configurations. This solution has been obtained using the duty-cycle space-vector approach, which consists of a representation of the switch state by space vectors [31-35]. In space vector approach, the input currents and output voltages are represented as space vectors in the complex plane. From 27 switching states, only 21 switching states are used for space vector approach. The eighteen active voltage states are assigned numbers from ±1 to ±9 and the three zero voltage vectors are assigned 01, 02 and 03 [31-35]. These switch states for output voltage and input currents are represented as hexagons in complex plane. With the sector number of output voltage and that for input current, the switch states common to both are noted and tabulated in four switching configurations. The duty cycles for the four switching configurations are derived for a given modulation index and that for zero voltage vector is calculated using the relation that the sum of the duty cycles for the four switching configurations and that for zero voltage vector state is unity [31-35]. Two sets of rules are proposed for these techniques in order to simplify the model implementation. Rules for assigning the zero voltage vector for ASVM, SSVM and CZASVM are proposed. SIMULINK model is developed and the simulation results are presented [36-37].

2.8 INDIRECT SPACE VECTOR MODULATION OF MATRIX CONVERTER: The indirect Space Vector Modulation (ISVM) for three phase AC to three phase AC Matrix Converter is presented in Chapter IX. In the proposed voltage Space Vector PWM control of MCs, the Indirect Transfer Function approach is used where the input AC voltage is first rectified to create a fictitious DC voltage which is then inverted at the required output frequency [25-30]. For low harmonic distortion, the inverter operation is achieved by Space Vector Modulation (SVM) simultaneously with input current SVM for rectification [25-30]. The simultaneous output voltage-input current SVM algorithm is reviewed here and the model of the 3 X 3 MC is derived based on this algorithm using SIMULINK. The simulation results are presented.

2.9 DUAL PROGRAMMABLE AC TO DC RECTIFIER USING THREE PHASE MATRIX CONVERTER: Three Phase AC to Three Phase AC Matrix Converter based dual AC to DC rectifier is reported in the literature [43-45]. But these reports only indicate that dual DC output voltages with fixed value is possible by setting the desired AC output voltage phase angle leading by 30 degrees and the frequency of output voltage zero in the model [43-44]. Detailed modelling studies using SIMULINK reveals that with the frequency of desired AC output voltage set to zero, as the AC output voltage phase angle is varied from 0 to $+\pi$ and 0 to $-\pi$, dual DC output voltages in multitude of

combinations are possible such as a) Both voltages positive and unequal, b) Both voltages positive and equal, c) Any one voltage zero and the other positive, d) Any one Voltage positive and the other negative with unequal modulus value, e) Any one voltage positive and the other negative with equal modulus value, f) Any one Voltage zero and the other negative, g) Both voltages negative and unequal, h) Both voltages negative and equal. In this chapter X, a detailed insight into this discovery is made with a mathematical derivation for the dual DC output voltage magnitude. Theoretical finding is confirmed by SIMULINK model simulation. The model is extended to verify the speed control, acceleration and braking of separately excited DC motors. Applications of this separately excited DC motor and Permanent Magnet DC motor for Hybrid Electric Vehicles and Electric Traction are highlighted.

2.10 DELTA-SIGMA MODULATION OF MATRIX CONVERTER: The chapter XI examines the recently proposed delta-sigma modulation technique for matrix converter [46-49]. A model of the three phase AC to three phase AC matrix converter using delta-sigma modulation technique is developed in SIMULINK [51]. Both Venturini [1-5] as well as advanced modulation algorithm [13-14, 16-17] are used for generating the modulation voltage signals. Simulation is carried out for a given sampling frequency. It is seen from simulation results that voltage harmonic peaks are reduced at integral multiples of sampling frequency [46-48]. The delta-sigma modulation technique can reduce noise peaks in the output voltage as compared to conventional PWM technique and has the advantage of maintaining noise regulation. Also performance of three phase induction motor drive fed by delta-sigma modulated MC using the above two algorithms are presented.

2.11 SINGLE PHASE AC TO THREE PHASE AC MATRIX CONVERTER: For single phase AC to three phase AC power conversion, three phase indirect method is used where the single phase AC is first rectified to DC and this DC link voltage is inverted to AC using three phase inverter. A control and designing method of the capacitance of the compensation capacitor for a direct single phase AC to three phase AC matrix converters with application to a variable speed induction motor is reported in the literature [50]. The amplitude of the compensation capacitor voltage is controlled to absorb the single phase power fluctuation along with the load power. A method is proposed to decide the input side parameters such as the capacitance of the compensation capacitor, considering the input voltage and the power of the IM [50]. A circuit configuration with a compensation capacitor in the input side is introduced which absorbs the fluctuating power due to the single phase AC power. Here the single phase AC source is connected to an LC filter and compensating capacitor [50]. The two nodes of the LC filter and the compensating capacitor end terminals are connected to nine bidirectional switches [50]. Indirect virtual rectifier-inverter analysis is used. Derivations for modulation ratio and output power flow are presented [50]. A method of designing and selecting the compensating capacitor is given in terms of the output phase voltage, output power flow and input frequency [50]. In this chapter a detailed analysis of the single phase AC to three phase AC MC is presented. A model of this single phase AC to three phase AC MC is developed in SIMULINK [51].

Simulation results of the single phase AC to three phase AC MC is presented for both R-L load and three phase IM load.

2.12 A NOVEL AC TO AC CONVERTER USING A DC LINK: A novel method of generating a Pulse Width Modulated Single Phase and Three Phase variable frequency, variable voltage AC from the normal 220 Volts/440 Volts, Single Phase/Three phase 50 Hz AC supply mains using a step down transformer and an intermediate DC link is presented here.

2.13 MODEL VERIFICATION: This chapter provides the verification of models of **selected** three phase AC to three phase AC Matrix Converter topologies discussed in the previous chapters using either PSIM or PSCAD software [52-53].

2.14 CONCLUSIONS: This chapter provides the summary of contributions and conclusions drawn from the simulation results or performance of the three phase Matrix Converter models discussed in the previous chapters and suggestion for further research work.

2.15 APPENDIX: The first appendix provides the gate drive using PIC microcontroller PIC16F84A to generate 2kHz saw-tooth carrier waveform and also the gate drive for the bidirectional switches in the novel three phase AC to three phase AC converter using a DC link. The second appendix provides the speed control and braking of three phase IM fed by MC, highlighting applications for HEVs. The third appendix provides the list of publications from this thesis.

Chapter III

Modelling of Three Phase Matrix Converters Using Venturini and Optimum Venturini Modulation Algorithms

3.1 INTRODUCTION: Recently considerable interest is shown in the development of AC to AC converters also known as "Matrix Converters" for Adjustable Speed Drive applications [1-8]. Although several topologies for IGBT bidirectional switches have been proposed, the common emitter bidirectional switch topology is used here. The switching of the bidirectional switches in an MC is really complicated. Several algorithms have been proposed for switching the MC bidirectional switches. This chapter presents the model of the three phase AC to three phase AC MC using Venturini and Optimum Venturini modulation algorithms. The model is developed using the software SIMULINK [51]. Simulation results are presented.

3.2 MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER: A three phase AC to three phase AC matrix converter is shown in Fig. 3.1. While operating the Matrix

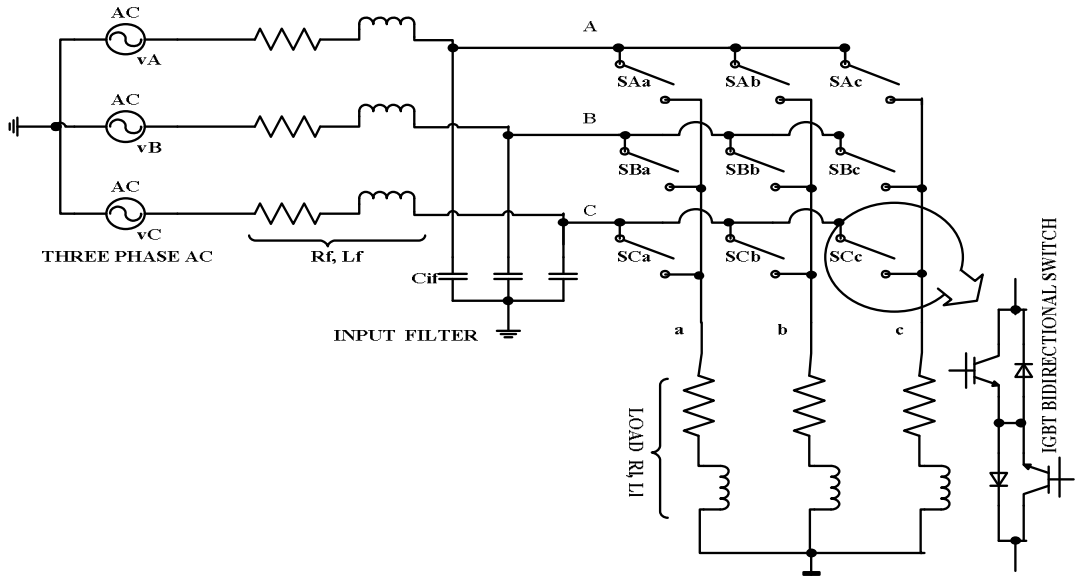


FIG. 3.1: THREE PHASE MATRIX CONVERTER

Converter, two essential points must be remembered. The three or any two combination of the bidirectional switches in any one output phase should NOT be closed at the same instant of time [4-5]. Referring to Fig. 3.1, if any two or all of switches SAa, SBa and SCa are closed simultaneously, the input lines are short circuited causing dangerous short circuit currents through the bidirectional switches. Similarly with inductive loads all the three bidirectional switches connected to an output phase should NOT be open simultaneously [4-5]. One switch at least in any output phase must remain closed. Matrix converter directly converts the AC input voltage at any given frequency to AC output voltage with arbitrary amplitude at any unrestricted frequency without the need for a dc link capacitor storage element at the input side. Sinusoidal input and output currents can be obtained with unity

power factor for any load. It has regeneration capability [1-5]. One limitation of the matrix converter is that the maximum output voltage available is limited to 86.6 % of the input voltage in the linear modulation range [4-5].

The introduction of bidirectional switch using power transistors made easy realization of the matrix converter. The real development of the matrix converter starts with the work of Venturini and Alesina who proposed a mathematical analysis and introduced the Low-Frequency Modulation Matrix concept to describe the low frequency behaviour of the matrix converter [1-3]. In this, the output voltages are obtained by multiplication of the modulation matrix or transfer matrix with the input voltages. Models for three phase ac to three phase ac matrix converters using Venturini modulation algorithm is reported [9-10]. These models are developed in SIMULINK [51].

The 3 X 3 matrix converter shown in Fig.3.1 connects the three phase AC source to the three phase load. The switching Function for a 3 X 3 matrix converter can be defined as follows [4-5]:

$$S_{Kj} = \begin{cases} 1 \ when \ S_{Kj} \ \ is \ closed \\ 0 \ when \ S_{Kj} \ \ is \ open \end{cases} \qquad (3.1)$$
$$K \in \{A, B, C\} \ and \ j \in \{a, b, c\}$$

The above constraint can be expressed in the following form:

$$S_{Aj} + S_{Bj} + S_{Cj} = 1 \qquad (3.2)$$
$$j \in \{a, b, c\}$$

With the above restrictions a 3 X 3 matrix converter has 27 possible switching states which are given in Table 1.1 of chapter I [25-30].

The mathematical expression that represents the operation of a three phase AC to three phase AC Matrix Converter (MC) can be expressed as follows [4-5]:

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} S_{Aa}(t) & S_{Ba}(t) & S_{Ca}(t) \\ S_{Ab}(t) & S_{Bb}(t) & S_{Cb}(t) \\ S_{Ac}(t) & S_{Bc}(t) & S_{Cc}(t) \end{bmatrix} * \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} \qquad (3.3)$$

$$\begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} = \begin{bmatrix} S_{Aa}(t) & S_{Ba}(t) & S_{Ca}(t) \\ S_{Ab}(t) & S_{Bb}(t) & S_{Cb}(t) \\ S_{Ac}(t) & S_{Bc}(t) & S_{Cc}(t) \end{bmatrix}^{T} * \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \qquad (3.4)$$

where va, vb and vc and iA, iB and iC are the output voltages and input currents respectively. To determine the behaviour of the MC at output frequencies well below the switching frequency, a modulation duty cycle can be defined for each switch. The modulation duty cycle M_{Kj} for the switch S_{Kj} in Fig.3.1 is defined as in equation 3.5 below.

$$M_{Kj} = \frac{t_{Kj}}{T_S} \qquad (3.5)$$
$$K \in \{A, B, C\} \ and \ j \ \in \ \{a, b, c\}$$

where t_{Kj} is the on time for the switch S_{Kj} between input phase $K \in \{A, B, C\}$ and $j \in \{a, b, c\}$ and T_S is the period of the PWM switching signal or sampling period. In terms of the modulation duty cycle, equations 3.2, 3.3 and 3.4 can be rewritten as given below.

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} M_{Aa}(t) & M_{Ba}(t) & M_{Ca}(t) \\ M_{Ab}(t) & M_{Bb}(t) & M_{Cb}(t) \\ M_{Ac}(t) & M_{Bc}(t) & M_{Cc}(t) \end{bmatrix} * \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} \qquad (3.6)$$

$$\begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} = \begin{bmatrix} M_{Aa}(t) & M_{Ba}(t) & M_{Ca}(t) \\ M_{Ab}(t) & M_{Bb}(t) & M_{Cb}(t) \\ M_{Ac}(t) & M_{Bc}(t) & M_{Cc}(t) \end{bmatrix}^{\boldsymbol{T}} * \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \qquad (3.7)$$

$$M_{Aj} + M_{Bj} + M_{Cj} = 1 \qquad (3.8)$$

$$j \in \{a, b, c\}$$

3.3 VENTURINI AND OPTIMUM VENTURINI MODULATION ALGORITHM: The modulation problem normally encountered in matrix Converter can be stated as follows:

The input voltages and output currents are given as defined in equation 3.9 and 3.10 below [1-5]:

$$v_i = \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = V_{im} * \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t - \frac{2\pi}{3}) \\ \cos(\omega_i t - \frac{4\pi}{3}) \end{bmatrix} \qquad (3.9)$$

$$io = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = I_{om} * \begin{bmatrix} \cos(\omega_o t + \varphi_o) \\ \cos(\omega_o t + \varphi_o - \frac{2\pi}{3}) \\ \cos(\omega_o t + \varphi_o - \frac{4\pi}{3}) \end{bmatrix} \qquad (3.10)$$

Where ω_i, ω_o and φ_0 are the input and output angular frequency and output phase displacement angle. The problem is to find a modulation matrix M(t) such that equations 3.11 and 3.12 below and the constraint in equation 3.8 are satisfied.

$$v_o = M(t) * v_i = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = q * V_{im} * \begin{bmatrix} \cos(\omega_o t + \varphi_o) \\ \cos\left(\omega_o t + \varphi_o - \frac{2\pi}{3}\right) \\ \cos\left(\omega_o t + \varphi_o - \frac{4\pi}{3}\right) \end{bmatrix} \qquad (3.11)$$

where $q * V_{im} = V_{om}$

$$i_i = [M(t)]^T * i_O = \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \frac{q * cos(\varphi_o)}{cos(\varphi_i)} * I_{om} * \begin{bmatrix} \cos(\omega_i t + \varphi_i) \\ \cos\left(\omega_i t + \varphi_i - \frac{2\pi}{3}\right) \\ \cos\left(\omega_i t + \varphi_i - \frac{4\pi}{3}\right) \end{bmatrix} \qquad (3.12)$$

where q is the voltage transfer ratio, φ_i is the input phase displacement angle. The solution of equations 3.9 to 3.12 can be expressed as in equations 3.13 and 3.14 below for $\varphi_i = \varphi_o$ and for $\varphi_i = -\varphi_o$ respectively.

$$M1 = \frac{1}{3} * \begin{bmatrix} 1 + 2q.cos(\omega_m t) & 1 + 2q.cos\left(\omega_m t - \frac{2\pi}{3}\right) & 1 + 2q.cos\left(\omega_m t - \frac{4\pi}{3}\right) \\ 1 + 2q.cos\left(\omega_m t - \frac{4\pi}{3}\right) & 1 + 2q.cos(\omega_m t) & 1 + 2q.cos\left(\omega_m t - \frac{2\pi}{3}\right) \\ 1 + 2q.cos\left(\omega_m t - \frac{2\pi}{3}\right) & 1 + 2q.cos\left(\omega_m t - \frac{4\pi}{3}\right) & 1 + 2q.cos(\omega_m t) \end{bmatrix} \quad (3.13)$$

where $\omega_m = (\omega_o - \omega_i)$

$$M_2 = \frac{1}{3} * \begin{bmatrix} 1 + 2q.cos(\omega_m t) & 1 + 2q.cos\left(\omega_m t - \frac{2\pi}{3}\right) & 1 + 2q.cos\left(\omega_m t - \frac{4\pi}{3}\right) \\ 1 + 2q.cos\left(\omega_m t - \frac{2\pi}{3}\right) & 1 + 2q.cos\left(\omega_m t - \frac{4\pi}{3}\right) & 1 + 2q.cos(\omega_m t) \\ 1 + 2q.cos\left(\omega_m t - \frac{4\pi}{3}\right) & 1 + 2q.cos(\omega_m t) & 1 + 2q.cos\left(\omega_m t - \frac{2\pi}{3}\right) \end{bmatrix} \quad (3.14)$$

where $\omega_m = -(\omega_o - \omega_i)$

This basic solution gives the direct transfer function approach. During each switching sequence Ts, the average output voltage is equal to the demand or target output voltage. The target output voltage must fit into the input voltage envelope for any output frequency. Also combining the two solutions in equation 3.13 and 3.14 gives a method for input displacement factor control. This can be expressed as in equation 3.15 and 3.16 below:

$$M(t) = \alpha_1 * M_1(t) + \alpha_2 * M_2(t) \quad (3.15)$$

$$(\alpha_1 + \alpha_2) = 1 \quad (3.16)$$

For unity input phase displacement factor $\alpha_1 = \alpha_2 = 0.5$. For unity input displacement factor, the modulation function can be expressed as in equation 3.17 below:

$$M_{Kj} = \frac{t_{Kj}}{T_s} = \left[\frac{1}{3} + \frac{2v_K.v_j}{3.V_{im}^2}\right] \quad (3.17)$$

$$for\ K = A, B, C\ and\ j = a, b, c$$

This method has little practical significance because of the 50 % voltage ratio limitation. Venturini's optimum method employs a common mode addition technique defined in equation 3.18 below:

$$vo = q * V_{im} * \begin{bmatrix} \cos(\omega_o t) - \frac{1}{6} * \cos(3\omega_o t) + \frac{1}{2\sqrt{3}} * \cos(3\omega_i t) \\ \cos\left(\omega_o t + \frac{4\pi}{3}\right) - \frac{1}{6} * \cos(3\omega_o t) + \frac{1}{2\sqrt{3}} * \cos(3\omega_i t) \\ \cos\left(\omega_o t + \frac{2\pi}{3}\right) - \frac{1}{6} * \cos(3\omega_o t) + \frac{1}{2\sqrt{3}} * \cos(3\omega_i t) \end{bmatrix} \quad (3.18)$$

The target output voltage using equation 3.18 is 86.6 % of the input voltage. In this case equation 3.17 is modified to equation 3.19 shown below:

$$M_{Kj} = \frac{t_{Kj}}{T_s} = \left[\frac{1}{3} + \frac{2v_K.v_j}{3.V_{im}^2} + \frac{4q}{9\sqrt{3}} * \sin(\omega_i t + \beta_K) * \sin(3\omega_i t)\right] \quad (3.19)$$

$$for\ K = A, B, C\ and\ j = a, b, c\ and\ \beta_K = 0, \frac{2\pi}{3}, \frac{4\pi}{3}\ for\ K = A, B, C\ respectively.$$

In equation 3.19, v_j include the common mode addition defined in equation 3.18.

3.4 MODEL DEVELOPMENT: To study the behaviour of the three phase AC to three phase AC MC using Venturini and Optimum Venturini Modulation algorithm, a model of this matrix converter

is developed in SIMULINK [51]. The data shown in TABLE 3.1 are used to develop the model for all the above algorithms. The MC switching is developed based on equations 3.13, 3.17, 3.18 and 3.19.

TABLE 3.1: Model Parameters

Sl. No.	Modulation Index q	RMS Line to Neutral Input Voltage (Volts)	Input Frequency Hz	Output Frequency Hz	Carrier Frequency kHz
1	0.4	220	50	50	2

3.4.1 MODEL OF A MATRIX CONVERTER USING VENTURINI FIRST METHOD: The model of the three phase MC is developed using equation 3.13 for the data shown in Table 3.1. Equation 3.13 is proved in A3.2 Appendix in this chapter. The input and the output voltage are defined in equations 3.9 and 3.11. The nine modulation functions defined in equation 3.13 is developed using Embedded MATLAB Function in SIMULINK. These modulation functions are compared with a 2 kHz saw-tooth carrier generator and the gate pulses for the nine bidirectional switches are developed satisfying the constraint in equation 3.8 using another Embedded MATLAB Function. The source code used to generate the nine gate pulses is given below:

```
function [tAa,tBa,tCa,tAb,tBb,tCb,tAc,tBc,tCc] = fcn(MAa,MBa,MCa,MAb,MBb,MCb,MAc,MBc,MCc,vsaw)
%%Narayanaswamy.P.R.Iyer
if(vsaw < MAa )
   tAa = 1;
else
   tAa = 0;
end
if(vsaw < (MAa+MBa))
   tABab = 1;
else
   tABab = 0;
end
tBa = (~tAa & tABab);
tCa = ~(tABab);
if (vsaw < MAb)
   tAb = 1;
else
   tAb = 0;
end
if (vsaw < (MAb + MBb))
   tBAba = 1;
else
   tBAba = 0;
end
tBb = (tBAba & ~tAb);
tCb = ~(tBAba);
if (vsaw < MAc)
   tAc = 1;
else
   tAc = 0;
end
if (vsaw < (MAc + MBc))
   tBAca = 1;
else
   tBAca = 0;
end
tBc = (tBAca & ~tAc);
tCc = ~(tBAca);
```

In the source code above, the less than (<) and the plus (+) sign can be generated using op. amp. comparator and summer and the logic operation AND (&) and NOT (~) can be developed using integrated circuits AND and NOT gates respectively.

The nine bidirectional switches are the IGBT/diode model in the power electronics library and the Three Phase AC source used as input voltage is from the Electrical Sources library in the SimPowersystems blockset.

The three phase cosine input voltage as defined in equation 3.9 with data as in Table 3.2 can be generated by entering 90 in the box corresponding to Phase angle of phase A (degrees)", 50 in the box for frequency and 381.04 in the box for phase-to-phase rms voltage (V) in the three phase AC Source model.

The model of the three phase MC using Venturini First method developed in SIMULINK is shown in Fig. 3.2. A balanced three phase R-L load of 50 Ohms and 0.5 H is used. This R-L load is from the Elements library in the SimPowersystems blockset. The Three phase V-I measurement and Single phase Voltage measurement blocks are from the Measurements library in the SimPowersystems blockset.

3.4.2 SIMULATION RESULTS: The simulation of the MC using the Venturini First Method using the data in Table 3.1 is carried out using SIMULINK. The Fixed step ode3 (Bogacki-Shampine) solver is used. Harmonic spectrum of the line to neutral output voltage, phase A input current and line to line output voltage are shown in Fig. 3.3. to Fig. 3.5 respectively. The simulation results for the three phase line to neutral output voltage , phase A input current, three phase line to line output voltage and three phase load current are shown in Fig. 3.6 to Fig. 3.9 respectively. The simulation results from the harmonic spectrum are tabulated in Table 3.2 below. The 2 kHz saw-tooth carrier waveform and the gate pulse for the nine bidirectional switches are shown in Fig. 3.10 and Fig. 3.11 respectively.

3.4.3 MODEL OF A MATRIX CONVERTER USING VENTURINI SECOND METHOD: The model of the three phase MC is developed using equation 3.17 for the data shown in Table 3.1. Unity input phase displacement factor is assumed. The input voltage is defined in equation 3.9 and the output voltage in 3.11. The nine modulation functions defined in equation 3.17 is developed using Embedded MATLAB Function in SIMULINK. These modulation functions are compared with a 2 kHz saw-tooth carrier generator and the gate pulses for the nine bidirectional switches are developed satisfying the constraint in equation 3.8 using another Embedded MATLAB Function. The source code used to generate the nine gate pulses and the method of development of the model are already explained in section 3.4.1 in this chapter.

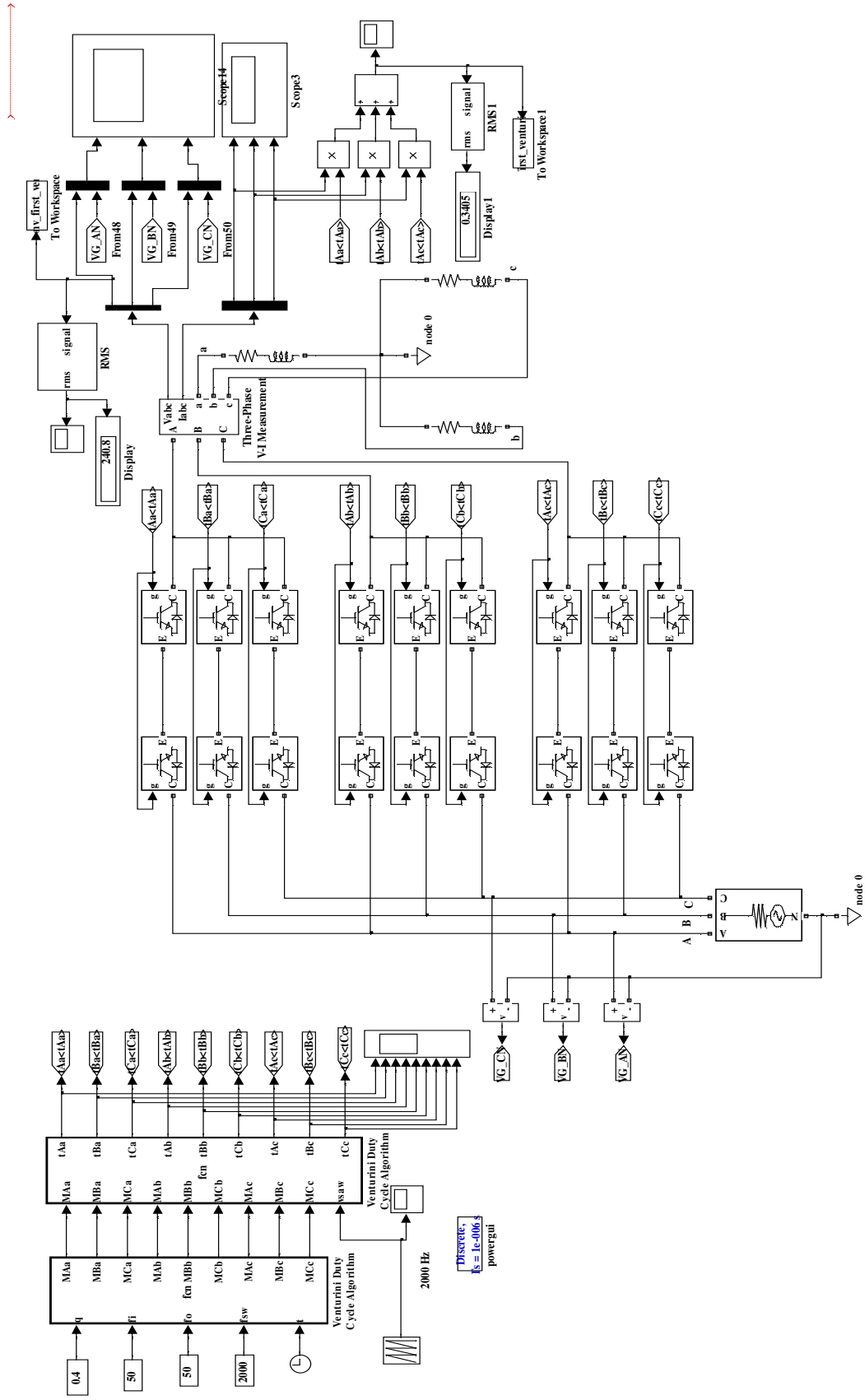
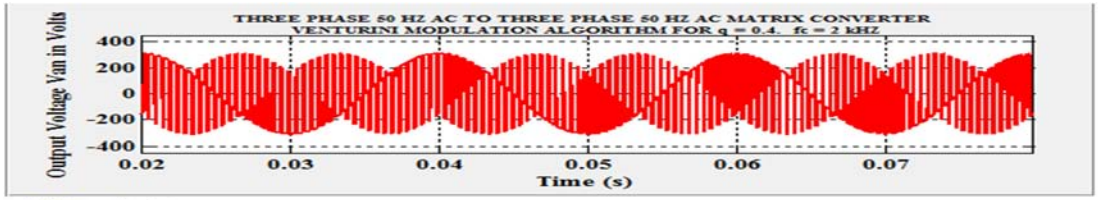


FIG. 3. 2: MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING VENTURINI FIRST METHOD



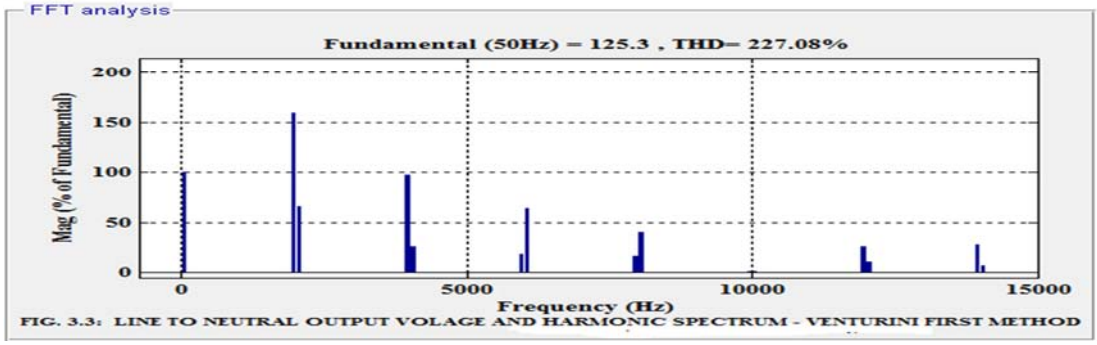
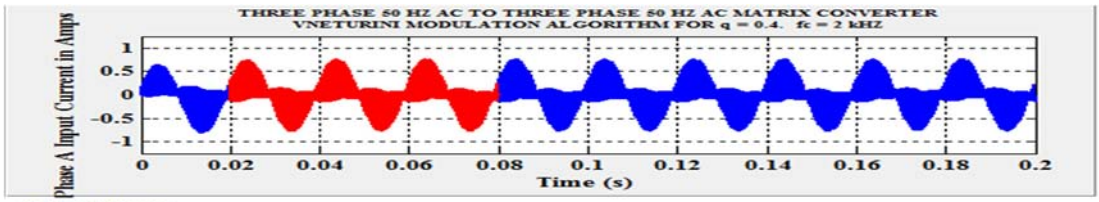


FIG. 3.3: LINE TO NEUTRAL OUTPUT VOLAGE AND HARMONIC SPECTRUM - VENTURINI FIRST METHOD



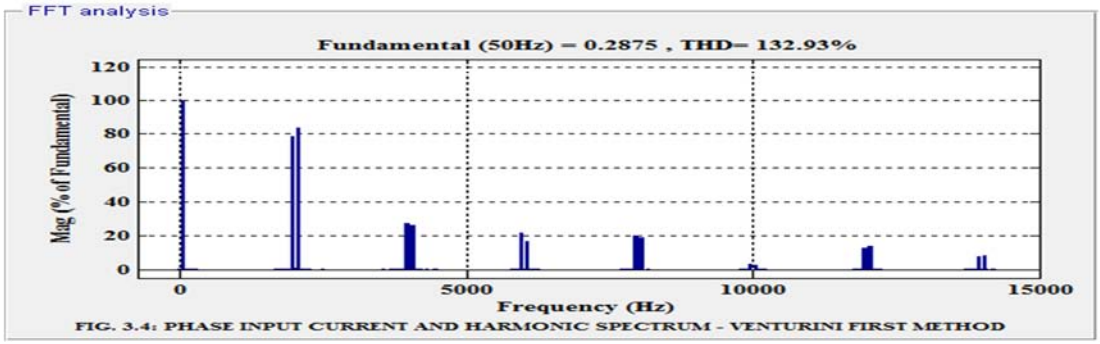
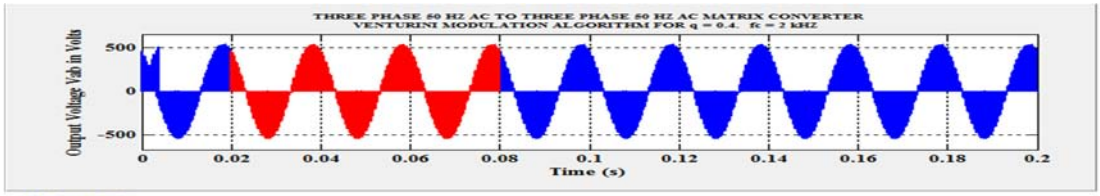


FIG. 3.4: PHASE INPUT CURRENT AND HARMONIC SPECTRUM - VENTURINI FIRST METHOD



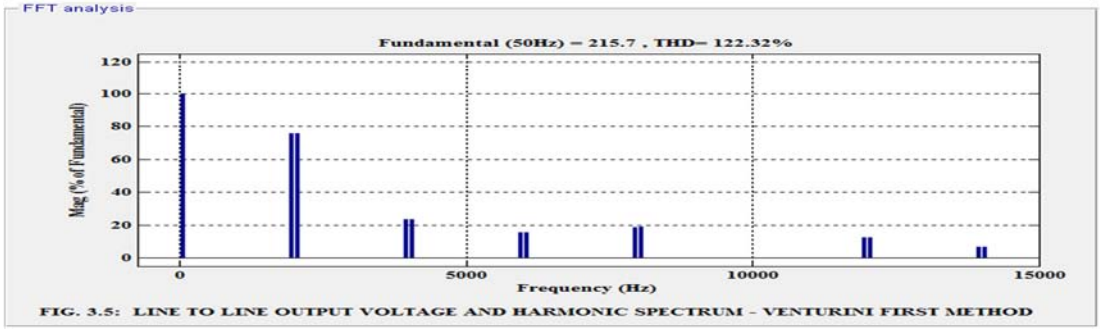


FIG. 3.5: LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM - VENTURINI FIRST METHOD

TABLE 3.2: Model Simulation Results 1

Sl.No.	Algorithm	THD of Line to Neutral Output Voltage (p.u.)	THD Line to Line Output Voltage (p.u.)	THD of Input Current (p.u.)
1	Venturini First Method	2.27	1.22	1.329

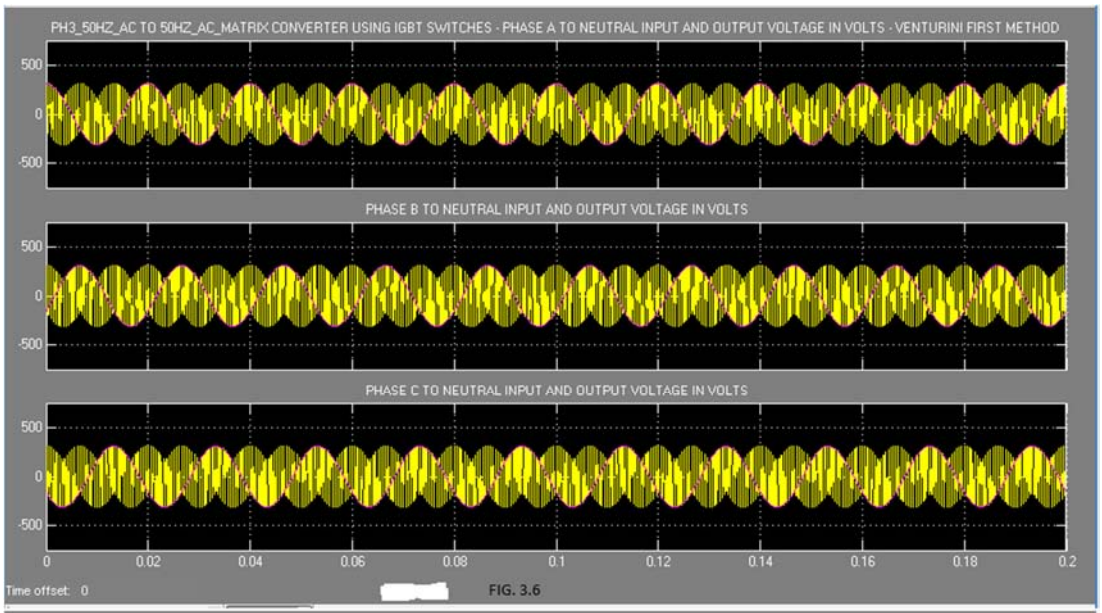


FIG. 3.6

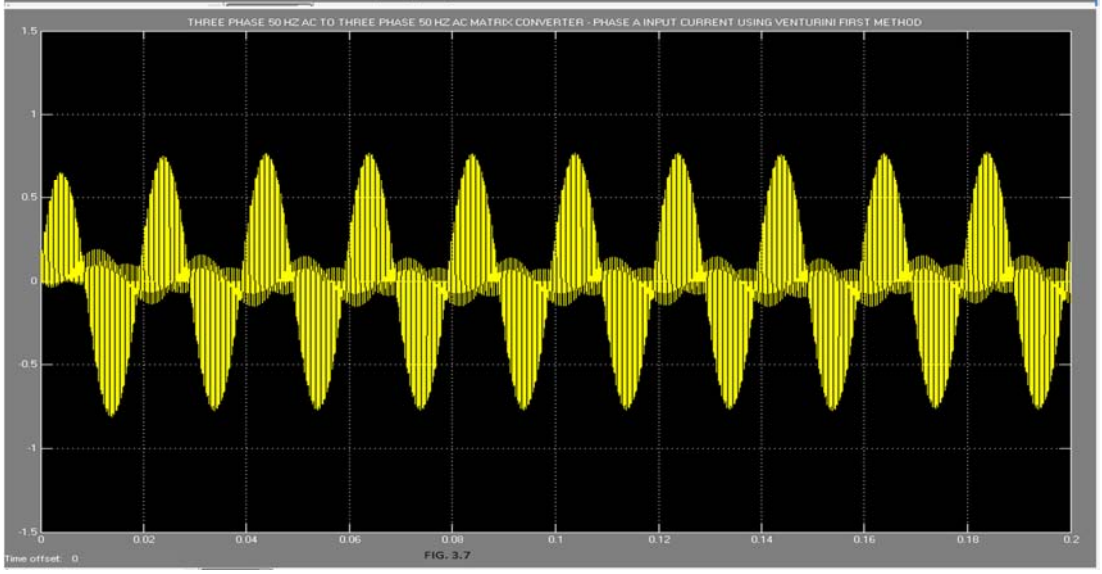


FIG. 3.7

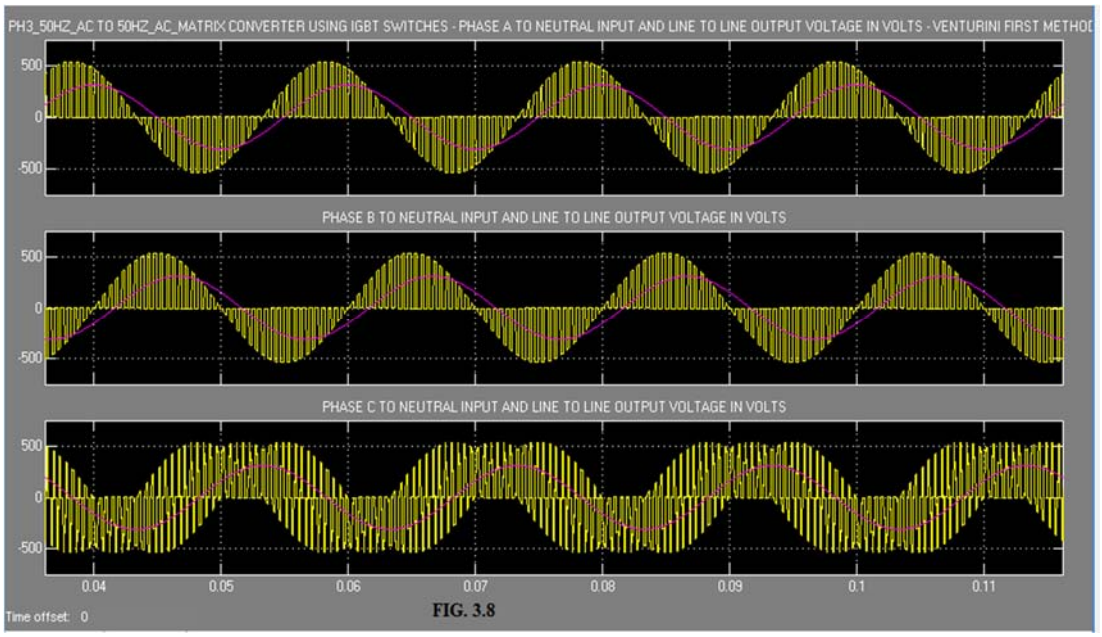


FIG. 3.8

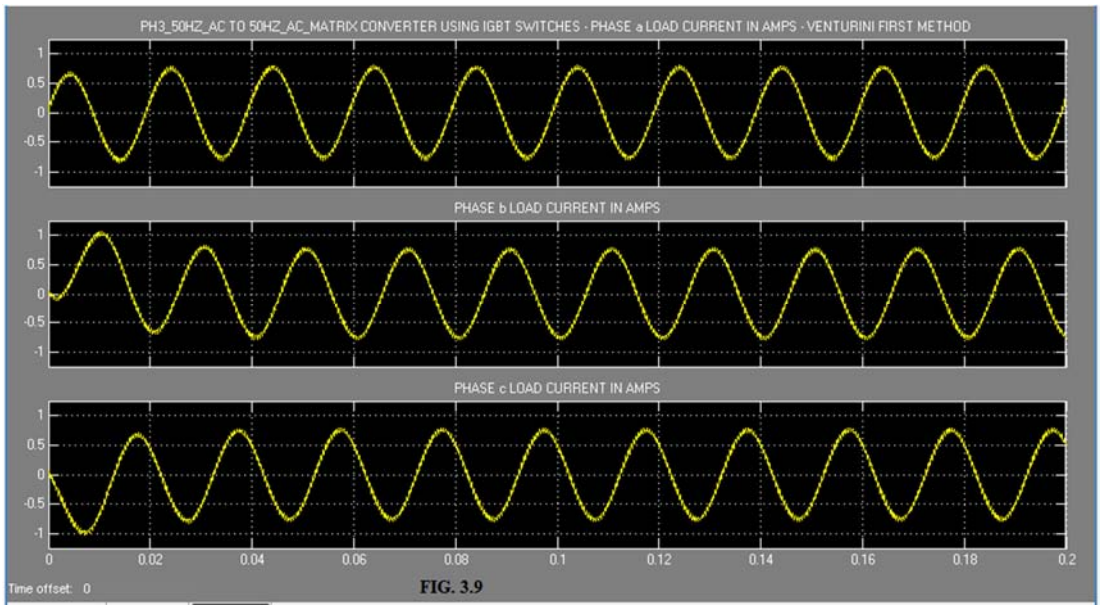


FIG. 3.9

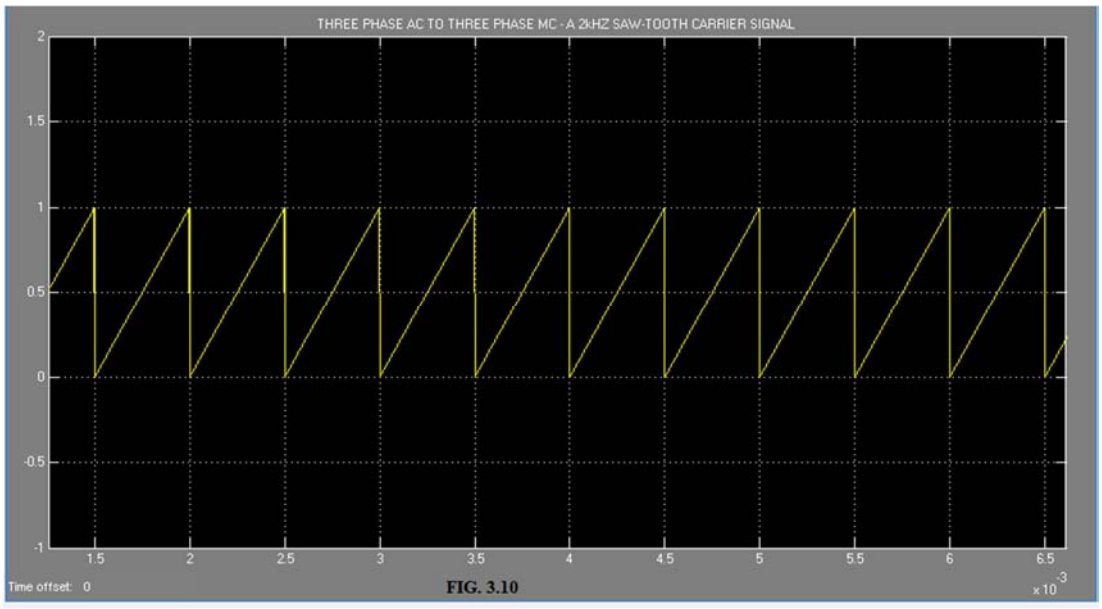


FIG. 3.10

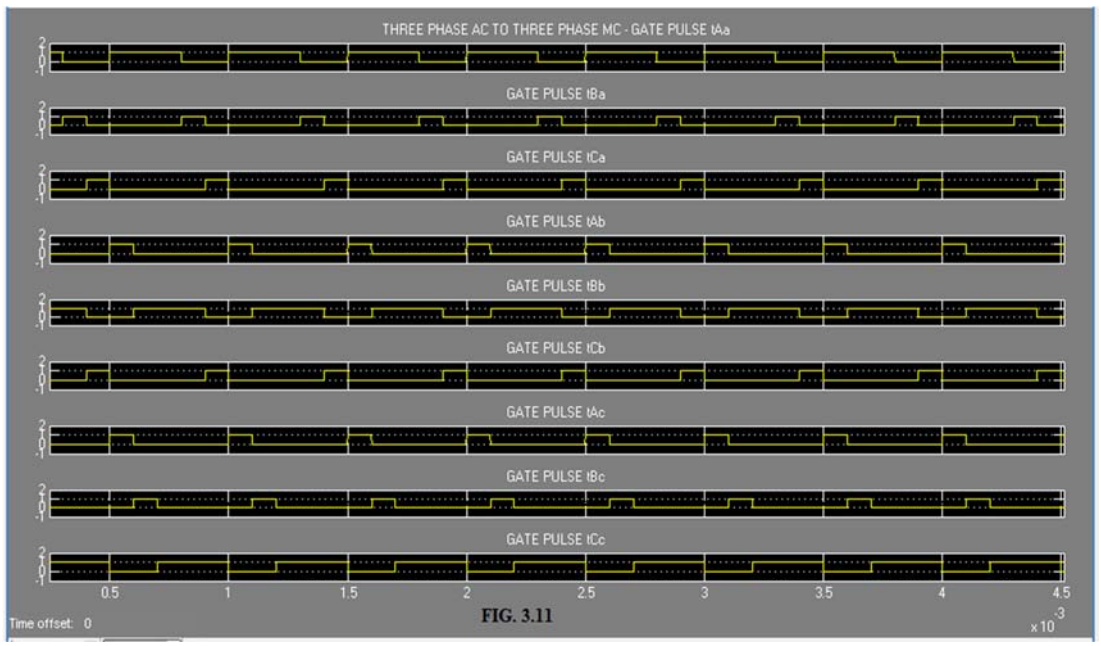


FIG. 3.11

At this stage it is worth noting that the three phase AC voltage generated by the grid is a sine wave of the form given below:

$$V_K = V_{im} * \sin(\omega_i . t - \gamma) \qquad (3.20)$$

$$where\ K = Input\ Phase\ A, B, C\ \ for\ \gamma = 0, \frac{2\pi}{3}, \frac{4\pi}{3}\ \ respectively.$$

The equation 3.17 is proved valid in Appendix A3.3 in this chapter both for three phase cosine wave and sine wave input and output voltages respectively. Hence although input and output voltages are defined in equations 3.9 and 3.11, a phase lag of π/2 radians is intentionally applied to these three phase input and output voltages so that this MC model by Venturini second method gains practical significance. The model of the three phase MC using Venturini second method developed in SIMULINK is shown in Fig. 3.12. In this model, the three phase cosine wave input and output voltages defined in equation 3.9 and 3.11 each made to phase lag by π/2 radians is used.

3.4.4 SIMULATION RESULTS: The simulation of the MC using the Venturini second Method using the data in Table 3.1 is carried out using SIMULINK. The variable step ode15s (Stiff/NDF) solver is used. Harmonic Spectrum of the Line to neutral output voltage, Phase A Input Current and Line to Line output voltage are shown in Fig. 3.13. to Fig. 3.15 respectively. The simulation results for the three phase Line to neutral output voltage , Phase A input current, three phase Line to Line output voltage and three phase load current are shown in Fig. 3.16 to Fig. 3.19 respectively. The simulation results from the Harmonic Spectrum are tabulated in Table 3.3. The 2 kHz saw-tooth carrier signal and the gate pulse pattern are already shown for the Venturini First method and are not repeated here.

3.4.5 MODEL OF A MATRIX CONVERTER USING OPTIMUM VENTURINI MODULATION ALGORITHM: The model of the three phase MC is developed using equation 3.19 with the input and output voltages as defined in equation 3.9 and 3.18 respectively for the data given in Table 3.1. The nine modulation functions defined in equation 3.19 is developed using Embedded MATLAB Function in SIMULINK. These modulation functions are compared with a 2 kHz saw-tooth carrier generator and the gate pulses for the nine bidirectional switches are developed satisfying the constraint in equation 3.8 using another Embedded MATLAB Function. The source code used to generate the nine gate pulses and the method of development of the model are already explained in section 3.4.1 in this chapter. The SIMULINK model is shown in Fig. 3.20.

3.4.6 SIMULATION RESULTS: The simulation of the MC using the Optimum Venturini method using the data in Table 3.1 is carried out using SIMULINK. The variable step ode15s (Stiff/NDF) solver is used. Harmonic spectrum of the Line to neutral output voltage, Phase A input current and line to line output voltage are shown in Fig. 3.21. to Fig. 3.23 respectively. The simulation results for the three phase line to neutral output voltage , Phase A input current, three phase line to line output voltage and three phase load current are shown in Fig. 3.24 to Fig. 3.27 respectively. The simulation results from the harmonic spectrum are tabulated in Table 3.4. The 2 kHz saw-tooth carrier signal

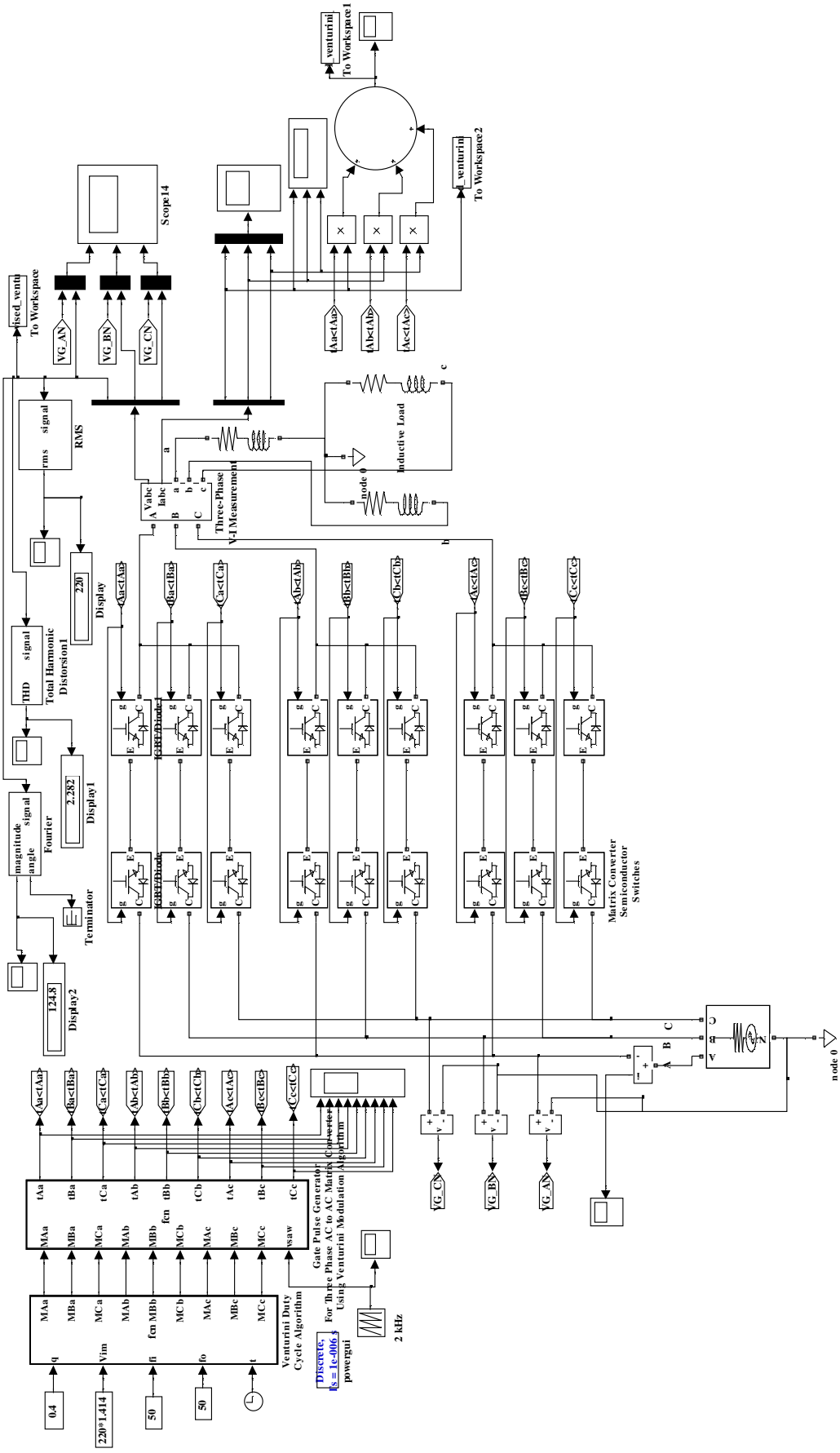


FIG. 3.12: MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING VENTURINI SECOND METHOD

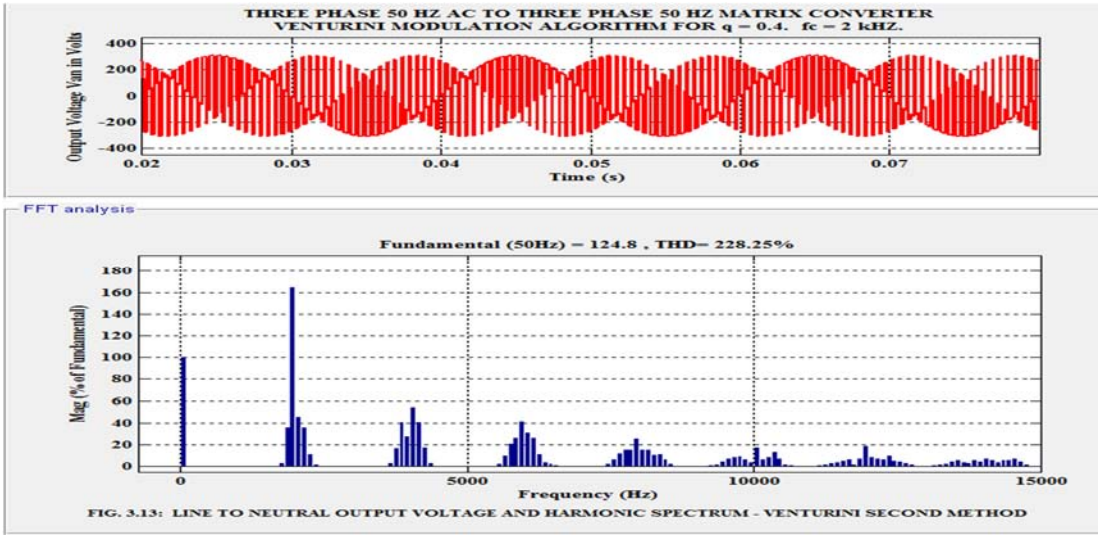


FIG. 3.13: LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM - VENTURINI SECOND METHOD

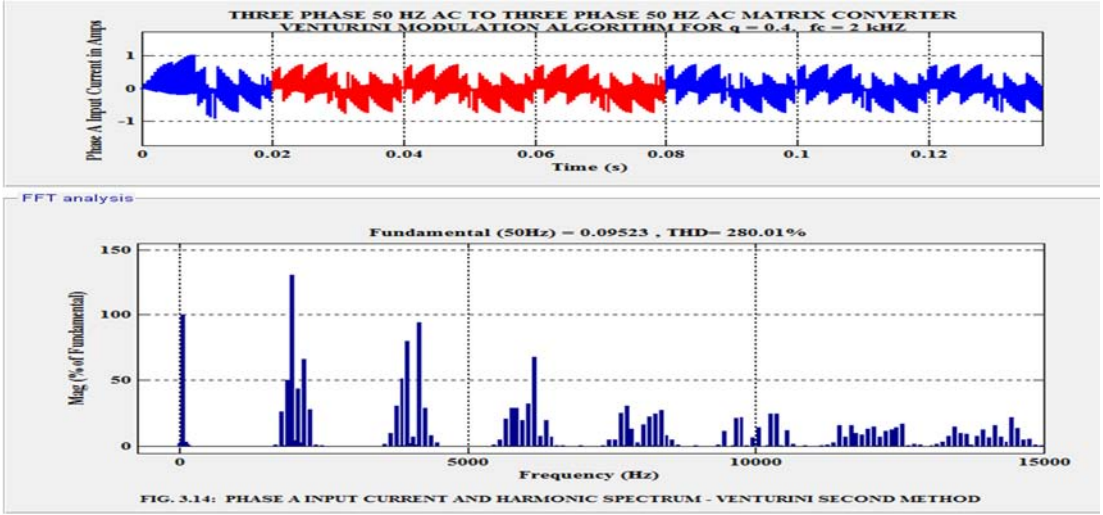


FIG. 3.14: PHASE A INPUT CURRENT AND HARMONIC SPECTRUM - VENTURINI SECOND METHOD

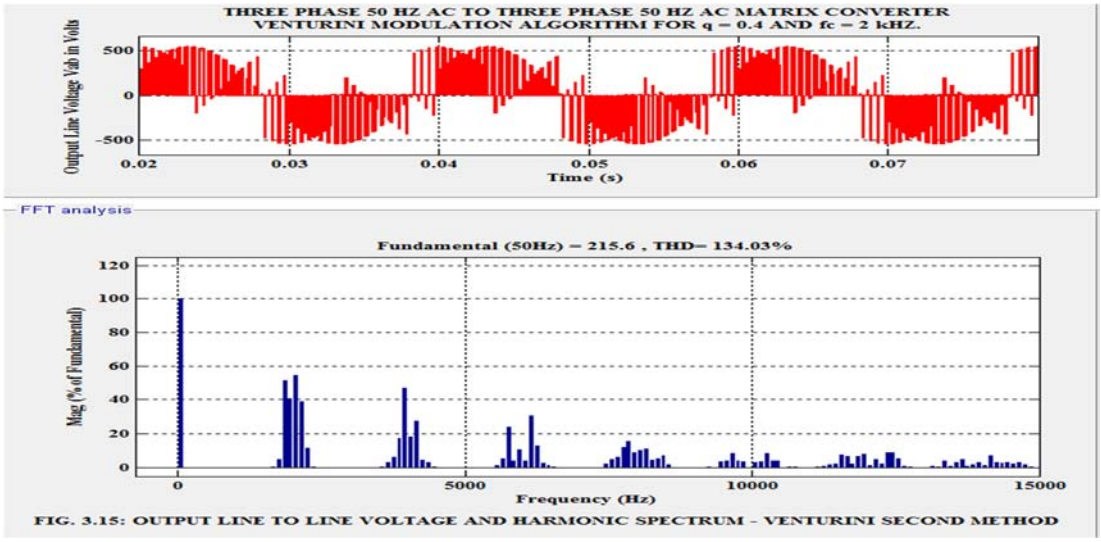


FIG. 3.15: OUTPUT LINE TO LINE VOLTAGE AND HARMONIC SPECTRUM - VENTURINI SECOND METHOD

TABLE 3.3: Model Simulation Results 2

Sl.No.	Algorithm	THD of Line to Neutral Output Voltage (p.u.)	THD Line to Line Output Voltage (p.u.)	THD of Input Current (p.u.)
1	Venturini Second Method	2.28	1.34	2.8

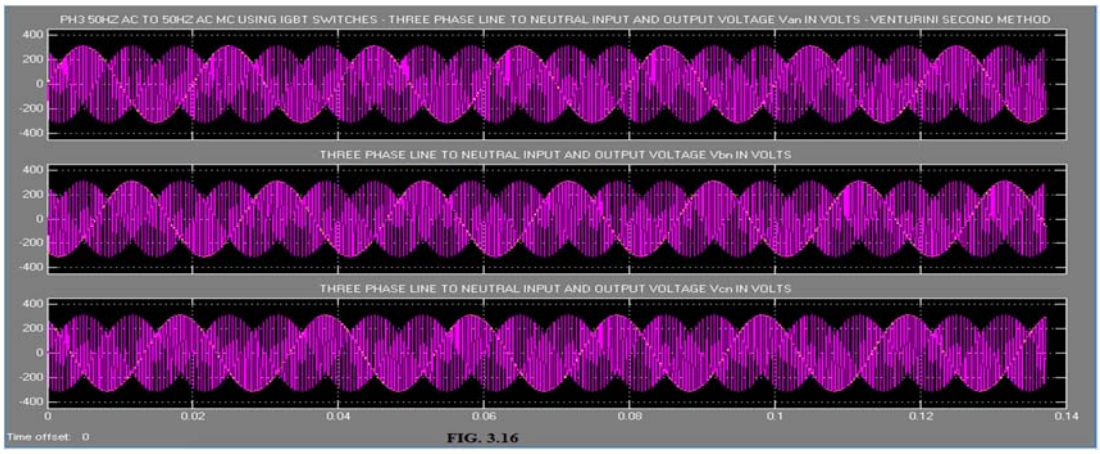


FIG. 3.16

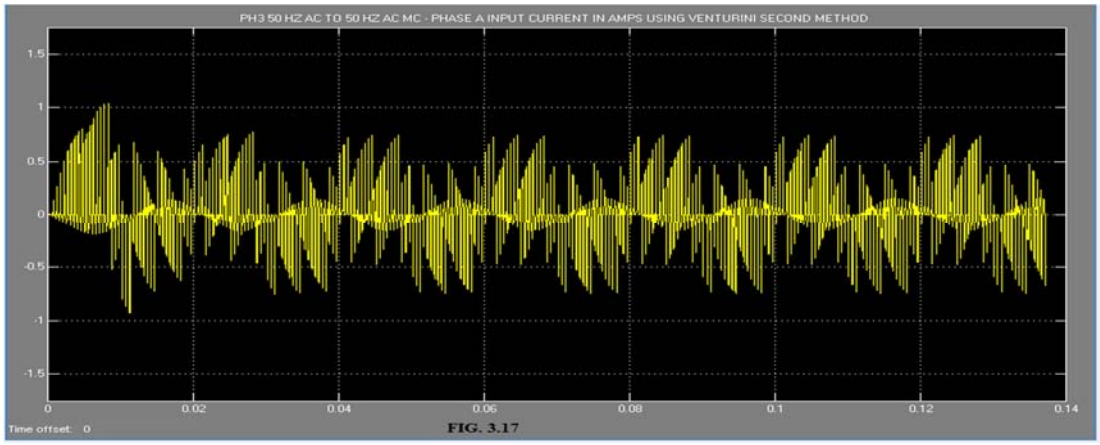


FIG. 3.17

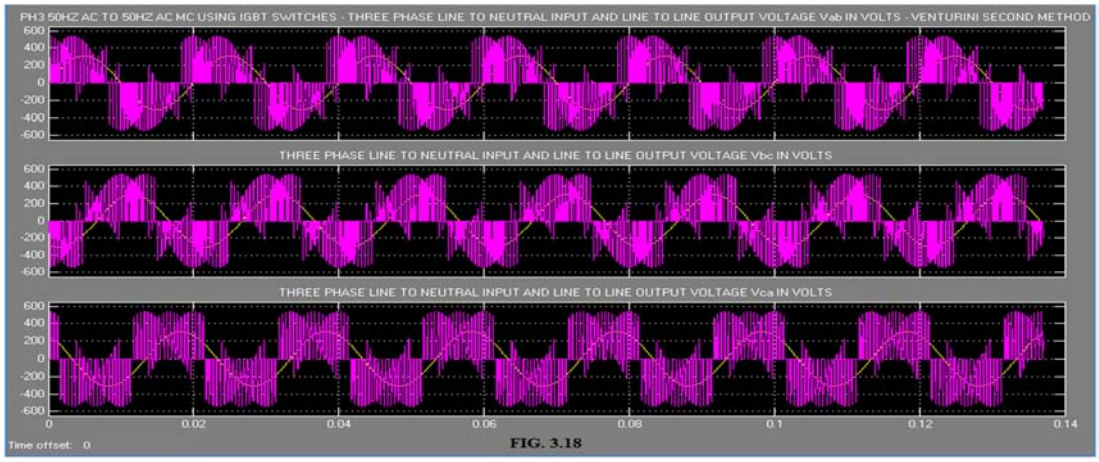


FIG. 3.18

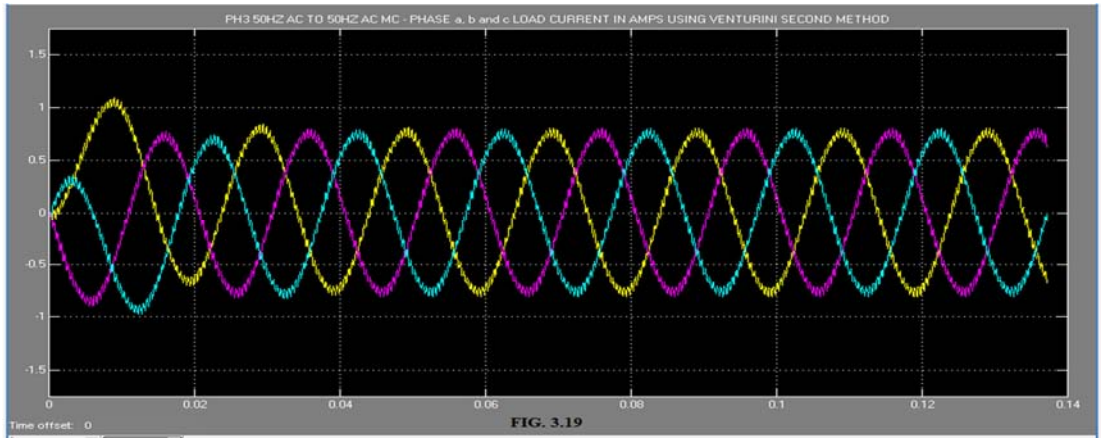


FIG. 3.19

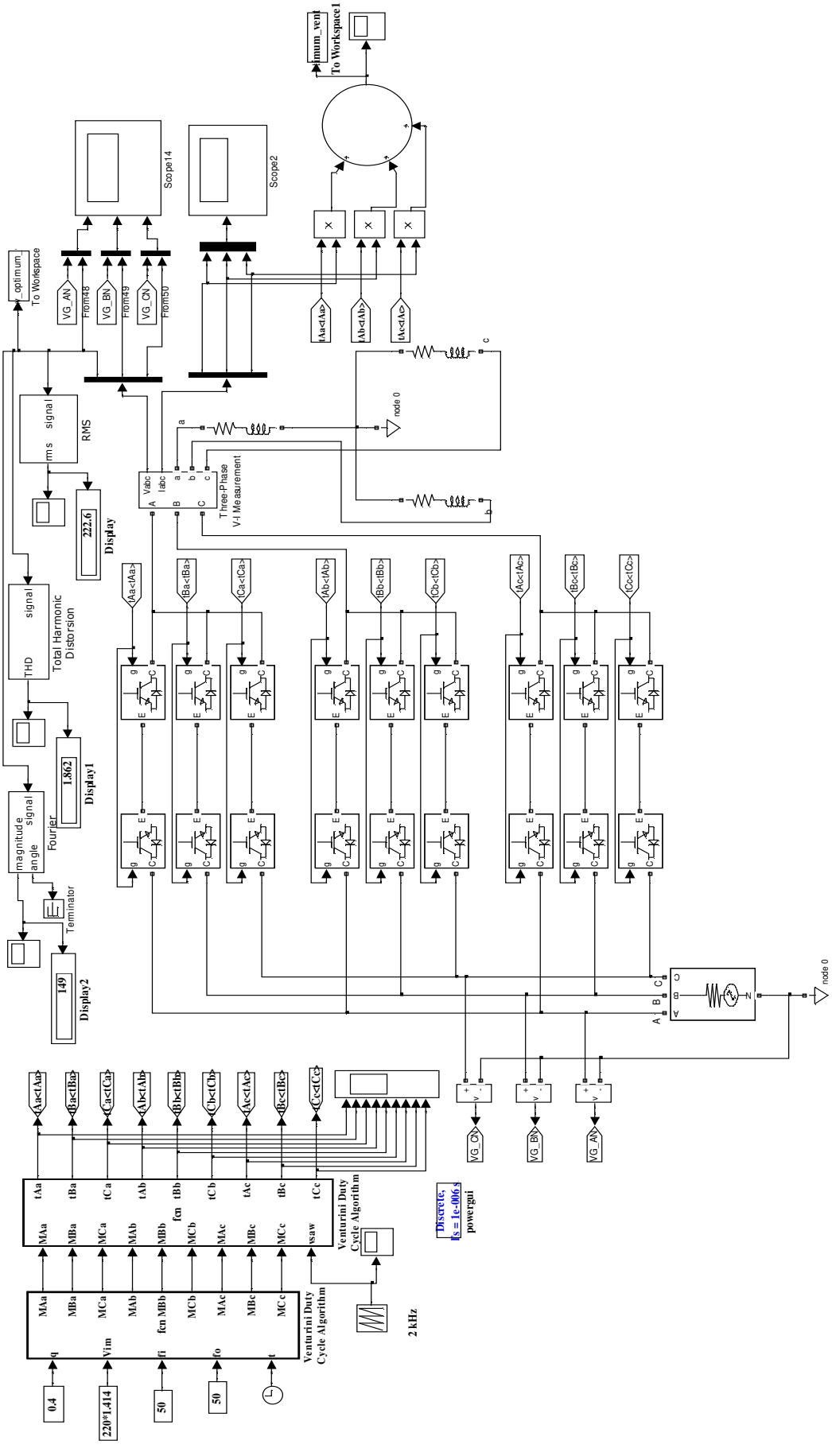


FIG. 3.20: OPTIMUM VENTURINI MODULATION ALGORITHM FOR THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER

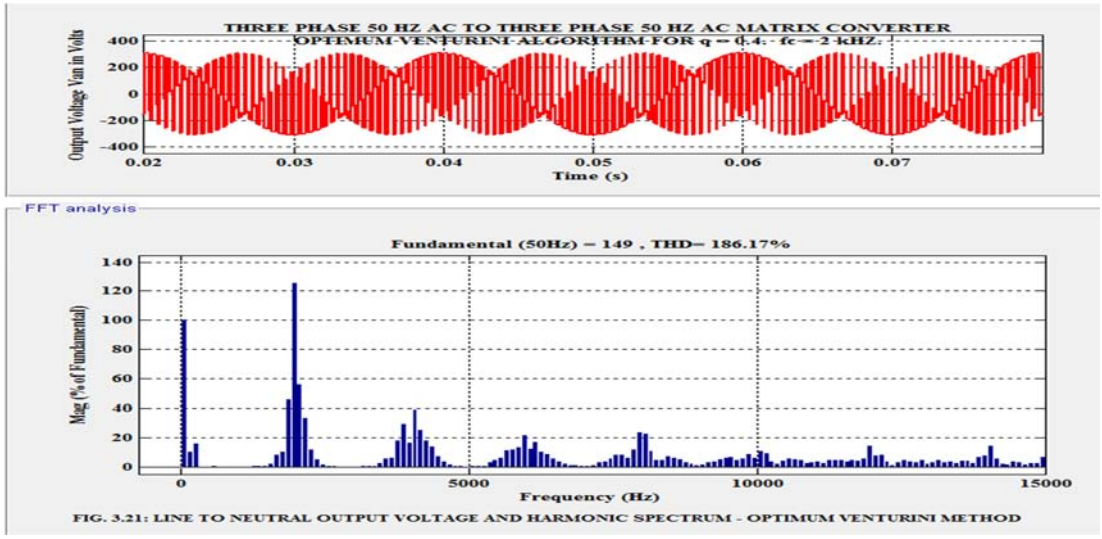


FIG. 3.21: LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM - OPTIMUM VENTURINI METHOD

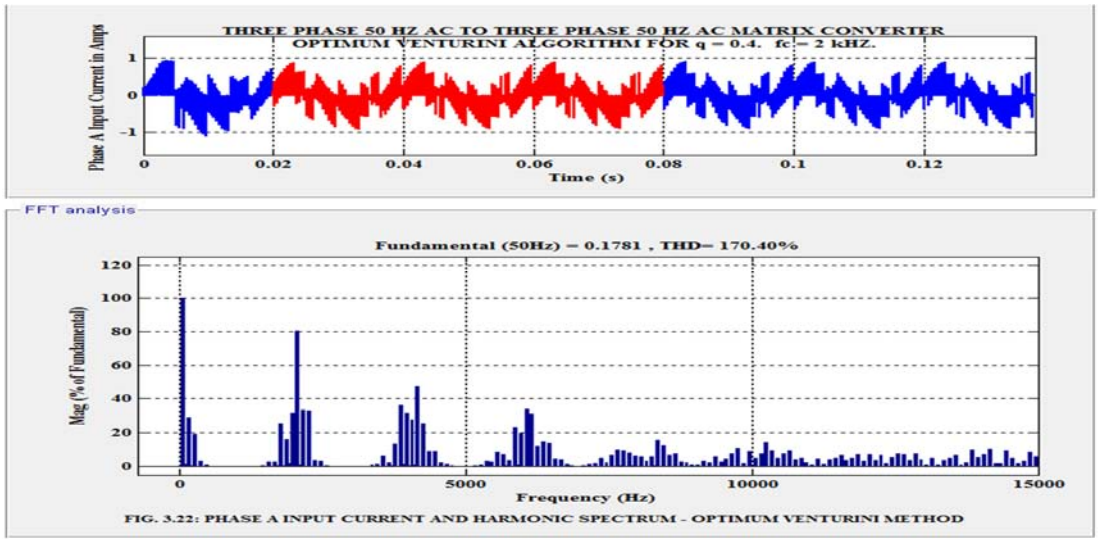


FIG. 3.22: PHASE A INPUT CURRENT AND HARMONIC SPECTRUM - OPTIMUM VENTURINI METHOD

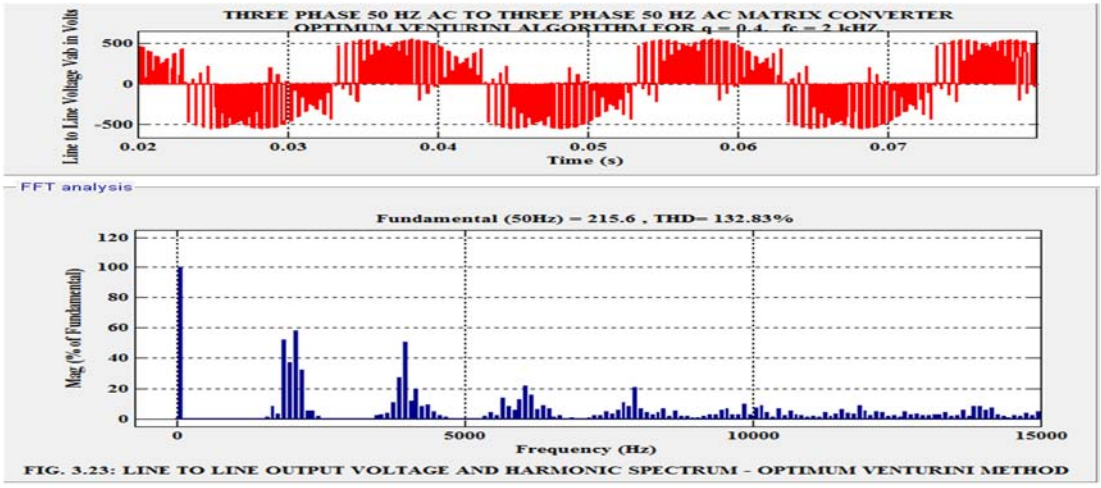


FIG. 3.23: LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM - OPTIMUM VENTURINI METHOD

TABLE 3.4: Model Simulation Results 3

Sl.No.	Algorithm	THD of Line to Neutral Output Voltage (p.u.)	THD Line to Line Output Voltage (p.u.)	THD of Input Current (p.u.)
1	Optimum Venturini	1.86	1.328	1.70

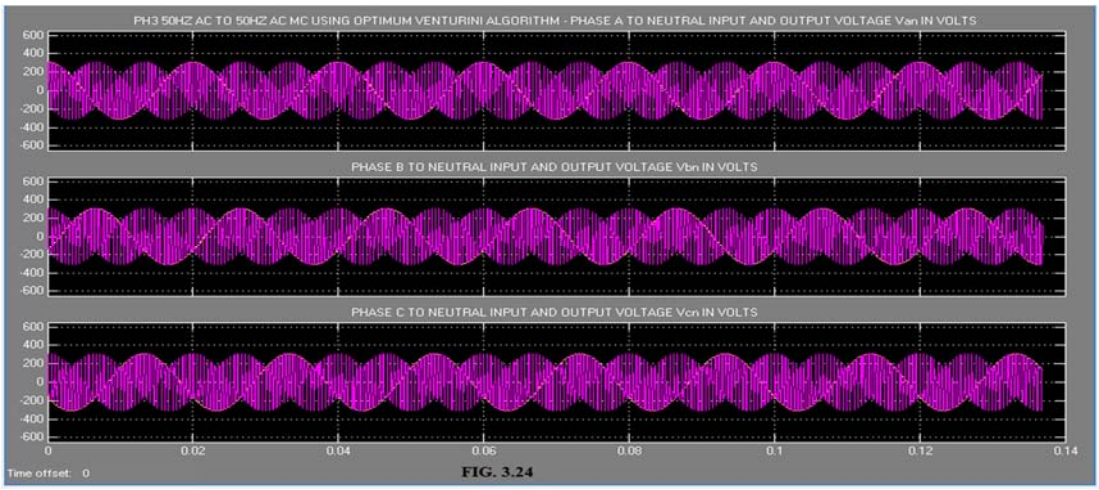


FIG. 3.24

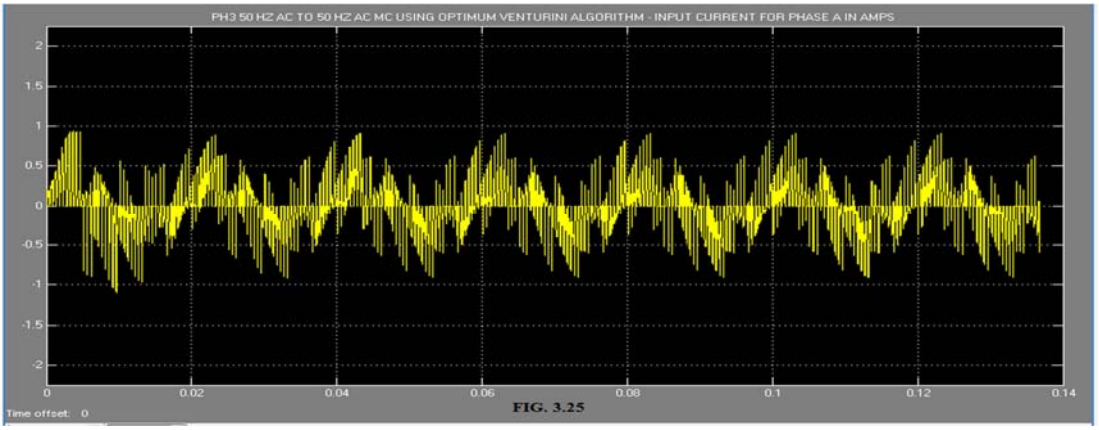


FIG. 3.25

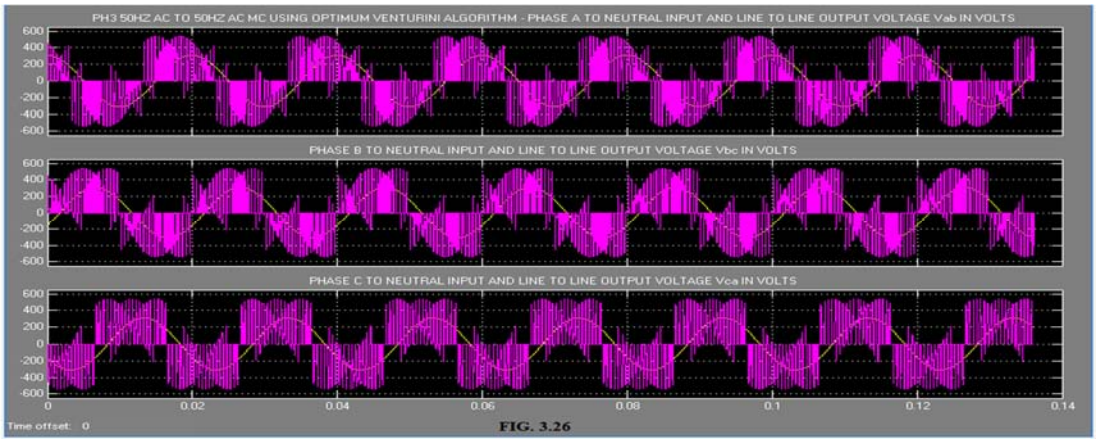


FIG. 3.26

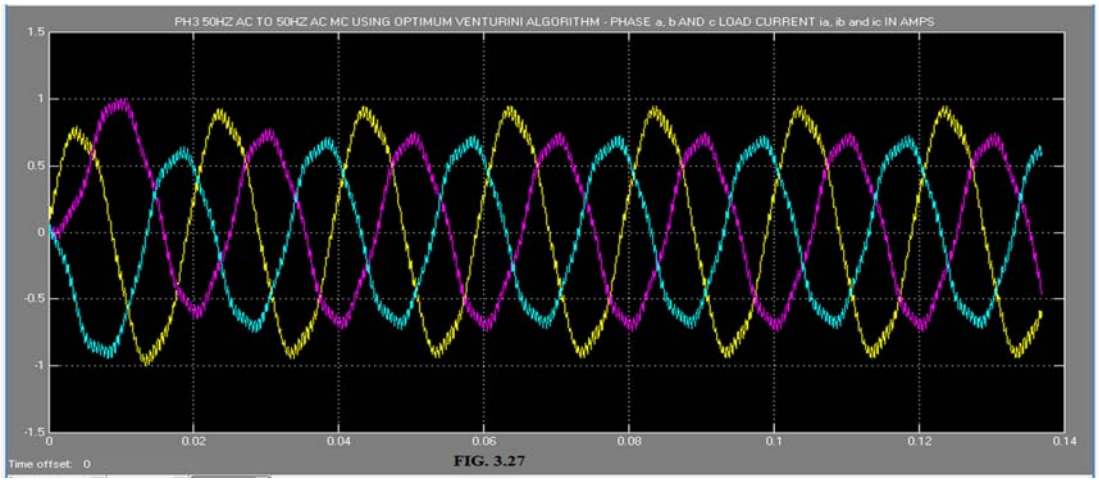


FIG. 3.27

and the gate pulse pattern are already shown for the Venturini First method and are not repeated here.

3.5 DISCUSSION OF RESULTS: Comparing the total harmonic distortion (THD) of line to neutral output voltage by the three methods, this value is minimum for optimum Venturini and maximum for Venturini second method. The THD for line to line output voltage and input current are minimum Venturini First method and maximum for Venturini second method in both cases. The linear modulation range for Venturini first and second method is 0 to 0.5 and for Optimum Venturini method is 0 to 0.866.

The application of Venturini algorithm second method for the speed control and brake by plugging of three phase induction motor fed by MC is presented in Appendix II.

3.6 CONCLUSIONS: This chapter examines the detailed development of the SIMULINK model by Venturini first, second and Optimum Venturini method. The modulation index used is within the linear modulation range for all the three methods. The predicted performance is valid for values of modulation index lying within this linear modulation range.

A3.1 APPENDIX: Case A**:** Consider the three phase input and output voltages as defined in equations 3.9 and 3.11. The nine modulation functions are defined in equation 3.13, using which the output voltage va across phase a can be expressed as follows:

$$v_a = q*V_{im}*\cos(\omega_O.t) = \frac{1}{3}*\left[\begin{array}{l}(1+2q.\cos(\alpha))*V_{im}\cos(\beta)+\left(1+2q.\cos\left(\alpha-\frac{2\pi}{3}\right)\right)*V_{im}\cos\left(\beta-\frac{2\pi}{3}\right)\\ +\left(1+2q.\cos\left(\alpha-\frac{4\pi}{3}\right)\right)*V_{im}\cos\left(\beta-\frac{4\pi}{3}\right)\end{array}\right] \quad (A3.1.1)$$

where $\alpha = \omega_m.t$, $\beta = \omega_i.t$ *and* $\omega_m = (\omega_i - \omega_O)$

Using the relation cos(A)*cos(B) = 0.5*cos(A+B) + 0.5*cos(A-B) in equation A3.1.1 and simplifying, we have the following equation:

$$v_a = \frac{V_{im}}{3}*\left[\begin{array}{l}\cos(\beta)+\cos\left(\beta-\frac{2\pi}{3}\right)+\cos\left(\beta-\frac{4\pi}{3}\right)+q*\left(\begin{array}{l}\cos(\alpha+\beta)+\cos\left(\alpha+\beta-\frac{4\pi}{3}\right)\\ +\cos\left(\alpha+\beta-\frac{8\pi}{3}\right)+\\ \cos(\alpha-\beta)+\cos(\alpha-\beta)+\\ \cos(\alpha-\beta)\end{array}\right)\end{array}\right] \quad (A3.1.2)$$

Equation A3.1.2 simplifies to the following:

$$\begin{aligned} v_a &= q*V_{im}*\cos(\alpha-\beta)\\ &= q*V_{im}*\cos(\omega_O.t) \quad (A3.1.3)\end{aligned}$$

Equation A3.1.3 well agree with the expression for output voltage va in the LHS of equation A3.1.1. This proves Venturini algorithm first method for three phase cosine wave input and output voltages.

Case B: Now consider the three phase input and output voltages defined in equation 3.9 and 3.11 all made to phase lag by 90 degrees so that they are now three phase sine wave input and output voltages at the respective frequencies. The nine modulation functions are defined in equation 3.13, using which the output voltage va across phase a can be expressed as follows:

$$v_a = q*V_{im}*\sin\left(\omega_O.t\right) = \frac{1}{3}*\begin{bmatrix}\left(1+2q.\cos(\alpha)\right)*V_{im}\sin(\beta)+\left(1+2q.\cos\left(\alpha-\frac{2\pi}{3}\right)\right)*V_{im}\sin\left(\beta-\frac{2\pi}{3}\right)\\ +\left(1+2q.\cos\left(\alpha-\frac{4\pi}{3}\right)\right)*V_{im}\sin\left(\beta-\frac{4\pi}{3}\right)\end{bmatrix} \quad (A3.1.4)$$

where $\alpha = \omega_m.t$, $\beta = \omega_i.t$ *and* $\omega_m = \left(\omega_i - \omega_O\right)$

Using the relation sin(A)*cos(B) = 0.5*sin(A+B) + 0.5*sin(A-B) in equation A3.1.4 and simplifying, we have the following equation:

$$v_a = \frac{V_{im}}{3}*\begin{bmatrix}\sin(\beta)+\sin\left(\beta-\frac{2\pi}{3}\right)+\sin\left(\beta-\frac{4\pi}{3}\right)+q*\begin{pmatrix}\sin(\alpha+\beta)+\sin\left(\alpha+\beta-\frac{4\pi}{3}\right)\\ +\sin\left(\alpha+\beta-\frac{8\pi}{3}\right)+\\ \sin(\beta-\alpha)+\sin(\beta-\alpha)+\\ \sin(\beta-\alpha)\end{pmatrix}\end{bmatrix} \quad (A3.1.5)$$

Equation A3.1.5 simplifies to the following:

$$\begin{aligned} v_a &= q*V_{im}*\sin(\beta-\alpha)\\ &= q*V_{im}*\sin\left(\omega_O.t\right) \quad (A3.1.6)\end{aligned}$$

Equation A3.1.6 well agree with the expression for output voltage va in the LHS of equation 3.1.4. This proves Venturini algorithm first method for three phase sine wave input and output voltages.

A3.2 APPENDIX: Case A**:** Consider the three phase input and output voltages as defined in equations 3.9 and 3.11. The nine modulation functions are defined in equation 3.17, using which the modulation functions for the three bidirectional switches between input phase A and output phase a can be expressed as follows:

$$\begin{aligned} M_{Aa} &= \frac{1}{3}+\frac{2}{3.V_{im}^2}*\left[V_{im}*\cos\left(\omega_i.t\right)*q*V_{im}*\cos\left(\omega_O.t\right)\right]\\ &= \frac{1}{3}+\frac{2}{3}*\left[q*\cos\left(\omega_i.t\right)*\cos\left(\omega_O.t\right)\right] \quad (A3.2.1)\end{aligned}$$

Similarly modulation functions M_{Ba} and M_{Ca} can be expressed as follows:

$$M_{Ba} = \frac{1}{3} + \frac{2}{3} * \left[q * cos\left(\omega_i .t - \frac{2\pi}{3} \right) * cos\left(\omega_O .t \right) \right] \quad (A3.2.2)$$

$$M_{Ca} = \frac{1}{3} + \frac{2}{3} * \left[q * cos\left(\omega_i .t - \frac{4\pi}{3} \right) * cos\left(\omega_O .t \right) \right] \quad (A3.2.3)$$

Output voltage for phase a can be expressed as follows:

$$v_a = q * V_{im} * cos\left(\omega_O .t \right) = M_{Aa} * v_A + M_{Ba} * v_B + M_{Ca} * v_C \quad (A3.2.4)$$

Using equations 3.9 and A3.2.1 to A3.2.3 in equation A3.2.4 and letting $\omega_i.t = \theta$, the RHS of equation A3.2.4 reduces to the following:

$$v_a = \underbrace{\frac{V_{im}}{3} * \left[cos(\theta) + cos\left(\theta - \frac{2\pi}{3} \right) + cos\left(\theta - \frac{4\pi}{3} \right) \right]}_{Term\ \ 1} + \underbrace{\frac{2}{3} * V_{im} * q * cos\left(\omega_O .t \right) * \left[cos^2(\theta) + cos^2\left(\theta - \frac{2\pi}{3} \right) + cos^2\left(\theta - \frac{4\pi}{3} \right) \right]}_{Term\ \ 2} \quad (A3.2.5)$$

The term 1 in equation A3.2.5 reduces to zero. Noting that $\cos^2(\theta)$ is [0.5 + 0.5*cos(2θ)] and using this in term 2 of equation A3.2.5, we have the following:

$$v_a = \frac{2}{3} * V_{im} * q * cos\left(\omega_O .t \right) * \left[\frac{3}{2} + cos(2\theta) + cos\left(2\theta - \frac{4\pi}{3} \right) + cos\left(2\theta - \frac{8\pi}{3} \right) \right]$$

$$= q * V_{im} * cos\left(\omega_O .t \right) \quad (A3.2.6)$$

Equation A3.2.6. well agree with the LHS of equation A3.2.4. This proves Venturini algorithm with three phase cosine wave input and output voltages and with unity input phase displacement factor.

Case B: Now consider the three phase input and output voltages defined in equation 3.9 and 3.11 all made to phase lag by 90 degrees so that they are now three phase sine wave input and output voltages at the respective frequencies. The nine modulation functions are defined in equation 3.17, using which the modulation functions for the three bidirectional switches between input phase A and output phase a can be expressed as follows:

$$M_{Aa} = \frac{1}{3} + \frac{2}{3.V_{im}^2} * \left[V_{im} * sin\left(\omega_i .t \right) * q * V_{im} * sin\left(\omega_o .t \right) \right]$$

$$= \frac{1}{3} + \frac{2}{3} * \left[q * sin\left(\omega_i .t \right) * sin\left(\omega_O .t \right) \right] \quad (A3.2.7)$$

Similarly modulation functions M_{Ba} and M_{Ca} can be expressed as follows:

$$M_{Ba} = \frac{1}{3} + \frac{2}{3} * \left[q * \sin\left(\omega_i .t - \frac{2\pi}{3} \right) * \sin(\omega_O .t) \right] \quad (A3.2.8)$$

$$M_{Ca} = \frac{1}{3} + \frac{2}{3} * \left[q * \sin\left(\omega_i .t - \frac{4\pi}{3} \right) * \sin(\omega_O .t) \right] \quad (A3.2.9)$$

Output voltage for phase a can be expressed as follows:

$$v_a = q * V_{im} * \sin(\omega_O .t) = M_{Aa} * v_A + M_{Ba} * v_B + M_{Ca} * v_C \quad (A3.2.10)$$

Using equations A3.2.7 to A3.2.9 and the newly defined three phase sine wave input voltages in equation A3.2.10, and letting $\omega_i.t = \theta$, the RHS of equation A3.2.10 reduces to the following:

$$v_a = \underbrace{\frac{V_{im}}{3} * \left[\sin(\theta) + \sin\left(\theta - \frac{2\pi}{3} \right) + \sin\left(\theta - \frac{4\pi}{3} \right) \right]}_{Term\ \ 1} + \underbrace{\frac{2}{3} * V_{im} * q * \sin(\omega_O .t) * \left[\sin^2(\theta) + \sin^2\left(\theta - \frac{2\pi}{3} \right) + \sin^2\left(\theta - \frac{4\pi}{3} \right) \right]}_{Term\ \ 2} \quad (A3.2.11)$$

The term 1 in equation A3.2.11 reduces to zero. Noting that $\sin^2(\theta)$ is [0.5 - 0.5*cos(2θ)] and using this in term 2 of equation A3.2.11, we have the following:

$$v_a = \frac{2}{3} * V_{im} * q * \sin\left(\omega_O .t \right) * \left[\frac{3}{2} - \cos(2\theta) - \cos\left(2\theta - \frac{4\pi}{3} \right) - \cos\left(2\theta - \frac{8\pi}{3} \right) \right]$$

$$= q * V_{im} * \sin\left(\omega_O .t \right) \quad (A3.2.12)$$

Equation A3.2.12. well agree with the LHS of equation A3.2.10. This proves Venturini algorithm with three phase sine wave input and output voltages and with unity input phase displacement factor.

Chapter IV

Modelling of Three Phase Matrix Converters Using Advanced Modulation Algorithms

4.1 INTRODUCTION: Although Venturini and Optimum Venturini algorithm form the fundamental method used for switching three phase Matrix Converters (MC), recently new algorithms have been proposed for switching MC. These include the algorithm proposed by Sunter-Clare [11-12] and the one proposed by Ned Mohan [13-14, 16-17]. This chapter examines the performance of MC in detail when switching is carried out using these two new algorithms.

4.2 SUNTER-CLARE MODULATION ALGORITHM: The Venturini modulation algorithm is suitable for synchronous operation of the input with the output [11-12]. This approach is unsuitable for closed loop applications where it is required to calculate the duty cycle every sampling period to achieve voltage control in which output frequency is continuously varying with time [11-12]. To overcome this problem the approach taken is to measure the input voltage at every sampling period and to determine voltage vector magnitude and ratio and position directly [11-12]. A simplified version of Venturini algorithm is defined in terms of the three phase input and output voltages at each sampling instant [11-12]. This allows the demand voltage ratio, output voltage magnitude and angle to be updated at every sampling period which is a requirement for closed loop control [11-12].

For the real time implementation of the proposed modulation algorithm, it is required to measure any two of three line to line input voltages. Then V_{im} and $\omega_i.t$ are calculated as give below [11-12].

$$V_{im}^2 = \frac{4}{9}.\left[v_{AB}^2 + v_{BC}^2 + v_{AB}.v_{BC} \right] \quad (4.1)$$

$$\omega_i.t = \arctan\left(\frac{V_{BC}}{\sqrt{3}.\left(\frac{2.V_{AB}}{3} + \frac{V_{BC}}{3} \right)} \right) \quad (4.2)$$

where v_{AB}, v_{BC} are the input line voltages.

The target output peak voltage and position are calculated as follows:

$$V_{om}^2 = \frac{2}{3}.\left[V_a^2 + V_b^2 + V_c^2 \right] \quad (4.3)$$

$$\omega_o.t = \arctan\left(\frac{V_b - V_c}{\sqrt{3}.V_a} \right) \quad (4.4)$$

where V_a, V_b and V_c are the target phase output voltages. In a closed loop system such as a field oriented or a vector controlled drive system, the voltage magnitude and angle may be direct outputs of the control loop. Then the voltage ratio is calculated as follows:

$$q = \sqrt{\frac{V_{om}^2}{V_{im}^2}} \quad (4.5)$$

where q is the desired voltage ratio and V_{im} is the peak input voltage. The triple harmonic terms are found using the following equations.

$$K_{31} = \frac{2q}{9q_m}.\sin(\omega_i.t).\sin(3\omega_i.t) \quad (4.6)$$

$$K_{32} = \frac{2q}{9q_m}.\sin\left(\omega_i.t - \frac{2\pi}{3}\right).\sin(3\omega_i.t) \quad (4.7)$$

$$K_{33} = -\sqrt{V_{om}^2}.\left[\frac{1}{6}.\cos(3\omega_o.t) - \frac{1}{4.q_m}.\cos(3\omega_i.t)\right] \quad (4.8)$$

where q_m is the maximum voltage transfer ratio which is 0.866. Then the three modulation functions for output phase a are given as follows:

$$M_{Aa} = \frac{1}{3} + k_{31} + \frac{2}{3.V_{im}^2}.(v_a + k_{33}).\left(\frac{2.v_{AB}}{3} + \frac{v_{BC}}{3}\right) \quad (4.9)$$

$$M_{Ba} = \frac{1}{3} + k_{32} + \frac{2}{3.V_{im}^2}.(v_a + k_{33}).\left(\frac{v_{BC}}{3} - \frac{v_{AB}}{3}\right) \quad (4.10)$$

$$M_{Ca} = 1 - (M_{Aa} + M_{Ba}) \quad (4.11)$$

$$M_{Ab} = \frac{1}{3} + k_{31} + \frac{2}{3.V_{im}^2}.(v_b + k_{33}).\left(\frac{2.v_{AB}}{3} + \frac{v_{BC}}{3}\right) \quad (4.12)$$

$$M_{Bb} = \frac{1}{3} + k_{32} + \frac{2}{3.V_{im}^2}.(v_b + k_{33}).\left(\frac{v_{BC}}{3} - \frac{v_{AB}}{3}\right) \quad (4.13)$$

$$M_{Cb} = 1 - (M_{Ab} + M_{Bb}) \quad (4.14)$$

$$M_{Ac} = \frac{1}{3} + k_{31} + \frac{2}{3.V_{im}^2}.(v_c + k_{33}).\left(\frac{2.v_{AB}}{3} + \frac{v_{BC}}{3}\right) \quad (4.15)$$

$$M_{Bc} = \frac{1}{3} + k_{32} + \frac{2}{3.V_{im}^2}.(v_c + k_{33}).\left(\frac{v_{BC}}{3} - \frac{v_{AB}}{3}\right) \quad (4.16)$$

$$M_{Cc} = 1 - (M_{Ac} + M_{Bc}) \quad (4.17)$$

The modulation functions have third harmonic components at the input and output frequencies added to them to produce output voltage V_o. This is a requirement for getting maximum possible voltage ratio. The three phase output voltages and input currents can be defined in terms of modulation functions as in equation 3.6 and 3.7 with constraint as in equation 3.8 given in Chapter III.

4.2.1 MODEL DEVELOPMENT: To study the behaviour of the three phase AC to three phase AC Matrix converter using Sunter-Clare Modulation algorithm, a model of this MC is developed in SIMULINK [51]. The data shown in Table 3.1 in Chapter III are used to develop the model.

4.2.2 MODEL OF A MATRIX CONVERTER USING SUNTER-CLARE ALGORITHM: A model of the Three Phase AC to three phase AC Matrix converter using the above Sunter-Clare algorithm developed in SIMULINK is shown in Fig. 4.1. In this case three phase sine wave input and output phase voltages with peak values Vim and q*Vim having frequency ωi and ωo rad/sec respectively are used. The three phase sine wave input and output voltages along with equations 4.1 to 4.17 are calculated using an Embedded MATLAB Function. The nine modulation functions derived from equations 4.9 to 4.17 are compared with a saw-tooth carrier generator vsaw and the nine gate pulse are derived in Embedded MATLAB Function using the following source code:

```
if (MAa >= vsaw)
   tAa = 1;
else
   tAa = 0;
end
if ((MAa + MBa) >= vsaw)
```

```
   tABa = 1;
else
   tABa = 0;
end
tBa = (tAa & ~(tABa) | tABa & ~tAa);
tCa = ~(tABa);
if (MAb >= vsaw)
   tAb = 1;
else
   tAb = 0;
end
if ((MAb + MBb) >= vsaw)
   tBAb = 1;
else
   tBAb = 0;
end
tBb = (tAb & ~(tBAb) | tBAb & ~tAb);
tCb = ~(tBAb);
if (MAc >= vsaw)
   tAc = 1;
else
   tAc = 0;
end
if ((MAc + MBc) >= vsaw)
   tBAc = 1;
else
   tBAc = 0;
end
tBc = (tAc & ~(tBAc) | tBAc & ~tAc);
tCc = ~(tBAc);
```

In the above source code, the symbols (>=), (&), (|) and (~) represent greater than or equal to, logic AND, OR and NOT operation respectively. The above source code can also be realized using integrated circuit Op.Amp. comparators, EXCUSIVE OR and NOT gates. The above source code is an alternative method and performs the same function as that give in section 3.3.1 of Chapter III. The three phase AC Voltage source, nine IGBT switches of the MC, R-L load etc. are the same as that given in Fig. 3.2 of Chapter III.

4.2.3 SIMULATION RESULTS: The simulation of the model shown in Fig. 4.1 was carried out using SIMULINK [51]. The ode15s(stiff/NDF) solver is used. The simulation results for the harmonic spectrum of line to neutral output voltage, input current and line to line output voltage are shown in Fig. 4.1 to 4.3 respectively. Simulation results for the line to neutral output voltage, input current, line to line output voltage, load current are shown in Fig. 4.5 to 4.8. The 2 kHZ saw-tooth carrier and gate pulse pattern are the same as in Section 3.3.2 of Chapter III. Simulation results are tabulated in Table 4.1 below:

TABLE 4.1: Model Simulation Results 1

Sl.No.	Algorithm	THD of Line to Neutral Output Voltage (p.u.)	THD Line to Line Output Voltage (p.u.)	THD of Input Current (p.u.)
1	Sunter-Clare	1.715	1.303	2.46

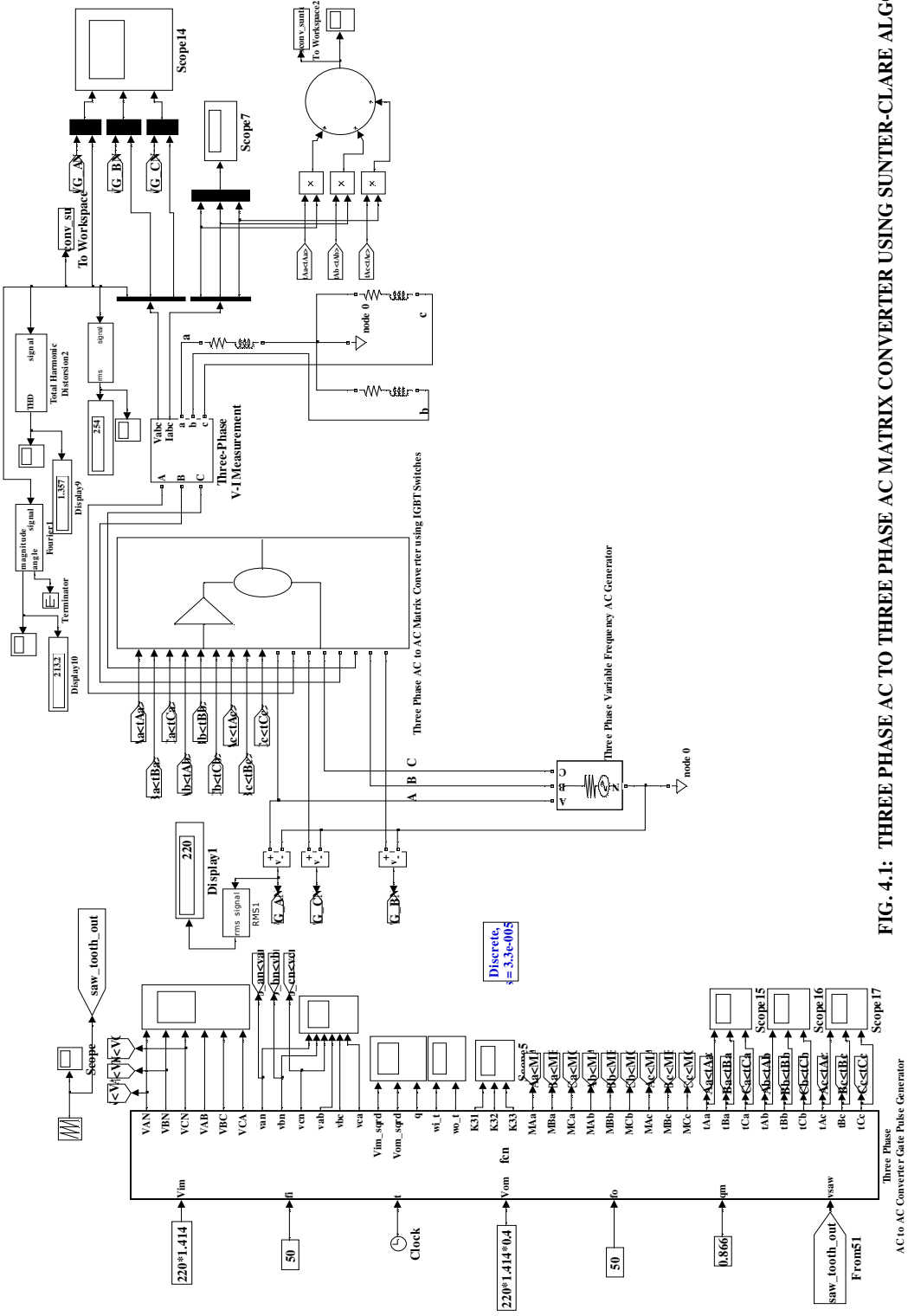


FIG. 4.1: THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING SUNTER-CLARE ALGORITHM

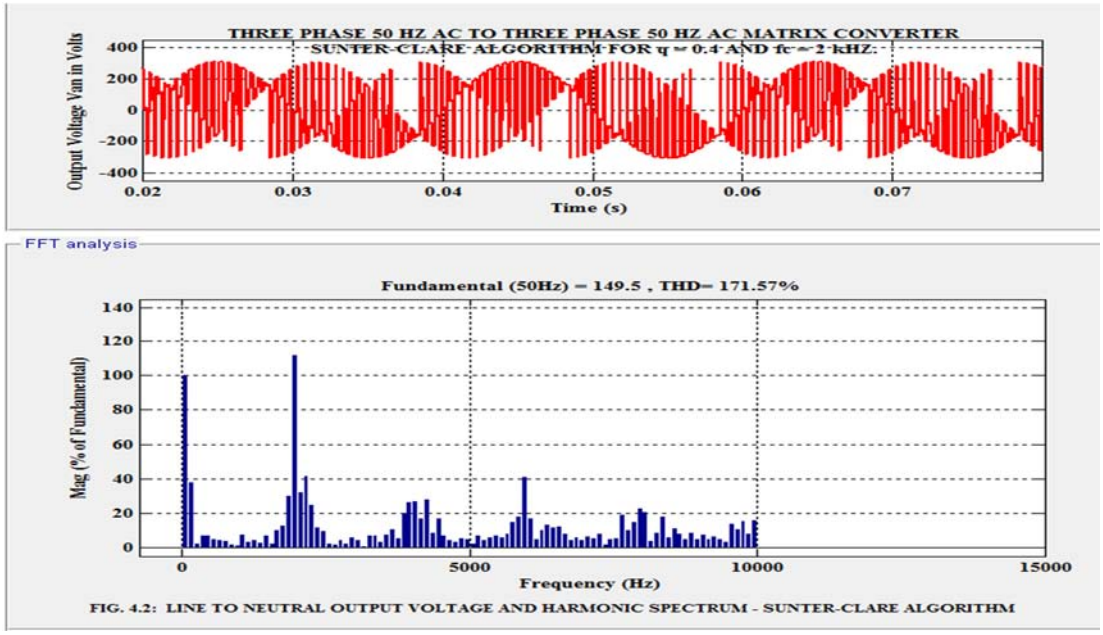


FIG. 4.2: LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM - SUNTER-CLARE ALGORITHM

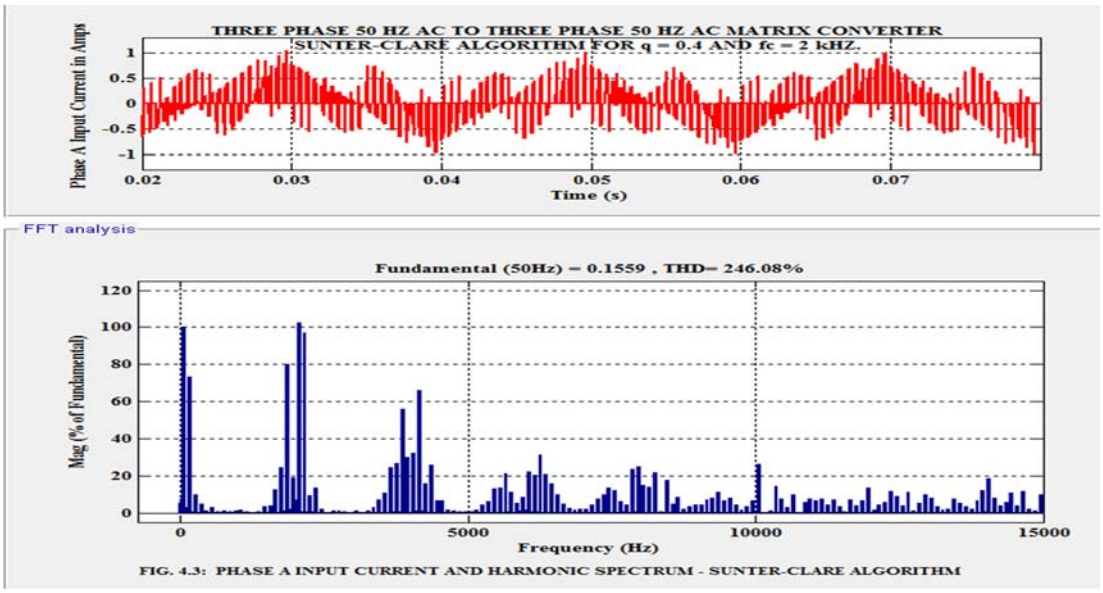


FIG. 4.3: PHASE A INPUT CURRENT AND HARMONIC SPECTRUM - SUNTER-CLARE ALGORITHM

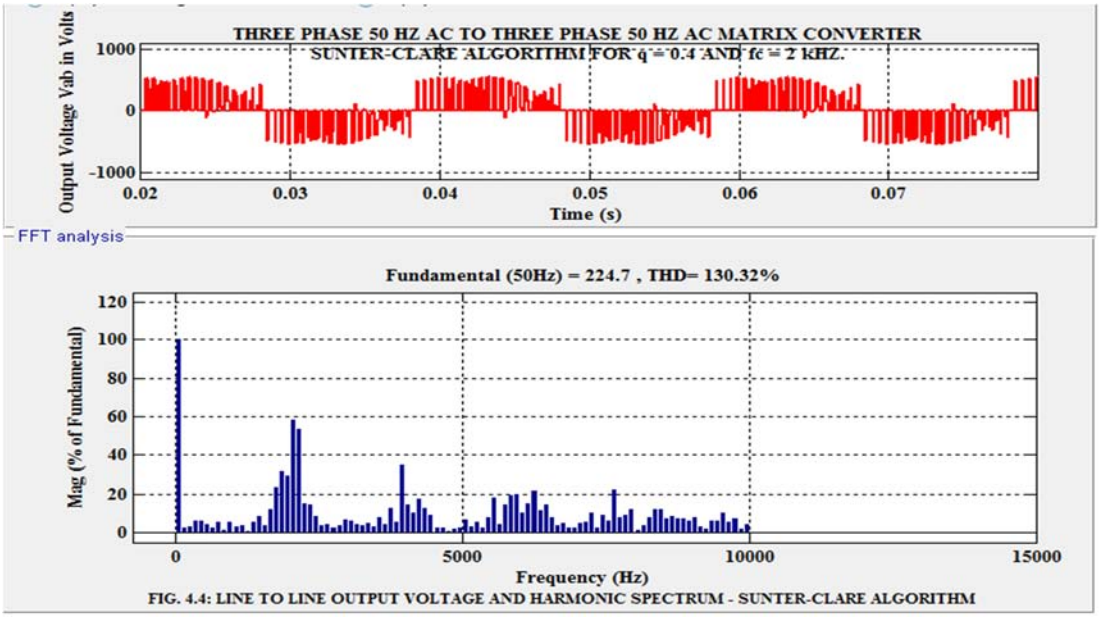


FIG. 4.4: LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM - SUNTER-CLARE ALGORITHM

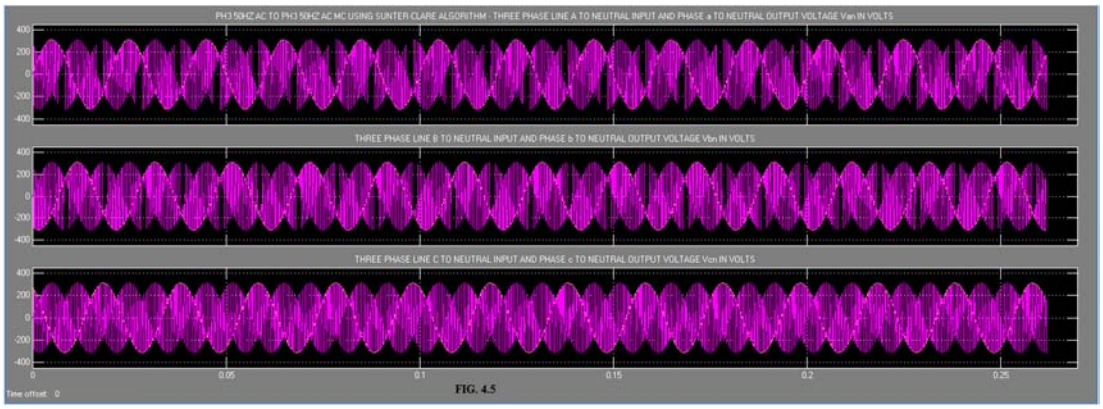


FIG. 4.5

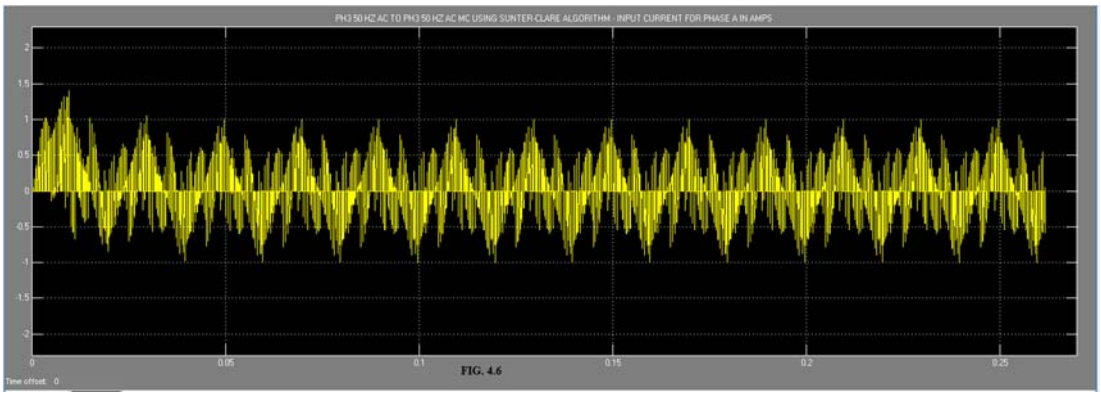


FIG. 4.6

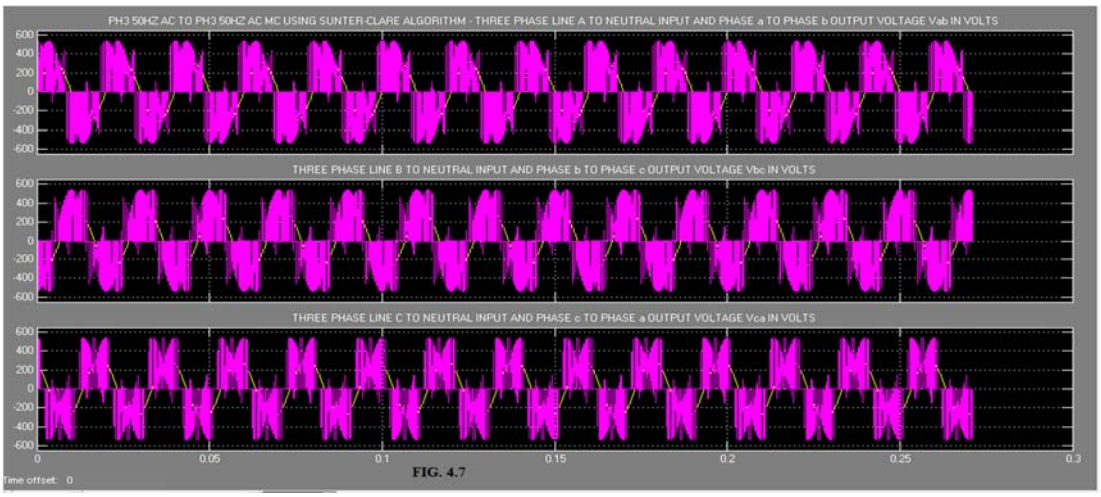


FIG. 4.7

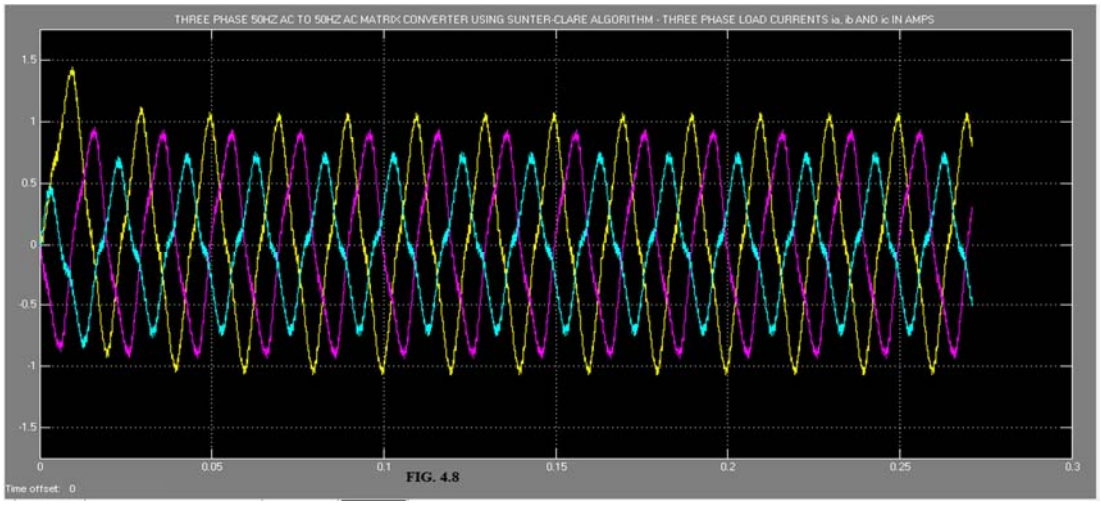


FIG. 4.8

4.3 NED MOHAN MODULATION ALGORITHM USING THREE PHASE COSINE WAVE INPUT VOLTAGES: A novel carrier-based modulation scheme is proposed by Ned Mohan et.al. which requires no sector information and look-up table to calculate duty ratios, with output voltage amplitude 0.866 times that of the input voltage and the input power factor controllable [13-14, 16-17]. This algorithm is briefly explained below:

Let the three phase input voltages, $v_i = [v_A \quad v_B \quad v_C]^T$ be defined as in equation 3.9 and the corresponding output phase voltages be defined as in equation 3.6 given in Chapter III. The duty ratios be chosen such that the output voltages are independent of the input frequency. This is possible by considering the input voltages in stationary reference frame and the output voltages in synchronous reference frame. Hence M_{Aa}, M_{Ba} and M_{Ca} are chosen as given in equation 4.18 below:

$$\begin{bmatrix} M_{Aa} \\ M_{Ba} \\ M_{Ca} \end{bmatrix} = \begin{bmatrix} k_a * \cos(\omega_i t - \varphi_i) \\ k_a * \cos\left(\omega_i t - \varphi_i - \frac{2\pi}{3}\right) \\ k_a * \cos\left(\omega_i t - \varphi_i - \frac{4\pi}{3}\right) \end{bmatrix} \qquad (4.18)$$

Using equation 3.6, 3.9 and 4.18 and simplifying, the output voltage equation v_a for phase a reduces to the following:

$$v_a = \frac{3}{2} * k_a . V_{im} . \cos(\varphi_i) \qquad (4.19)$$

Equation 4.19 shows that the output phase voltage v_a is independent of the input frequency but dependent only on the amplitude of the input voltage. Equation 4.19 is proved in A4.1 Appendix. The modulation index k_a is a function of the output frequency ω_o as defined below:

$$\begin{bmatrix} k_a \\ k_b \\ k_c \end{bmatrix} = \begin{bmatrix} k * \cos(\omega_o t) \\ k * \cos\left(\omega_o t - \frac{2\pi}{3}\right) \\ k * \cos\left(\omega_o t - \frac{4\pi}{3}\right) \end{bmatrix} \qquad (4.20)$$

Where k_a, k_b and k_c are the modulation indices for phase a, b and c respectively.

Using equations 4.19 and 4.20, the output phase voltage v_a simplifies to the following:

$$v_a = \left[\frac{3}{2} . k . V_{im} . \cos(\varphi_i) . \cos(\omega_o t)\right] \qquad (4.21)$$

From equation 4.18 and 4.20, it is clear that the duty-ratios of the switches takes negative values. But the requirement is that the duty ratios of the switches must lie in the range 0 to 1. This is made possible by adding offset duty ratios to the existing duty ratios. Thus absolute values of duty ratios are added. The offset duty ratio is defined by equation 4.22 below:

$$\begin{bmatrix} D_A(t) \\ D_B(t) \\ D_C(t) \end{bmatrix} = \begin{bmatrix} |k_a * \cos(\omega_i t - \varphi_i)| \\ \left|k_a * \cos\left(\omega_i t - \varphi_i - \frac{2\pi}{3}\right)\right| \\ \left|k_a * \cos\left(\omega_i t - \varphi_i - \frac{4\pi}{3}\right)\right| \end{bmatrix} \qquad (4.22)$$

Thus the new duty ratios are defined below:

$$\begin{bmatrix} M_{Aa} \\ M_{Ba} \\ M_{Ca} \end{bmatrix} = \begin{bmatrix} D_A(t) + k_a * \cos(\omega_i t - \varphi_i) \\ D_B(t) + k_a * \cos\left(\omega_i t - \varphi_i - \frac{2\pi}{3}\right) \\ D_C(t) + k_a * \cos\left(\omega_i t - \varphi_i - \frac{4\pi}{3}\right) \end{bmatrix} \quad (4.23)$$

Using equation 4.22 in 4.23, in order that the new duty ratio in 4.23 lies in the range 0 to 1, the following inequality should be satisfied:

$$0 < 2.|k_a| = 2.k < 1 \quad (4.24)$$

Thus the maximum value of k_a and k can be 0.5. Using this value, the offset duty ratios are chosen as given below:

$$\begin{bmatrix} D_A(t) \\ D_B(t) \\ D_C(t) \end{bmatrix} = \begin{bmatrix} |0.5 * \cos(\omega_i t - \varphi_i)| \\ \left|0.5 * \cos\left(\omega_i t - \varphi_i - \frac{2\pi}{3}\right)\right| \\ \left|0.5 * \cos\left(\omega_i t - \varphi_i - \frac{4\pi}{3}\right)\right| \end{bmatrix} \quad (4.25)$$

To utilize the input voltage capability to the full extend, additional common mode voltage term is added which gives the new modulation index as given below:

$$\begin{bmatrix} M_{Aa} \\ M_{Ba} \\ M_{Ca} \end{bmatrix} = \begin{bmatrix} D_A(t) + [k_a - \{max(k_a, k_b, k_c) + min(k_a, k_b, k_c)\}/2] * \cos(\omega_i t - \varphi_i) \\ D_B(t) + [k_a - \{max(k_a, k_b, k_c) + min(k_a, k_b, k_c)\}/2] * \cos\left(\omega_i t - \varphi_i - \frac{2\pi}{3}\right) \\ D_C(t) + [k_a - \{max(k_a, k_b, k_c) + min(k_a, k_b, k_c)\}/2] * \cos\left(\omega_i t - \varphi_i - \frac{4\pi}{3}\right) \end{bmatrix} \quad (4.26)$$

Similar calculations apply to the other two output phases b and c.

To calculate input power factor, the input current is represented as a function of duty ratios and output currents, as defined in equation 3.7 in Chapter III. Hence the input current in phase A can be expressed as follows:

$$i_A = (k_a.i_a + k_b.i_b + k_c.i_c) * \cos(\omega_i t - \varphi_i) \quad (4.27)$$

In equation 4.27, the modulation index and output currents are at output frequency. Equation 4.27 simplifies to the following:

$$i_A = \left(\frac{3}{2}.k.I_O.\cos(\varphi_O)\right) * \cos(\omega_i t - \varphi_i) \quad (4.28)$$

Where I_O is the amplitude of the output current and φ_O is the output power factor angle.

Comparing equation 4.28 with the input phase voltage v_A, it is seen that the input current lags the input phase voltage by an angle of φ_i. Thus φ_i is chosen to be zero for unity power factor operation. Also from equation 4.21, we have

$$q = \frac{3}{2} * k * \cos(\varphi_i) \quad (4.29)$$

The switching signals corresponding to output phase a are obtained by comparing M_{Aa} and (M_{Aa} + M_{Ba}) with a triangular carrier signal whose peak value is one and minimum value is zero. The resulting PWM signals are given to logic gates to obtain the switching pulses for the matrix converter.

4.3.1 MODEL DEVELOPMENT: A model of the three phase matrix converter using the above Ned Mohan algorithm was developed in SIMULINK [51]. The input power factor is unity. The value of modulation index k used is 0.26667 for a q value of 0.4 using equation 4.29. The triangle carrier has a peak value of one and a minimum value of zero. The values for the input voltage, input frequency, output frequency and triangle carrier frequency are the same as shown in Table 3.1 in Chapter III.

4.3.2 MODEL OF A MATRIX CONVERTER USING NED MOHAN ALGORITHM: The SIMULINK model of the MC using Ned Mohan algorithm for three phase cosine wave input voltages is shown in Fig. 4.9. The modulation index k, input frequency fi, output frequency fo, time t and input p.f. angle phi_i are given as inputs to calculate k_a, k_b, k_c and $D_A(t)$, $D_B(t)$ and $D_C(t)$ according to equations 4.20 and 4.25 using Embedded MATLAB function. The minimum and maximum values of the outputs k_a, k_b and k_c are calculated using two MinMax block in the Simulink block set. The two resulting outputs min_k_abc and max_k_abc together with the above calculated values for $D_A(t)$, $D_B(t)$ and $D_C(t)$ and the input phi_i are used to calculate the duty ratios of the switches according to equation 4.26 using the same Embedded MATLAB function.

A 2 kHz triangle carrier with a peak value and minimum value of one and zero volt is generated using a 2 kHz square pulse generator with 50 % duty cycle, a subtractor and an integrator with multiplication constant. The nine calculated values of the duty ratios for the switches and the 2 kHz triangle carrier are given as inputs to another Embedded MATLAB function to generate the gate switching pulses for the nine bidirectional switches. A method of generating the gate switching pulses using adders, comparators and logic gates is also shown in Fig. 4.9. The source code for generating the gate switching pulses is the same as given in section 4.2.2 above, except that the nine gate pulses tAa to tCc, tABa, tBAb and tBAc in this source code are replaced by qAa to qCc, qABa, qABb and qABc respectively. The three phase cosine wave generator, the nine IGBT bidirectional switch matrix, R-L load etc. are the same as explained in Section 3.3.1 of Chapter III.

4.3.3 SIMULATION RESULTS: The simulation of the model shown in Fig. 4.9 was carried out using SIMULINK [51]. The ode15s(stiff/NDF) solver is used. The simulation results for the harmonic spectrum of line to neutral output voltage, input current and line to line output voltage are shown in Fig. 4.10 to 4.12 respectively. Simulation results for the line to neutral output voltage, input current, line to line output voltage, load current are shown in Fig. 4.13 to 4.16. The 2 kHZ triangle carrier and gate pulse pattern are shown in Fig. 4.17 and 4.18 respectively. Simulation results for a modulation index k of 0.26667 and three phase cosine wave input voltage are tabulated in Table 4.2 below:

TABLE 4.2: Model Simulation Results 2

Sl.No.	Algorithm	THD of Line to Neutral Output Voltage (p.u.)	THD Line to Line Output Voltage (p.u.)	THD of Input Current (p.u.)
1	Ned Mohan	2.80	1.398	2.829

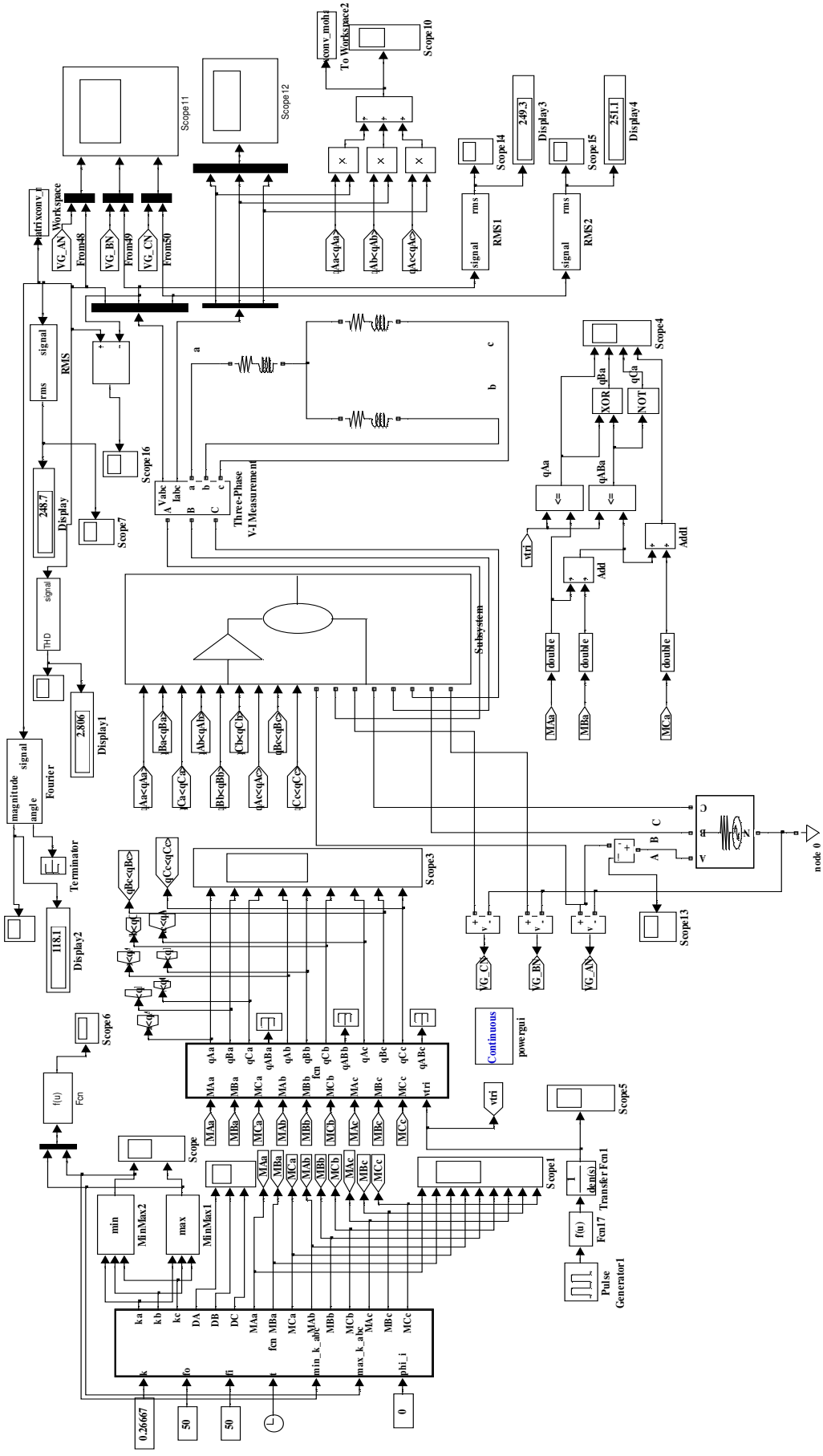


FIG. 4.9: MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING NED MOHAN ALGORITHM

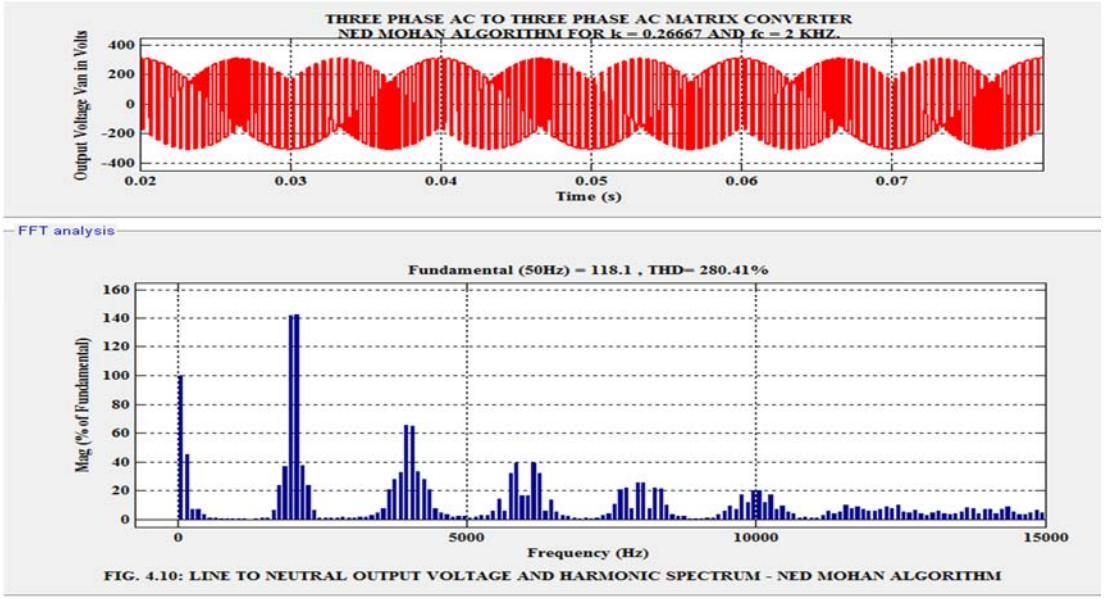
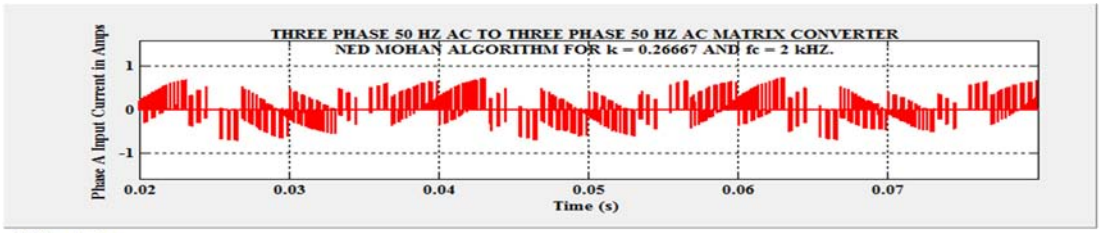


FIG. 4.10: LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM - NED MOHAN ALGORITHM



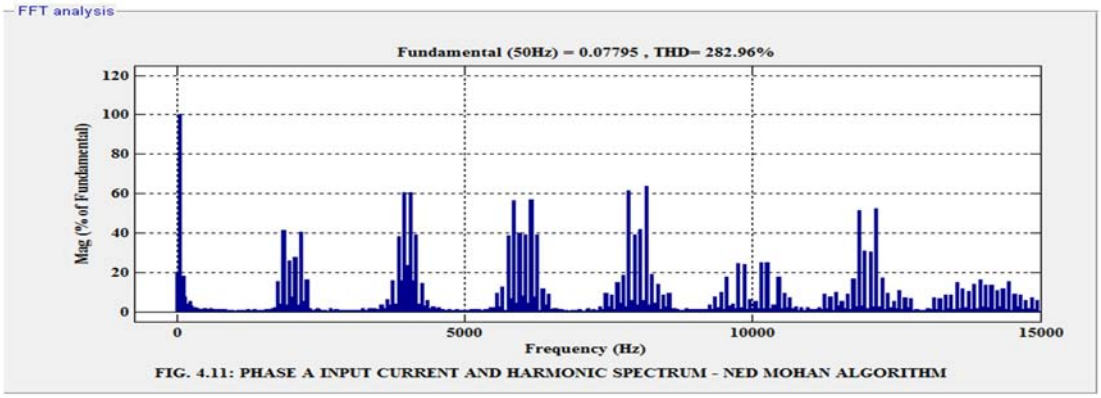
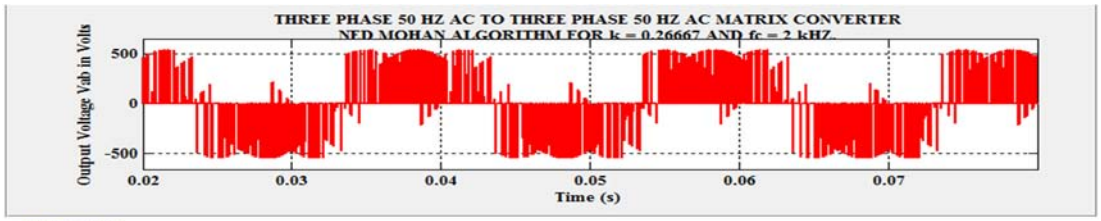


FIG. 4.11: PHASE A INPUT CURRENT AND HARMONIC SPECTRUM - NED MOHAN ALGORITHM



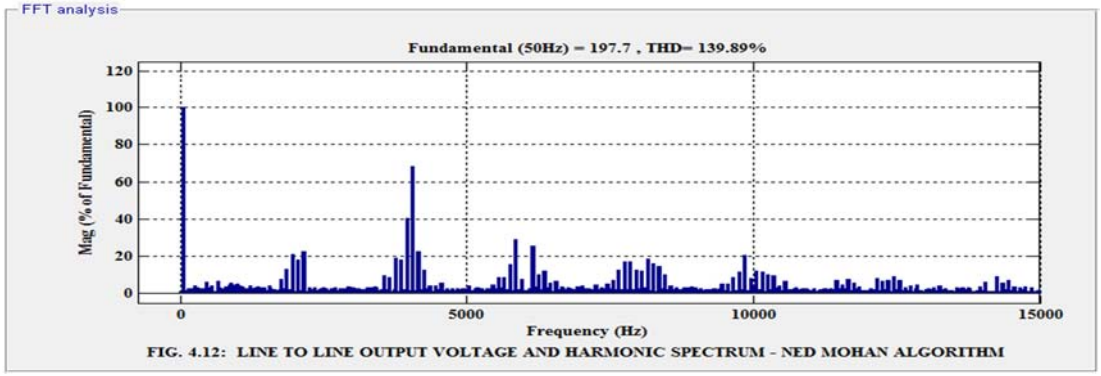


FIG. 4.12: LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM - NED MOHAN ALGORITHM

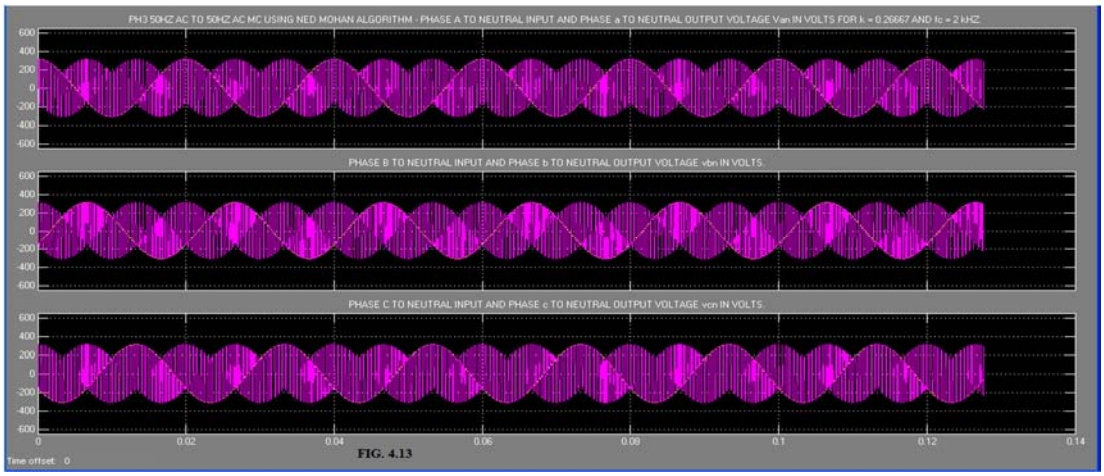


FIG. 4.13

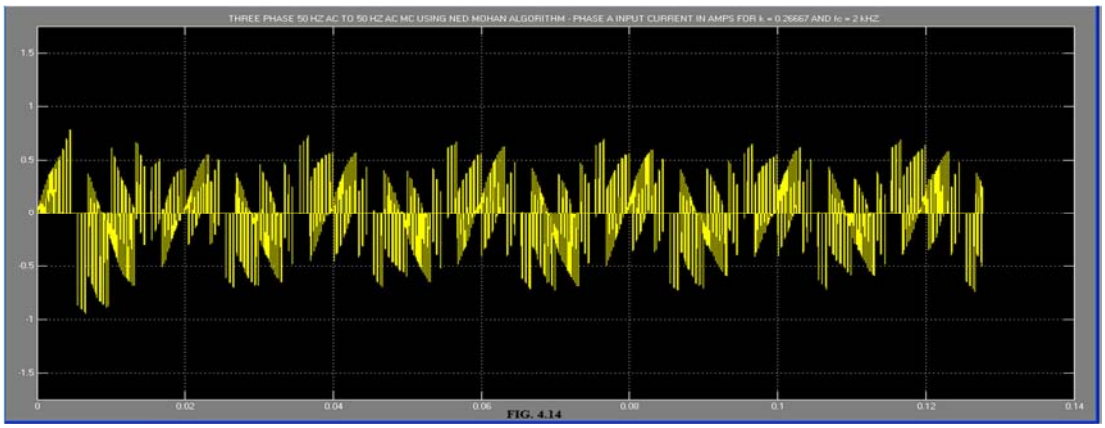


FIG. 4.14

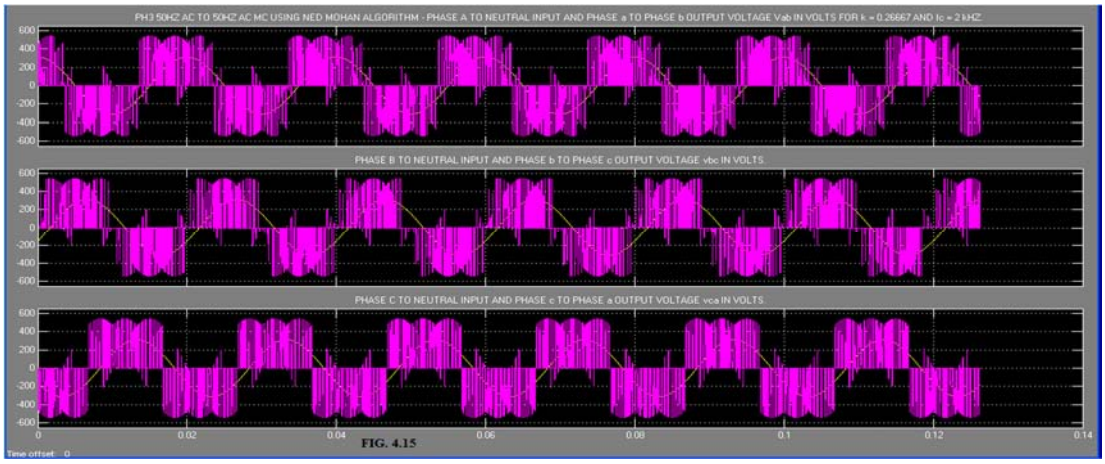


FIG. 4.15

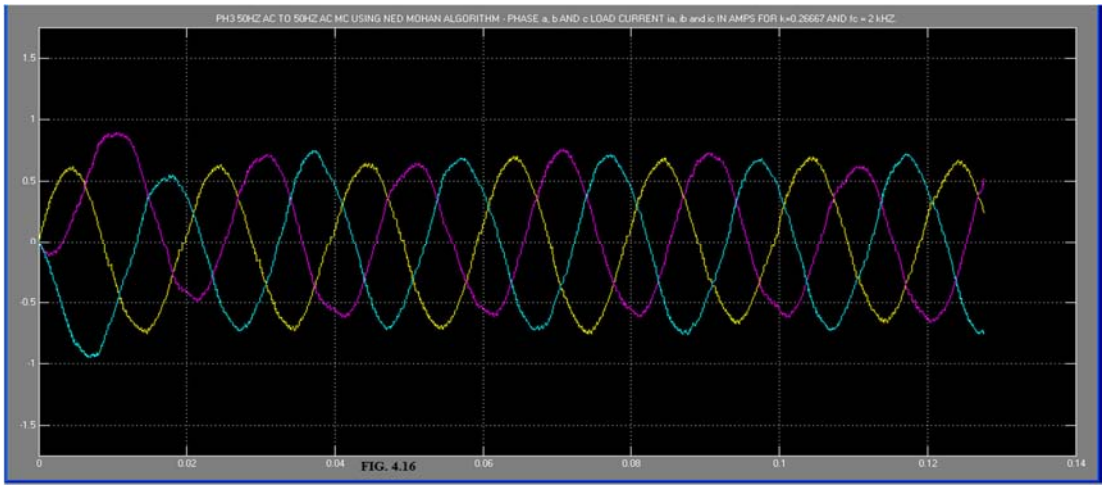


FIG. 4.16

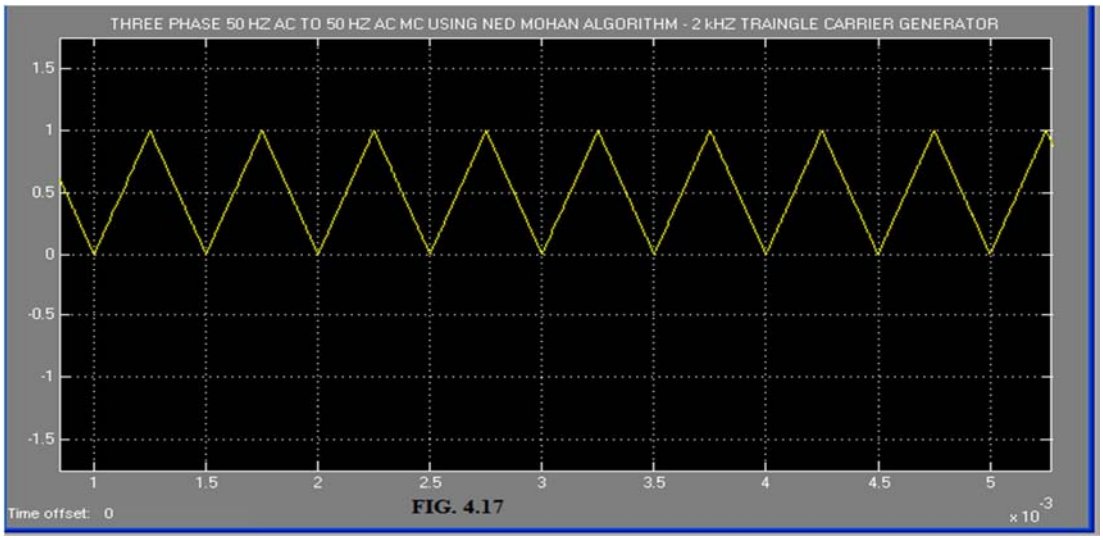


FIG. 4.17

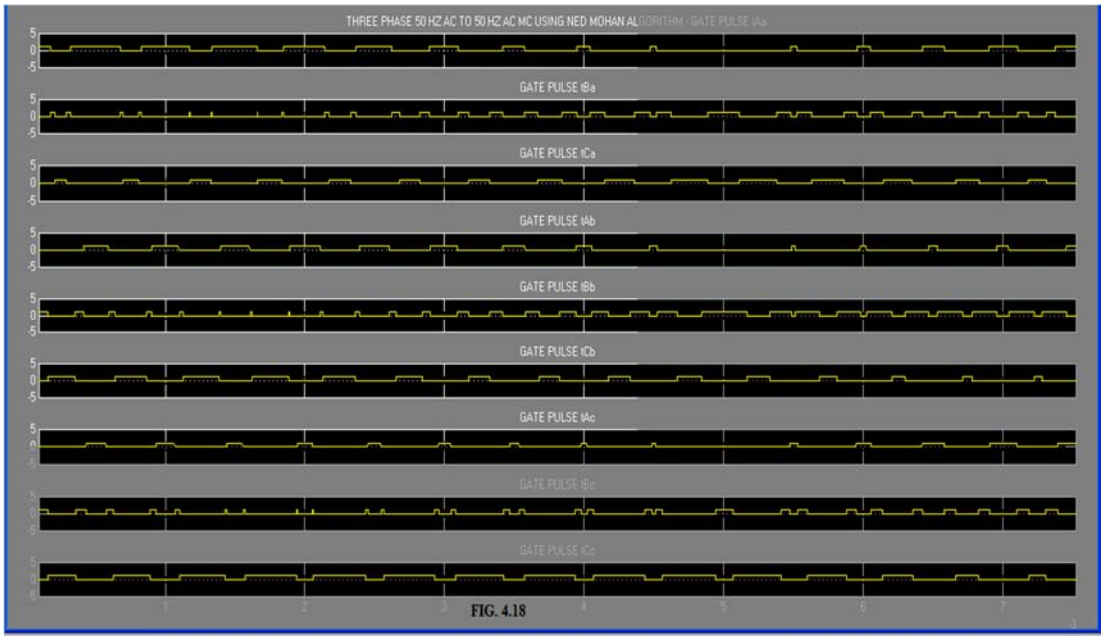


FIG. 4.18

4.4 NED MOHAN MODULATION ALGORITHM USING THREE PHASE SINE WAVE INPUT VOLTAGES: Let the three phase input voltages, $v_i = [v_A \quad v_B \quad v_C]^T$ be defined as in equation 4.30 and the corresponding output phase voltages $v_o = [v_a \quad v_b \quad v_c]^T$ be defined as in equation 4.31 given below:

$$vi = V_{im} * \begin{bmatrix} \sin(\omega_i t) \\ \sin(\omega_i t - \frac{2\pi}{3}) \\ \sin(\omega_i t - \frac{4\pi}{3}) \end{bmatrix} \quad (4.30)$$

$$vo = q * V_{im} * \begin{bmatrix} \sin(\omega_o t + \varphi_o) \\ \sin(\omega_o t + \varphi_o - \frac{2\pi}{3}) \\ \sin(\omega_o t + \varphi_o - \frac{4\pi}{3}) \end{bmatrix} \quad (4.31)$$

The duty ratios be chosen such that the output voltages are independent of the input frequency. This is possible by considering the input voltages in stationary reference frame and the output voltages in synchronous reference frame. Hence M_{Aa}, M_{Ba} and M_{Ca} are chosen as given in equation 4.32 below:

$$\begin{bmatrix} M_{Aa} \\ M_{Ba} \\ M_{Ca} \end{bmatrix} = \begin{bmatrix} k_a * \sin(\omega_i t - \varphi_i) \\ k_a * \sin\left(\omega_i t - \varphi_i - \frac{2\pi}{3}\right) \\ k_a * \sin\left(\omega_i t - \varphi_i - \frac{4\pi}{3}\right) \end{bmatrix} \qquad (4.32)$$

Using equation 4.30, 4.31 and 4.32 and simplifying, the output voltage equation v_a for phase a reduces to the following:

$$v_a = \frac{3}{2} * k_a . V_{im} . \cos(\varphi_i) \qquad (4.33)$$

Equation 4.33 shows that the output phase voltage v_a is independent of the input frequency but dependent only on the amplitude of the input voltage. Equation 4.33 is proved in A4.1 Appendix. The modulation index k_a is a function of the output frequency ω_o as defined below:

$$\begin{bmatrix} k_a \\ k_b \\ k_c \end{bmatrix} = \begin{bmatrix} k * \sin(\omega_o t) \\ k * \sin\left(\omega_o t - \frac{2\pi}{3}\right) \\ k * \sin\left(\omega_o t - \frac{4\pi}{3}\right) \end{bmatrix} \qquad (4.34)$$

Where k_a, k_b and k_c are the modulation indices for phase a, b and c respectively.

Using equations 4.33 and 4.34, the output phase voltage v_a simplifies to the following:

$$v_a = \left[\frac{3}{2} . k . V_{im} . \cos(\varphi_i) . \sin(\omega_o t)\right] \qquad (4.35)$$

From equation 4.32 and 4.34, it is clear that the duty-ratios of the switches takes negative values. But the requirement is that the duty ratios of the switches must lie in the range 0 to 1. This is made possible by adding offset duty ratios to the existing duty ratios. Thus absolute values of duty ratios are added. The offset duty ratio is defined by equation 4.36 below:

$$\begin{bmatrix} D_A(t) \\ D_B(t) \\ D_C(t) \end{bmatrix} = \begin{bmatrix} |k_a * \sin(\omega_i t - \varphi_i)| \\ \left|k_a * \sin\left(\omega_i t - \varphi_i - \frac{2\pi}{3}\right)\right| \\ \left|k_a * \sin\left(\omega_i t - \varphi_i - \frac{4\pi}{3}\right)\right| \end{bmatrix} \qquad (4.36)$$

Thus the new duty ratios are defined below:

$$\begin{bmatrix} M_{Aa} \\ M_{Ba} \\ M_{Ca} \end{bmatrix} = \begin{bmatrix} D_A(t) + k_a * \sin(\omega_i t - \varphi_i) \\ D_B(t) + k_a * \sin\left(\omega_i t - \varphi_i - \frac{2\pi}{3}\right) \\ D_C(t) + k_a * \sin\left(\omega_i t - \varphi_i - \frac{4\pi}{3}\right) \end{bmatrix} \qquad (4.37)$$

Using equation 4.36 in 4.37, in order that the new duty ratio in 4.37 lies in the range 0 to 1, the following inequality should be satisfied:

$$0 < 2.|k_a| = 2.k < 1 \qquad (4.38)$$

Thus the maximum value of k_a and k can be 0.5. Using this value, the offset duty ratios are chosen as given below:

$$\begin{bmatrix} D_A(t) \\ D_B(t) \\ D_C(t) \end{bmatrix} = \begin{bmatrix} |0.5 * \sin(\omega_i t - \varphi_i)| \\ \left|0.5 * \sin\left(\omega_i t - \varphi_i - \frac{2\pi}{3}\right)\right| \\ \left|0.5 * \sin\left(\omega_i t - \varphi_i - \frac{4\pi}{3}\right)\right| \end{bmatrix} \quad (4.39)$$

To utilize the input voltage capability to the full extend, additional common mode voltage term is added which gives the new modulation index as given below:

$$\begin{bmatrix} M_{Aa} \\ M_{Ba} \\ M_{Ca} \end{bmatrix}$$

$$= \begin{bmatrix} D_A(t) + [k_a - \{max(k_a, k_b, k_c) + min(k_a, k_b, k_c)\}/2] * \sin(\omega_i t - \varphi_i) \\ D_B(t) + [k_a - \{max(k_a, k_b, k_c) + min(k_a, k_b, k_c)\}/2] * \sin\left(\omega_i t - \varphi_i - \frac{2\pi}{3}\right) \\ D_C(t) + [k_a - \{max(k_a, k_b, k_c) + min(k_a, k_b, k_c)\}/2] * \sin\left(\omega_i t - \varphi_i - \frac{4\pi}{3}\right) \end{bmatrix} \quad (4.40)$$

Similar calculations apply to the other two output phases b and c.

To calculate input power factor, the input current is represented as a function of duty ratios and output currents, as defined in equation 3.7 in Chapter III. Hence the input current in phase A can be expressed as follows:

$$i_A = (k_a . i_a + k_b . i_b + k_c . i_c) * \sin(\omega_i t - \varphi_i) \quad (4.41)$$

In equation 4.27, the modulation index and output currents are at output frequency. Equation 4.27 simplifies to the following:

$$i_A = \left(\frac{3}{2} . k . I_O . \cos(\varphi_O)\right) * \sin(\omega_i t - \varphi_i) \quad (4.42)$$

Where I_O is the amplitude of the output current and φ_O is the output power factor angle.

Comparing equation 4.42 with the input phase voltage v_A, it is seen that the input current lags the input phase voltage by an angle of φ_i. Thus φ_i is chosen to be zero for unity power factor operation. Also from equation 4.35, we have

$$q = \frac{3}{2} * k * \cos(\varphi_i) \quad (4.43)$$

The switching signals corresponding to output phase a are obtained by comparing M_{Aa} and (M_{Aa} + M_{Ba}) with a triangular carrier signal whose peak value is one and minimum value is zero. The resulting PWM signals are given to logic gates to obtain the switching pulses for the matrix converter.

4.4.1 MODEL DEVELOPMENT: A model of the three phase matrix converter using the above Ned Mohan algorithm for three phase sine wave input is developed in SIMULINK [51]. The input power factor is unity. The value of modulation index k used is 0.26667 for a q value of 0.4 using equation 4.43. The triangle carrier has a peak value of one and a minimum value of zero. The values for the input voltage, input frequency, output frequency and triangle carrier frequency are the same as shown in Table 3.1 in Chapter III.

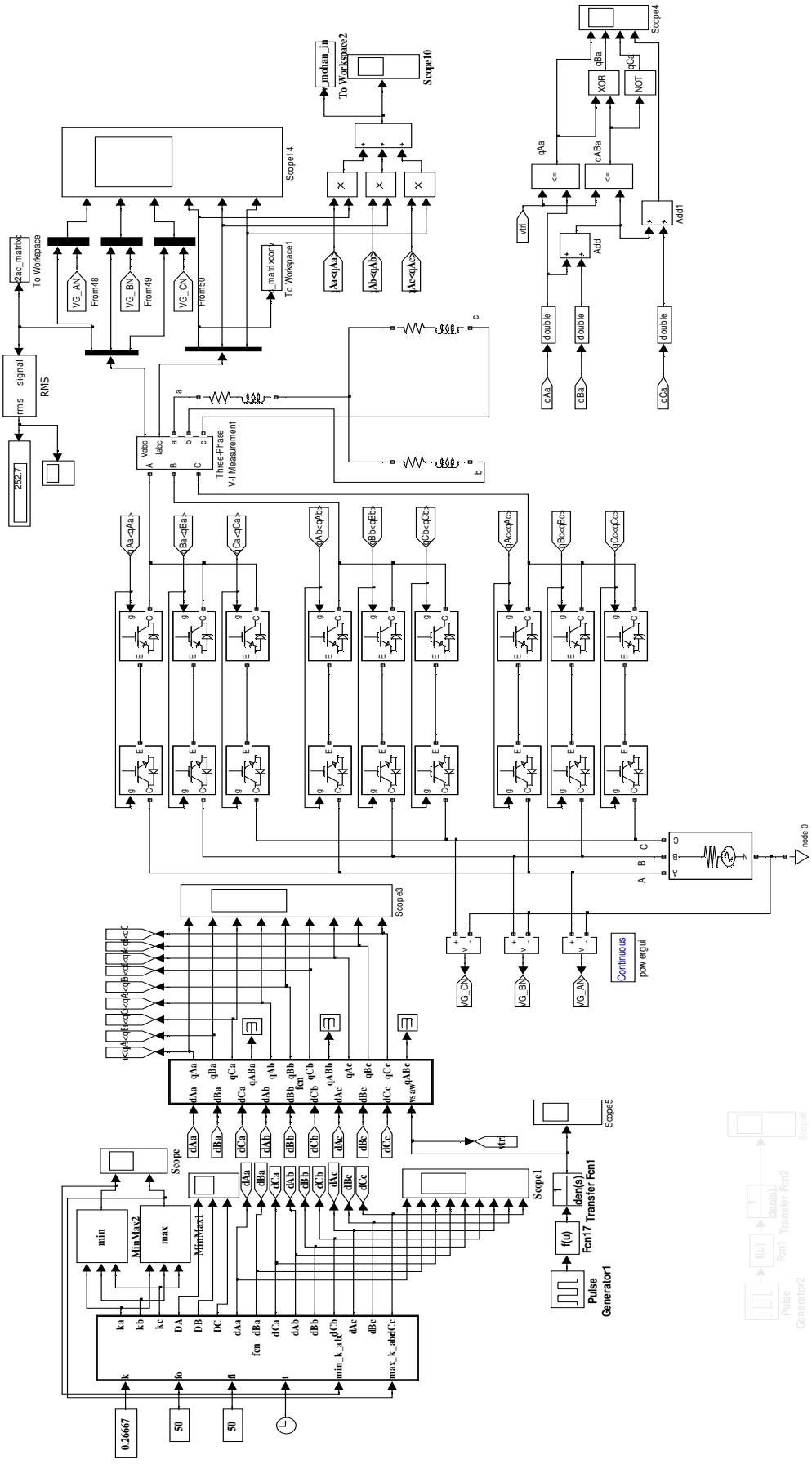


FIG. 4.19: MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER WITH THREE PHASE SINE WAVE VOLTAGE INPUT USING NED MOHAN ALGORITHM

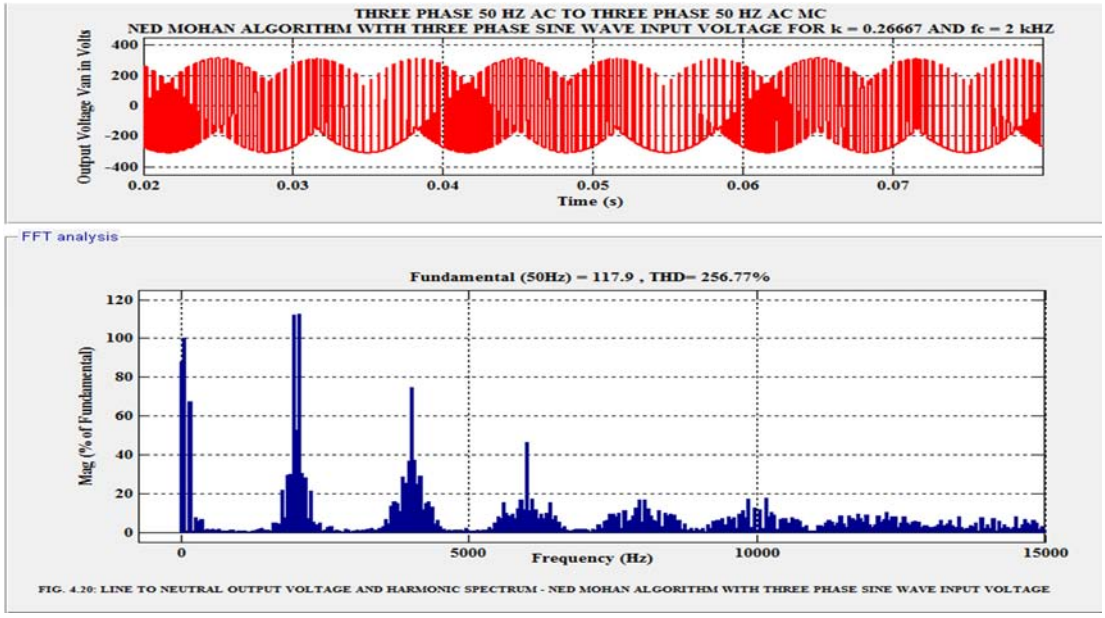


FIG. 4.20: LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM - NED MOHAN ALGORITHM WITH THREE PHASE SINE WAVE INPUT VOLTAGE

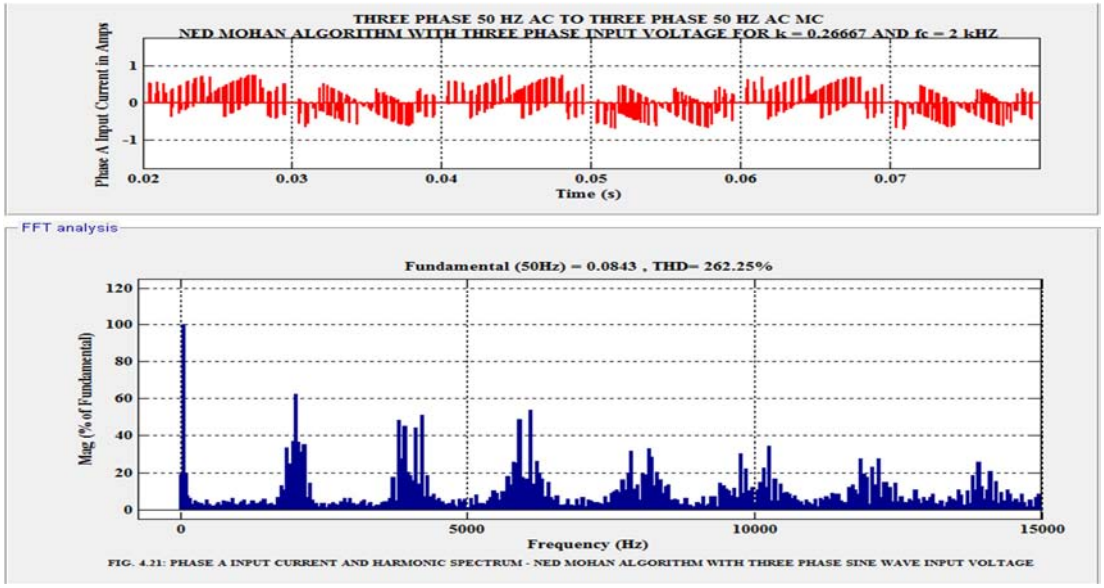


FIG. 4.21: PHASE A INPUT CURRENT AND HARMONIC SPECTRUM - NED MOHAN ALGORITHM WITH THREE PHASE SINE WAVE INPUT VOLTAGE

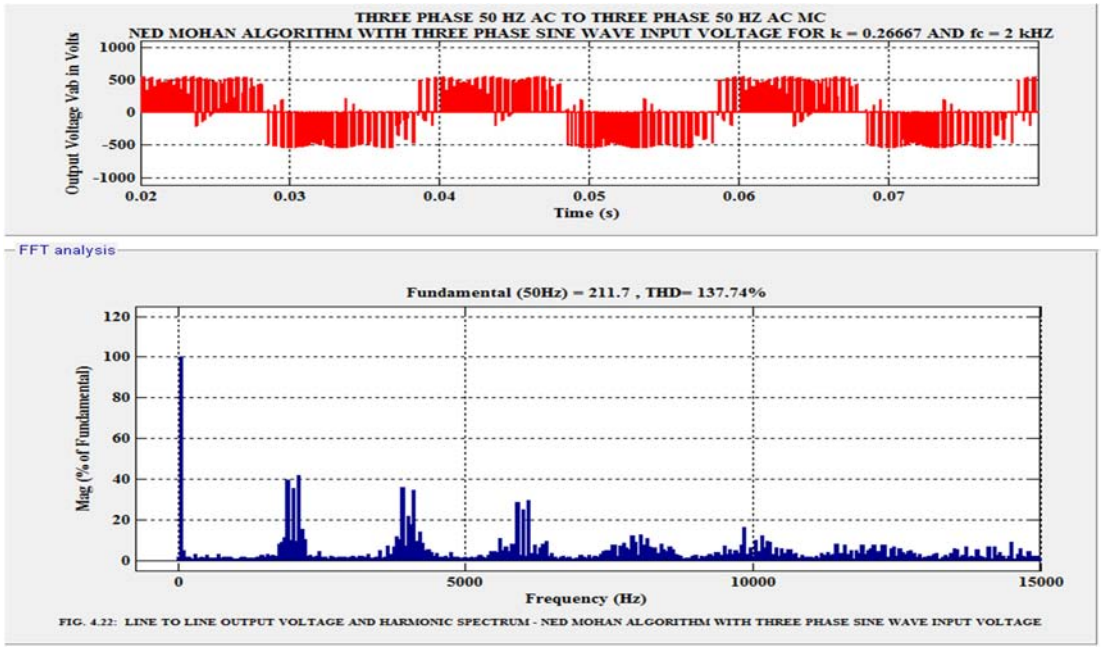


FIG. 4.22: LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM - NED MOHAN ALGORITHM WITH THREE PHASE SINE WAVE INPUT VOLTAGE

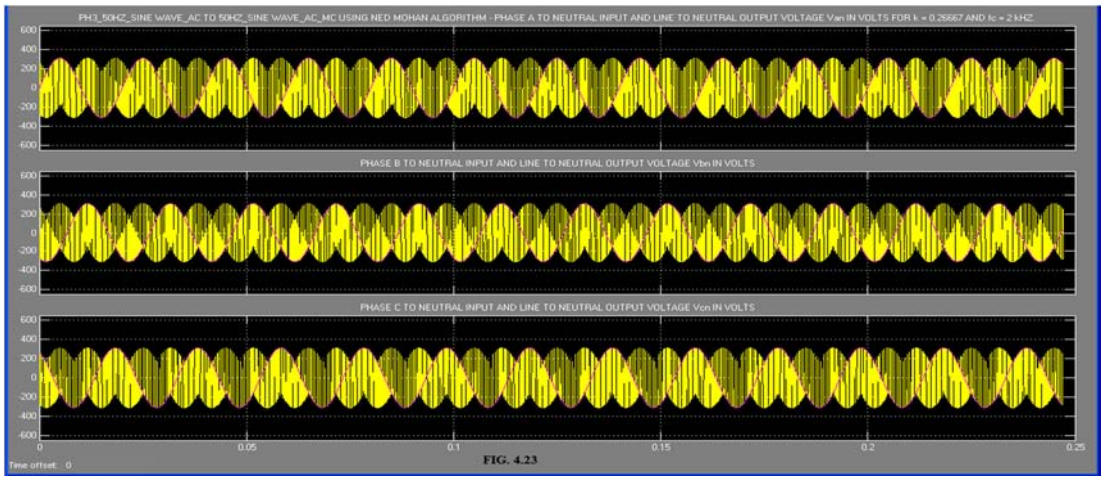


FIG. 4.23

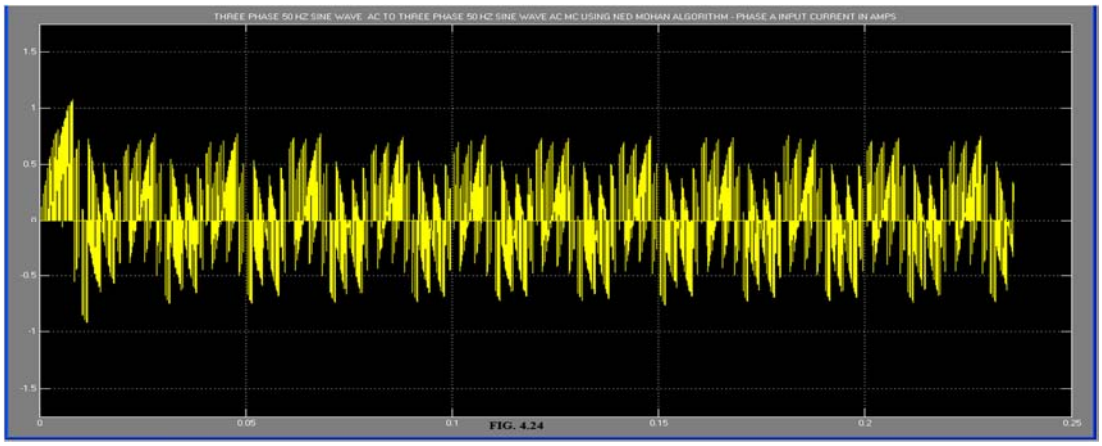


FIG. 4.24

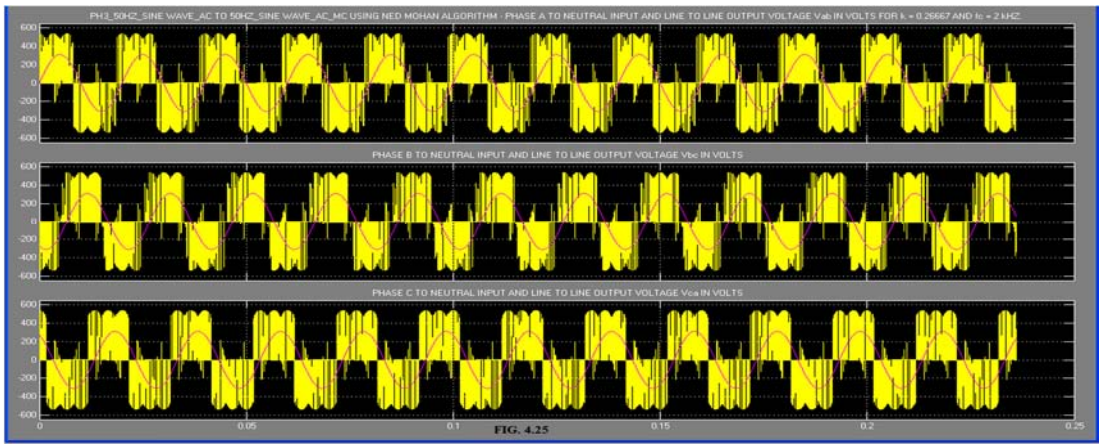


FIG. 4.25

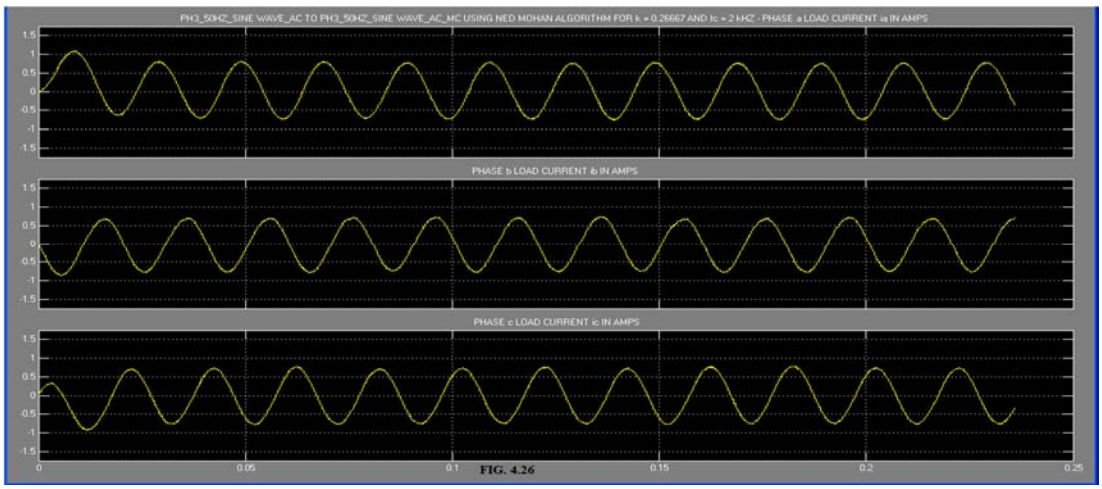


FIG. 4.26

4.4.2 MODEL OF A MATRIX CONVERTER USING NED MOHAN ALGORITHM: The SIMULINK model of the MC using Ned Mohan algorithm for three phase sine wave input voltages is shown in Fig. 4.19. The modulation index k, input frequency fi, output frequency fo, time t and input p.f. angle phi_i are given as inputs to calculate k_a, k_b, k_c and $D_A(t)$, $D_B(t)$ and $D_C(t)$ according to equations 4.34 and 4.39 using Embedded MATLAB function. The minimum and maximum values of the outputs k_a, k_b and k_c are calculated using two MinMax block in the Simulink block set. The two resulting outputs min_k_abc and max_k_abc together with the above calculated values for $D_A(t)$, $D_B(t)$ and $D_C(t)$ and the input phi_i are used to calculate the duty ratios of the switches according to equation 4.40 using the same Embedded MATLAB function.

A 2 kHz triangle carrier with a peak value and minimum value of one and zero volt is generated using a 2 kHz square pulse generator with 50 % duty cycle, a subtractor and an integrator with multiplication constant. The nine calculated values of the duty ratios for the switches and the 2 kHz triangle carrier are given as inputs to another Embedded MATLAB function to generate the gate switching pulses for the nine bidirectional switches. A method of generating the gate switching pulses using adders, comparators and logic gates is also shown in Fig. 4.19. The source code for generating the gate switching pulses is the same as given in section 4.2.2 above, except that the nine gate pulses tAa to tCc, tABa, tBAb and tBAc in this source code are replaced by qAa to qCc, qABa, qABb and qABc respectively. The three phase sine wave generator, the nine IGBT bidirectional switch matrix, R-L load etc. are the same as explained in Section 3.3.1 of Chapter III, except that in the three phase AC source model, in the box corresponding to Phase Angle of Phase A (in degrees), a value of zero is entered.

4.4.3 SIMULATION RESULTS: The simulation of the model shown in Fig. 4.19 was carried out using SIMULINK [51]. The ode15s(stiff/NDF) solver is used. The simulation results for the harmonic spectrum of line to neutral output voltage, input current and line to line output voltage are shown in Fig. 4.20 to 4.22 respectively. Simulation results for the line to neutral output voltage, input current, line to line output voltage, load current are shown in Fig. 4.23 to 4.26. The 2 kHZ triangle carrier and gate pulse pattern are same as shown in Fig. 4.17 and 4.18 respectively. Simulation results for a modulation index k of 0.26667 and three phase sine wave input voltage are tabulated in Table 4.3 below:

TABLE 4.3: Model SimulationResults 3

Sl.No.	Algorithm	THD of Line to Neutral Output Voltage (p.u.)	THD Line to Line Output Voltage (p.u.)	THD of Input Current (p.u.)
1	Ned Mohan	2.567	1.377	2.622

4.5 DISCUSSION OF RESULTS: Comparing the results in Table 4.2 with Table 4.3, it is seen that with three phase sine wave input voltages the value of THD for the line to neutral, line to line and input current are lower compared to three phase cosine wave input voltages for the Ned Mohan algorithm. Comparing Table 4.1 with Table 4.2 and 4.3, it is seen that the THD of line to neutral, line to line voltages and the input current are much lower for Sunter-Clare algorithm as compared to Ned

Mohan algorithm. Considering practical implementation issues discussed in Section 3.3.3 of Chapter III, Ned Mohan algorithm with three phase sine wave input voltages is preferable to that with three phase cosine wave input voltages. The linear range for modulation index is 0.866 for Sunter-Clare algorithm and 0.577 for Ned Mohan algorithm.

4.6 CONCLUSIONS: Considering factors like THD of line to neutral, line to line output voltages and input current, it is seen that Sunter-Clare algorithm is superior to Ned Mohan algorithm. The two algorithms discussed in this chapter are recently proposed. Also for both the algorithms the modulation index is well within the linear modulation range.

A4.1 APPENDIX: The Sunter-Clare algorithm is empirical based on assumptions and hence a direct mathematical proof can't be given. Ned Mohan algorithm for three phase cosine wave and sine wave input voltages is proved below:

Case A: The phase a output voltage v_a using equation 4.18 for three phase cosine wave input voltages can be be defined as follows:

$v_a = k_a*V_{im}*[cos\ (\omega_i.t)*cos(\omega_i.t - \varphi_i) + cos(\omega_i.t - 2\pi/3)*cos(\omega_i.t - 2\pi/3 - \varphi_i) + cos(\omega_i.t - 4\pi/3)*cos(\omega_i.t - 4\pi/3 - \varphi_i)]$ *(A4.1.1)*

$cos(A)*cos(B) = (1/2)*cos(A+B) + (1/2)*cos(A-B)$ *(A4.1.2)*

Using equation A.4.1.2 in equation A4.1.1 and simplifying,

$v_a = k_a*V_{im}*[(1/2)*cos(2\omega_i.t - \varphi_i) + (-1/2)*cos(2\omega_i.t - \varphi_i) + (3/2)*cos(\varphi_i)]$ *(A4.1.3)*

i.e. $v_a = (3/2)*k_a* V_{im}*cos(\varphi_i)$ *(A4.1.4)*

Equation A4.1.4 well agrees with equation 4.19.

Case B: The phase a output voltage v_a using equation 4.32 for three phase sine wave input voltages can be be defined as follows:

$v_a = k_a*V_{im}*[sin\ (\omega_i.t)*sin(\omega_i.t - \varphi_i) + sin(\omega_i.t - 2\pi/3)*sin(\omega_i.t - 2\pi/3 - \varphi_i) + sin(\omega_i.t - 4\pi/3)*sin(\omega_i.t - 4\pi/3 - \varphi_i)]$ *(A4.1.5)*

$sin(A)*sin(B) = (1/2)*cos(A-B) - (1/2)*cos(A+B)$ *(A4.1.6)*

Using equation A4.1.6 in equation A4.1.5 and simplifying,

$$v_a = k_a * V_{im} * \frac{1}{2} * \left[cos(\varphi_i) - cos(\theta) + cos(\varphi_i) - cos\left(\theta - \frac{4\pi}{3}\right) + cos(\varphi_i) - cos\left(\theta - \frac{8\pi}{3}\right) \right] \quad (A4.1.7)$$

$$where \quad \theta = \left(2.\omega_i.t - \varphi_i\right)$$

$$v_a = \frac{3}{2} * k_a * V_{im} * cos(\varphi_i) \quad (A4.1.8)$$

Equation A4.1.8 well agrees with equation 4.33.

This proves Ned Mohan algorithm for three phase cosine wave and sine wave input voltages.

Chapter V
Matrix Converter Fed Vector Controlled Three Phase Induction Motor Drive

5.1 INTRODUCTION: The three phase AC to three phase AC Matrix Converter (MC) finds applications in three phase Induction M-otor (IM) drives [6-8, 12, 14]. This chapter examines the modelling aspects of vector controlled three phase IM drive fed by MC. The performance of the Vector controlled three phase IM drive is obtained by simulation using SIMULINK when the MC is switched by various carrier based modulation techniques such as by using Venturini and the recently proposed Sunter-Clare and Ned Mohan algorithms.

5.2 VECTOR CONTROL OF THREE PHASE INDUCTION MOTOR DRIVE: This section on Vector control of three phase IM drive is completely based on reference 15. Referring to Fig.5.1, at time t, the d-axis is shown at an angle θda with respect to the stator a-axis. The relation connecting d-q axis stator current with the abc-axis stator current can be expressed as in equation 5.1 below.

The same transformation matrix defined in equation 5.1 applies to transform stator abc-axis voltages and flux linkages to corresponding dq-axis stator voltages and flux linkages.

The transformation matrix for the rotor currents from abc to dq-axis is defined in equation 2 below, which applies to rotor three phase voltages and flux linkages as well.

$$\begin{bmatrix} isd \\ isq \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos(\theta_{da}) & \cos(\theta_{da} - \frac{2\pi}{3}) & \cos(\theta_{da} - \frac{4\pi}{3}) \\ -\sin(\theta_{da}) & -\sin(\theta_{da} - \frac{2\pi}{3}) & -\sin(\theta_{da} - \frac{4\pi}{3}) \end{bmatrix} * \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (5.1)$$

$$\begin{bmatrix} ird \\ irq \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos(\theta_{dA}) & \cos(\theta_{dA} - \frac{2\pi}{3}) & \cos(\theta_{dA} - \frac{4\pi}{3}) \\ -\sin(\theta_{dA}) & -\sin(\theta_{dA} - \frac{2\pi}{3}) & -\sin(\theta_{dA} - \frac{4\pi}{3}) \end{bmatrix} * \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \quad (5.2)$$

In equation 5.2, θ_{dA} is the angle made by the rotor A-axis with the d-axis.

The inverse relation connecting the abc-axis stator current with dq-axis stator current can be expressed as follows:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos(\theta_{da}) & -\sin(\theta_{da}) \\ \cos(\theta_{da} - \frac{2\pi}{3}) & -\sin(\theta_{da} - \frac{2\pi}{3}) \\ \cos(\theta_{da} - \frac{4\pi}{3}) & -\sin(\theta_{da} - \frac{4\pi}{3}) \end{bmatrix} * \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} \quad (5.3)$$

Similar transformation applies to abc-axis voltages and flux linkages in the stator.

The transformation of rotor currents in the dq-axis to abc-axis can be obtained by replacing θda to θdA in equation 5.3. This is given below:

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos(\theta_{dA}) & -\sin(\theta_{dA}) \\ \cos(\theta_{dA} - \frac{2\pi}{3}) & -\sin(\theta_{dA} - \frac{2\pi}{3}) \\ \cos(\theta_{dA} - \frac{4\pi}{3}) & -\sin(\theta_{dA} - \frac{4\pi}{3}) \end{bmatrix} * \begin{bmatrix} i_{rd} \\ i_{rq} \end{bmatrix} \quad (5.4)$$

The same transformation matrix given in equation 5.4 applies to voltages and flux linkages in the rotor.

5.2.1 FLUX LINKAGES OF STATOR AND ROTOR WINDINGS_: The flux linkages in the stator d and q axis windings can be expressed as follows [15]:

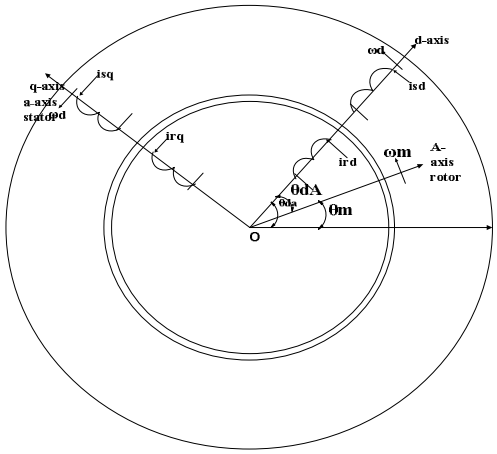


FIG. 5.1: STATOR AND ROTOR REPRESENTATION BY EQUIVALENT DQ WINDING CURRENTS

$$\lambda_{sd} = L_s . i_{sd} + L_m . i_{rd} \quad (5.5)$$

$$\lambda_{sq} = L_s . i_{sq} + L_m . i_{rq} \quad (5.6)$$

$$L_s = L_{ls} + L_m \quad (5.7)$$

Similarly for the rotor, the flux linkage expression in the d-q axis windings can be expressed as follows:

$$\lambda_{rd} = L_r . i_{rd} + L_m . i_{sd} \quad (5.8)$$

$$\lambda_{rq} = L_r . i_{rq} + L_m . i_{sq} \quad (5.9)$$

$$L_r = L_{lr} + L_m \quad (5.10)$$

5.2.2 VOLTAGE EQUATIONS FOR STATOR AND ROTOR DQ-AXIS WINDINGS: The dq-axis voltage equation for the stator can be expressed as follows [15]:

$$v_{sd} = R_s . i_{sd} + \frac{d(\lambda_{sd})}{dt} - \omega_d . \lambda_{sq} \quad (5.11)$$

$$v_{sq} = R_s . i_{sq} + \frac{d(\lambda_{sq})}{dt} + \omega_d . \lambda_{sd} \quad (5.12)$$

In equations 5.11 and 5.12, ωd is the speed of the dq-axis reference frame relative to the stator winding.

The rotor dq-axis voltage expression is given below [15]:

$$v_{rd} = R_r . i_{rd} + \frac{d(\lambda_{rd})}{dt} - \omega_{dA} . \lambda_{rq} \quad (5.13)$$

$$v_{rq} = R_r . i_{rq} + \frac{d(\lambda_{rq})}{dt} + \omega_{dA} . \lambda_{rd} \quad (5.14)$$

$$\omega_{dA} = (\omega_d - \omega_m) \quad (5.15)$$

$$\omega_m = \frac{(\text{No. of Poles } P) * \omega_{mech}}{2} \quad (5.16)$$

In equations 5.13 and 5.14 ω_{dA} is the speed of the dq-axis reference frame relative to the rotor winding speed.

The value of ω_d can be an arbitrary choice. The three common reference frames are classified as follows:

$\omega_d = \omega_{sync}$ = synchronous reference frame
$\omega_d = 0$ = stationary reference frame
$\omega_d = \omega_m$ =rotor reference frame.

PI controllers can be easily designed in synchronous reference frame and hence this reference frame is chosen here.

5.2.3 ELECTROMAGNETIC TORQUE: The torque is produced in the rotor d-axis due to flux density in the q-axis windings and in the rotor q-axis due to flux density in the d-axis windings. These two torque acts in opposite direction. The net electromagnetic torque can be expressed as follows [15]:

$$T_{em} = \frac{P}{2}.(\lambda_{rq}.i_{rd} - \lambda_{rd}.i_{rq}) \quad (5.17)$$

Equation 5.17 can also be expressed in the following form:

$$T_{em} = \frac{P.L_m}{2}.(i_{sq}.i_{rd} - i_{sd}.i_{rq}) \quad (5.18)$$

5.2.4 ELECTRODYNAMICS: The acceleration is determined by the difference of the electromagnetic torque and the load torque acting on Jeq, the combined inertia of the motor and the load. In terms of the rotor speed ωmech in mechanical radians per second, the following equation is valid [15]:

$$J_{eq}.\frac{d(\omega_{mech})}{dt} = (T_{em} - T_L) \quad (5.19)$$

In equation 5.19, T_L is the load torque.

Substituting equations 5.5 to 5.7 in equations 5.11 to 5.12, the stator voltage equations can be expressed as follows:

$$v_{sd} = R_s.i_{sd} - \omega_d.\lambda_{sq} + \frac{L_{ls}.d(i_{sd})}{dt} + \frac{L_m.d(i_{sd} + i_{rd})}{dt} \quad (5.20)$$

$$v_{sq} = R_s.i_{sq} + \omega_d.\lambda_{sd} + \frac{L_{ls}.d(i_{sq})}{dt} + \frac{L_m.d(i_{sq} + i_{rq})}{dt} \quad (5.21)$$

Similarly, using equations 5.8 to 5.10 in equations 5.13 and 5.14, the rotor voltage equations can be expressed as follows:

$$v_{rd} = 0 = R_r . i_{rd} - \omega_{dA} . \lambda_{rq} + \frac{L_{lr} . d(i_{rd})}{dt} + \frac{L_m . d(i_{sd} + i_{rd})}{dt} \quad (5.22)$$

$$v_{rq} = 0 = R_r . i_{rq} + \omega_{dA} . \lambda_{rd} + \frac{L_{lr} . d(i_{rq})}{dt} + \frac{L_m . d(i_{sq} + i_{rq})}{dt} \quad (5.23)$$

5.2.5 PRINCIPLE OF COMPUTER SIMULATION OF THREE PHASE INDUCTION MOTOR DRIVE: The dq winding currents can be calculated from flux linkage equations. Combining equations 5.5, 5.6 and 5.8, 5.9, we have the following:

From equation 5.24, the dq-axis stator and rotor currents can be expressed as follows:

$$\begin{bmatrix} \lambda_{sd} \\ \lambda_{sq} \\ \lambda_{rd} \\ \lambda_{rq} \end{bmatrix} = \begin{bmatrix} L_s & 0 & L_m & 0 \\ 0 & L_s & 0 & L_m \\ L_m & 0 & L_r & 0 \\ 0 & L_m & 0 & L_r \end{bmatrix} * \begin{bmatrix} i_{sd} \\ i_{sq} \\ i_{rd} \\ i_{rq} \end{bmatrix} \quad (5.24)$$

$$\begin{bmatrix} i_{sd} \\ i_{sq} \\ i_{rd} \\ i_{rq} \end{bmatrix} = \begin{bmatrix} L_s & 0 & L_m & 0 \\ 0 & L_s & 0 & L_m \\ L_m & 0 & L_r & 0 \\ 0 & L_m & 0 & L_r \end{bmatrix}^{-1} * \begin{bmatrix} \lambda_{sd} \\ \lambda_{sq} \\ \lambda_{rd} \\ \lambda_{rq} \end{bmatrix} \quad (5.25)$$

For computer simulation, initial values of dq-axis stator and rotor currents must be known and so also the flux linkages. These are given below:

$$i_{sd}(0) = \text{sqrt}(2/3)*(3*(Is/2))*\cos(\theta_i) \quad `(5.26)$$

$$i_{sq}(0) = \text{sqrt}(2/3)*(3*(Is/2))*\sin(\theta_i) \quad (5.27)$$

Similarly we can calculate $v_{sd}(0)$, $v_{sq}(0)$ and the dq-axis stator and rotor flux linkages.

5.2.6 PRINCIPLE OF VECTOR CONTROL: Accurate speed control of three phase IM can be achieved by vector control [15]. In speed and position control, the ability to produce a step change in torque on command represents total control over the drives. In vector control of three phase IM drives, the d-axis is aligned with the rotor flux linkage space vector such that the rotor flux linkage in the q-axis is zero. Thus we have the following equations:

$$\lambda_{rq}(t) = 0 \quad (5.28)$$

Using equation 5.28 in equation 5.9 and simplifying,

$$i_{rq} = \frac{- L_m . i_{sq}}{L_r} \quad (5.29)$$

The condition d-axis is always aligned with $\overrightarrow{\lambda_r}$, such that $\lambda_{rq} = 0$ also results in $\frac{d\lambda_{rq}}{dt} = 0$. Using this value of λ_{rq} and $\frac{d\lambda_{rq}}{dt}$ in the dq-axis equivalent circuit, the new simplified equivalent circuit for vector control of three phase IM is shown in Fig. 5.2 and 5.3.

In vector control, as long as the d-axis is aligned with rotor flux linkage, the q-axis rotor flux linkage and its first derivative are zero. Also in a squirrel cage rotor, vrq =0 and equation 5.14 gives the following equation:

$$\omega_{dA} = \frac{-R_r . i_{rq}}{\lambda_{rd}} \quad (5.30)$$

and rotor time constant is given by

$$\tau_r = \frac{L_r}{R_r} \quad (5.31)$$

Using equation 5.29 and 5.31 in equation 5.30, the rotor slip speed can be expressed as follows:

$$\omega_{dA} = \frac{L_m . i_{sq}}{\tau_r . \lambda_{rd}} \quad (5.32)$$

Since flux linkage in the rotor q-axis is zero, the e.m. torque is produced by rotor d-axis flux linkage acting on rotor q-axis current. The e.m. torque Tem is given below:

$$T_{em} = \frac{-P.\lambda_{rd} . i_{rq}}{2} \quad (5.33)$$

Using equation 5.29 in equation 5.33, we have the following:

$$T_{em} = \frac{P.\lambda_{rd}}{2} * \left(\frac{L_m . i_{sq}}{L_r} \right) \quad (5.34)$$

5.2.7 D-AXIS ROTOR FLUX LINKAGE DYNAMICS: Referring to Fig.5.2 and using Laplace Transform, we have the following equations [15]:

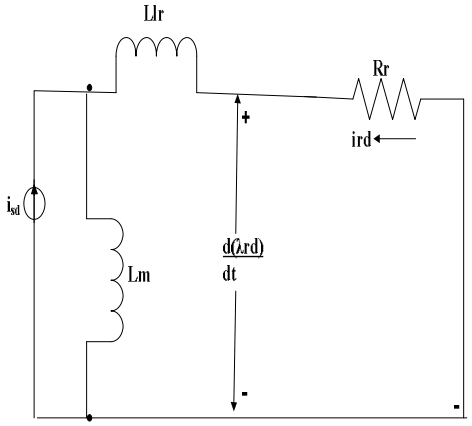


FIG. 5.2: THE D-AXIS SIMPLIFIED EQUIVALENT CIRCUIT UNDER VECTOR CONTROL

$$i_{rd}(s) = \frac{-s.L_m . i_{sd}(s)}{(R_r + sL_r)} \quad (5.35)$$

Using equation 5.8 and equation 5.31 in equation 5.35 and simplifying,

$$\lambda_{rd}(s) = \frac{L_m . i_{sd}(s)}{(1 + s\tau_r)} \quad (5.36)$$

In time domain, equation 5.36 can be expressed as follows:

$$\frac{d\lambda_{rd}}{dt} + \frac{\lambda_{rd}}{\tau_r} = \frac{L_m . i_{sd}}{\tau_r} \quad (5.37)$$

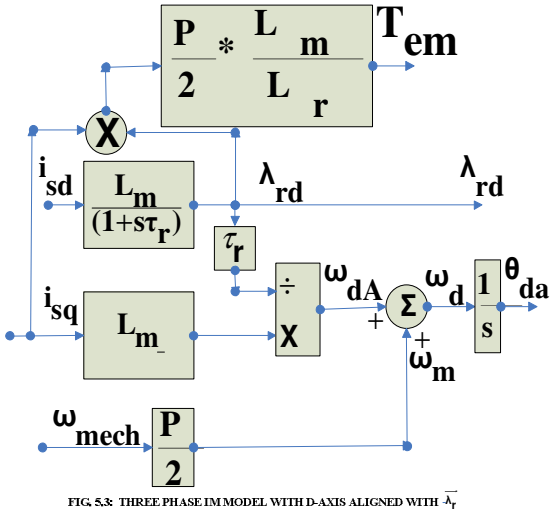


FIG. 5.3: THREE PHASE IM MODEL WITH D-AXIS ALIGNED WITH $\overline{\lambda_r}$

The detailed model of the three phase vector controlled IM using Current Regulated PWM inverter is shown in Fig. 5.3 and 5.4. The d-axis winding reference stator current i^*_{sd} controls the rotor flux linkage λrd and the q-axis winding reference stator current i^*_{sq} controls the rotor e.m. torque Tem. The reference dq-axis stator currents are converted into abc-axis reference stator phase current $i^*_a(t)$, $i^*_b(t)$ and $i^*_c(t)$.

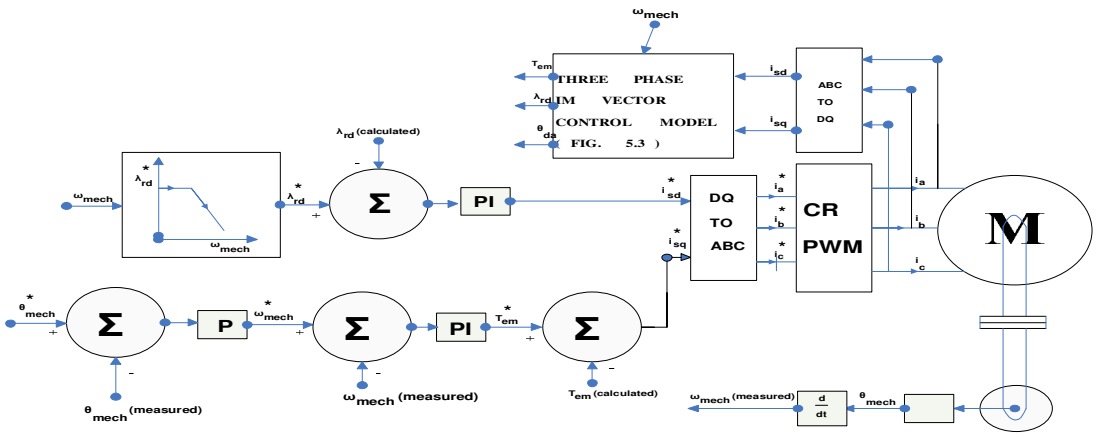


FIG. 5.4: VECTOR CONTROLLED THREE PHASE IM DRIVE WITH CR-PWM

A current regulated PWM inverter supplies the current to the three phase IM.

The current references i^*_{sd} and i^*_{sq} are generated by cascaded torque, speed and position control loops shown in the block diagram of Fig. 5.4. , where θ^*_{mech} is the position reference input. The actual position θ_{mech} and the rotor speed ω_{mech} are measured and the rotor flux linkage λrd is calculated as shown in Fig. 5.4. For extended speed range operation beyond rated speed flux weakening is implemented.

To design speed loop without torque loop, the torque expression is derived at the rated value of i^*_{sd}. In steady state under vector control, $i_{rd} = 0$ in Fig. 5.2. Using equation 5.8, under vector control in steady state, we have the following equation:

$$\lambda_{rd} = L_m .i_{sd} \qquad (5.38)$$

Substituting equation 5.38 and equation 5.29 into the torque expression of equation 33, we have the following:

$$T_{em} = \frac{P}{2}.\frac{L_m^2}{L_r}.i^*_{sd}.i_{sq} = k.i_{sq} \qquad (5.39)$$

where k is a constant. The speed loop diagram is shown in Fig. 5.5, where PI controller constants are calculated on the basis that the cross over frequency of the open loop is 25 rad/sec and the phase margin is 60 degrees.

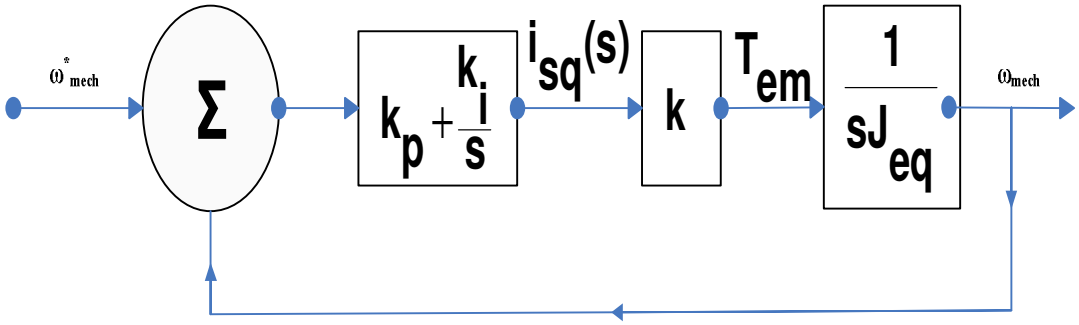


FIG. 5.5: SPEED LOOP CONTROLLER

The stator voltages to be applied can be calculated as follows:

The switching frequency of the PWM converter is maintained constant. The voltage to be applied to the pwm converter in order to get the stator current equal to the reference value is derived below:

The leakage factor σ is defined as follows:

$$\sigma = 1 - \frac{L_m^2}{L_s . L_r} \qquad (5.40)$$

Using equation 5.8 in equation 5.5, simplifying and using equation 5.40, we have the following:

$$\lambda_{sd} = \sigma L_s . i_{sd} + \frac{L_m . \lambda_{rd}}{L_r} \qquad (5.41)$$

Using equation 5.6 and 5.29, we have the following:

$$\lambda_{sq} = \sigma L_s . i_{sq} \qquad (5.42)$$

Using equations 5.41 and 5.42 in equations 5.11 and 5.12 and simplifying, we have the following:

$$v_{sd} = \underbrace{R_s . i_{sd} + \sigma L_s . \frac{di_{sd}}{dt}}_{v'_{sd}} + \underbrace{\frac{L_m}{L_r} . \frac{d(\lambda_{rd})}{dt} - \sigma . \omega_d . L_s . i_{sq}}_{v_{sd\_comp}} \qquad (5.43)$$

and

$$v_{sq} = \underbrace{R_s . i_{sq} + \sigma L_s . \frac{di_{sq}}{dt}}_{v'_{sq}} + \underbrace{\frac{\omega_d . L_m . \lambda_{rd}}{L_r} . — + \sigma . \omega_d . L_s . i_{sd}}_{v_{sq\_comp}} \qquad (5.44)$$

5.2.8 DESIGNING THE PI CONTROLLERS: In equations 5.43 and 5.44, the term vsd' and vsq' are due to d and q-axis stator currents. The vsd_comp and vsq_comp are disturbance terms. These equations are re-written as follows [15]:

$$v'_{sd} = R_s . i_{sd} + \sigma L_s . \frac{di_{sd}}{dt} \qquad (5.45)$$

and

$$v'_{sq} = R_s . i_{sq} + \sigma L_s . \frac{di_{sq}}{dt} \qquad (5.46)$$

The compensation terms are given below:

$$v_{sd\_comp} = \frac{L_m}{L_r} . \frac{d(\lambda_{rd})}{dt} - \sigma . \omega_d . L_s . i_{sq} \qquad (5.47)$$

$$v_{sq\_comp} = \frac{\omega_d . L_m . \lambda_{rd}}{L_r} + \sigma . \omega_d . L_s . i_{sd} \qquad (5.48)$$

The block diagram is shown in Fig. 5.6. As shown in Fig. 5.6, reference voltages for the stator d and q-axis are generated from stator d and q-axis stator currents i^*_{sd} and i^*_{sq}. Using the calculated value of θda, the reference phase voltages v^*_a, v^*_b and v^*_c are calculated. The actual phase voltages va, vb and vc are supplied by the three phase PWM inverter. The voltages v'_{sd} and v'_{sq} in Fig. 5.6 are generated by PI controllers in the current loop. Assuming perfect compensation, each channel results in the block diagram shown in Fig. 5.7(A) & (B). The transfer Function isd(s)/v'sd(s) and isq(s)/v'sq(s) are derived from equation 5.45 and 5.46 respectively. The PI controller for current loop is designed assuming that the bandwidth of the current loop controller is 10 times the bandwidth of the speed loop controller (250 rad/sec) and the phase margin is 60 degrees.

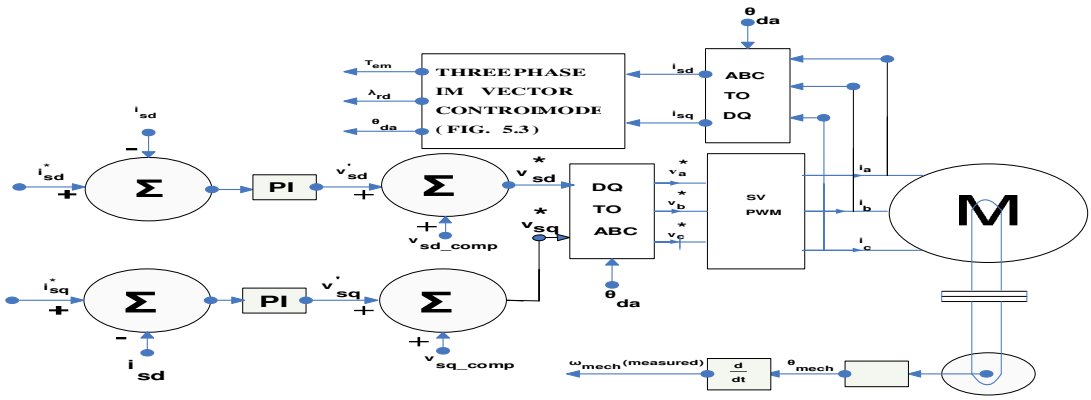


FIG. 5.6: THREE PHASE IM VECTOR CONTROL WITH APPLIED VOLTAGE

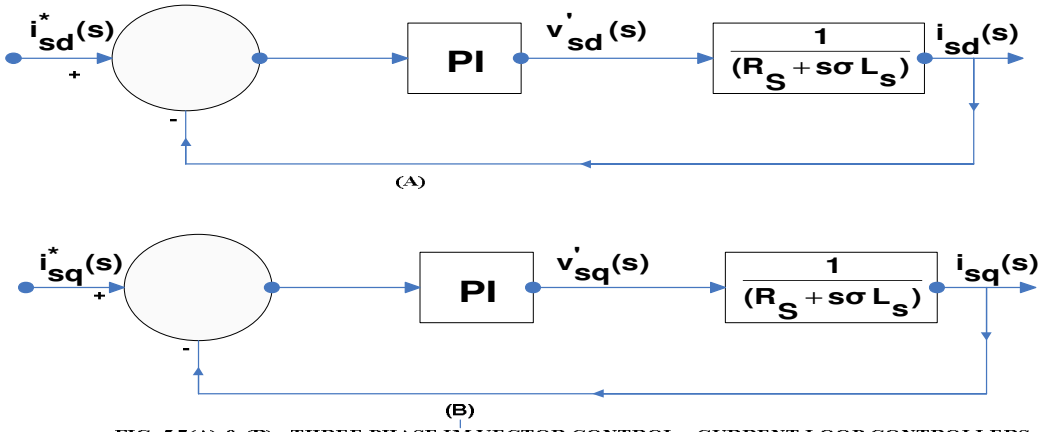


FIG. 5.7(A) & (B): THREE PHASE IM VECTOR CONTROL – CURRENT LOOP CONTROLLERS

5.3 MODEL OF VECTOR CONTROLLED THREE PHASE I.M. DRIVE: In this section the model of the vector controlled three phase IM drive is developed using SIMULINK [51]. The performance of the above IM drive is studied in detail by simulation. The three phase IM drive used here has the parameters given in Table 5.1.

TABLE 5.1: Three Phase IM Parameters

Sl.No.	Parameters	Value	Unit
1	RMS Line to Line Input Supply Voltage	400	Volts
2	Input Frequency	50	Hz
3	Power Output	4	kW
4	RMS Line to Line Machine Voltage	400	Volts
5	Machine Frequency	50	Hz
6	No. of Phase	3	-
7	No. of Poles	4	-
8	Stator Resistance Rs	1.405	Ohms
9	Stator Leakage Inductance Lls	0.005839	Henries

10	Rotor Resistance Rr'	1.395	Ohms
11	Rotor Leakage Inductance Llr'	0.005839	Henries
12	Mutual Inductance Lm	0.1722	Henries
13	Moment of Inertia J	0.0131	Kg-m^2
14	Damping Constant B	0.002985	Nw-m-sec

5.3.1 DEVELOPMENT OF THE MODEL: The model of Vector Controlled three phase IM drive developed in SIMULINK using parameters shown in Table 5.1 is shown in Fig. 5.8. The model is developed based on the equations and requirements set forth in Section 5.2. The MATLAB program to calculate the PI controller parameters for the speed control and current control loop, for the IM parameters in Table 5.1, is given in A5.1 Appendix in this chapter together with the simulation results. From the simulation results, the values are tabulated in Table 5.2.

TABLE 5.2: PI Controller Parameters

SL.NO.	SPEED CONTROL LOOP		CURRENT CONTROL LOOP		ROTOR SPEED	INITIAL D-AXIS STATOR CURRENT AMPS
	Kp	Ki	Kpi	Kii	Mech.Rad./Sec.	
1	0.1257	1.8139	1.7831	662.9626	149.225	6.7789

The model shown in Fig. 5.8 uses the values shown in Table 5.2 for the PI controller parameters for the speed control and current control loop, initial d-axis stator current and the rotor speed set point. The initial d-axis stator current Isd_0 is subtracted from the estimated/actual d-axis stator current from the IM model and the difference which gives the d-axis stator reference current Isd* is given to PI controller in the current control loop to generate d-axis stator reference voltage vsd*. Similarly the rotor speed set point is subtracted from the actual/estimated rotor speed from the IM model and the difference speed is given to PI controller in the speed control loop to generate q-axis stator current reference Isq*. This Isq* is subtracted from the actual/estimated q-axis stator current from the IM model and the difference current is given to PI controller in the current control loop to generate q-axis stator reference voltage vsq*. The actual/estimated angular position of the stator a-axis reference with respect to the d-axis theta_da_est, vsd*, vsq* are given to three Function blocks in Simulink block set to generate the three phase abc-axis equivalent of stator voltages va, vb and vc [15]. These values of va, vb and vc together with the rotor position theta_da from the IM model are given to two Function blocks to generate the dq-axis equivalent of the stator voltages vsd and vsq [15]. Using vsd, vsq, rotor speed ωd from the IM model, stator resistance and the stator dq-axis flux linkages as input, Embedded MATLAB Function1 block together with integrators in Fig. 5.8 generate the stator dq-axis flux linkages using equations 5.11 and 5.12. In vector control of three phase IM drive, rotor q-axis flux linkage λrq is set to zero. The equations 5.25 and 5.37 are combined together to generate stator cur -

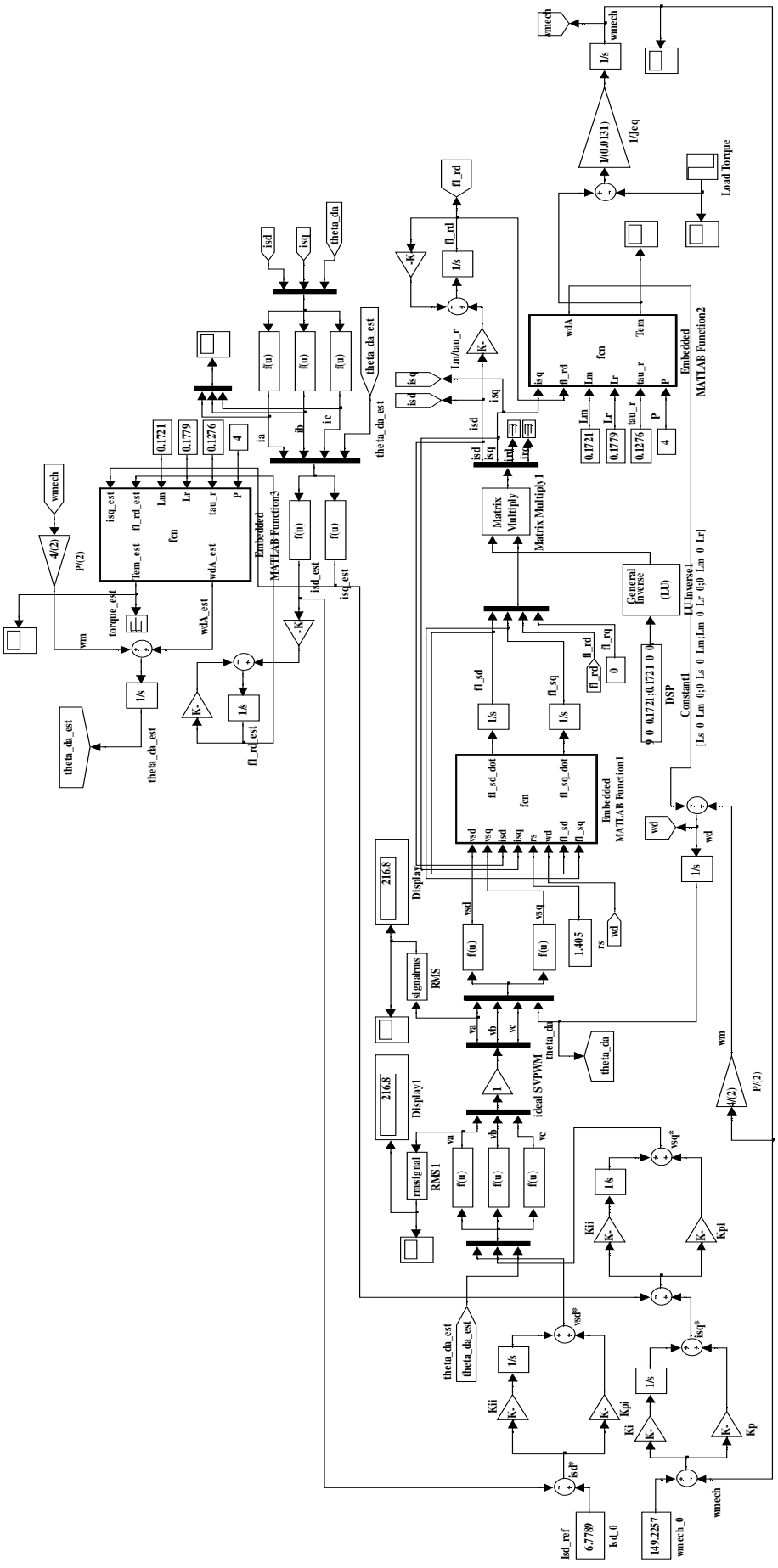


FIG. 5.8: MODEL OF A THREE PHASE VECTOR CONTROLLED INDUCTION MOTOR DRIVE

rents and the rotor d-axis flux linkage λrd as shown in Fig. 5.8, where the DSP constant1 block together with the LU Inverse1 block calculates the inverse of the stator and rotor inductance matrix defined in equation 5.25. The dq-axis stator and rotor flux linkages given as input to the MUX block is multiplied by the inverse of the stator and rotor inductance matrix using Matrix multiply1 block to generate the dq-axis stator and rotor currents. Using d-axis stator current as input, the two gain blocks, the subtractor and the integrator block calculates rotor d-axis flux linkage λrd using equation 5.37 given above. Using the given IM parameters, computed isq and λrd, Embedded MATLAB Function2 block calculates the rotor slip speed ωdA and the electromagnetic torque Tem using equations 5.32 and 5.34 respectively. The load torque TL is generated using step block which is assumed to vary from 30 Nw-m to 15 Nw-m in 0.1 second. The E.M. torque Tem and load torque TL are used to compute the rotor speed ωmech according to equation 5.19 using a subtractor block, gain block and integrator as shown in Fig. 5.8. This value of ωmech is multiplied by the number of pair of poles to get the rotor speed in electrical radians per second which is then added with computed rotor slip speed ωdA to calculate the synchronous speed ωd according to equation 5.15. This value of ωd is integrated to get stator angular position with respect to the d-axis theta_da, as shown in Fig. 5.8.

These computed values of isd, isq and theta_da are transformed to abc-axis stator currents using three function blocks using the dq-axis to abc-axis transformation [15]. Using this computed values of stator and rotor currents in the abc-axis, Embedded MATLAB Function3 block along with summing and integrating blocks re-estimates slip speed ωdA_est and e.m. torque Tem_est, theta_da_est and λrd_est using equations 5.32, 5.34, 5.37 and 5.15 for comparison and feedback to the actual model of vector controlled three phase IM drive.

5.3.2 SIMULATION RESULTS: The simulation of the vector controlled three phase IM drive was carried out using SIMULINK [51]. The ode15s (stiff/NDF) solver is used. Simulation results for the rotor speed, E.M. Torque, stator currents and the load torque are shown in Fig. 5.9 to 5.12 respectively.

5.3.3 DISCUSSION OF RESULTS: From the simulation results it is seen that as the load torque is vaired from 30 Nw-m to 15 Nw-m, the rotor speed from the set point of 149.2257 mech.rad per sec shoots up and finally settles to the set point value. Rotor E.M. torque Tem falls from the initial value of 30 Nw-m falls to 15 Nw-m in 0.1 second corresponding to load torque. Stator current initially shoots up and finally settles to a constant value. This shows the accuracy of vector control of three phase IM drive.

5.4 VECTOR CONTROLLED THREE PHASE IM DRIVE FED BY MC: The vector controlled three phase IM drive whose parameters are given in table 5.1 and 5.2 when fed by a three phase AC to three phase AC MC is studied here using model simulation. SIMULINK is used for model development [51]. The MC is switched by various carrier based modulation algorithms such as by Venturini, Sunter-Clare and Ned Mohan [1-8, 11-17]. The performance of the above IM drive when

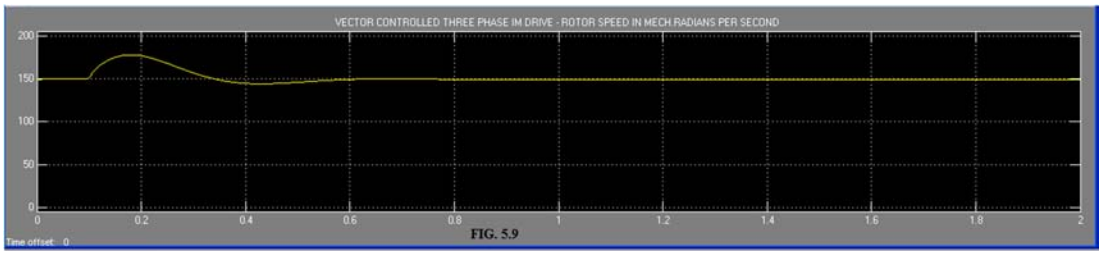


FIG. 5.9

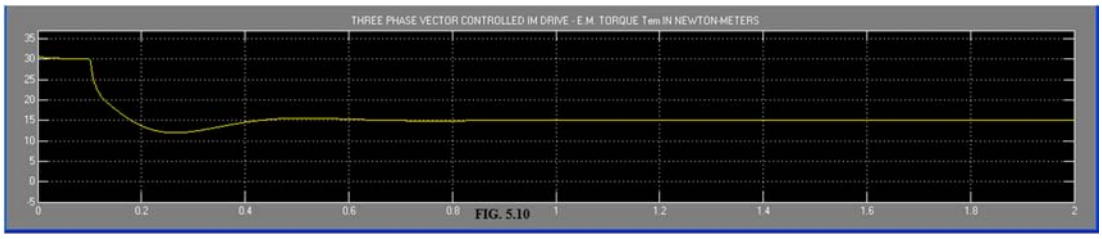


FIG. 5.10

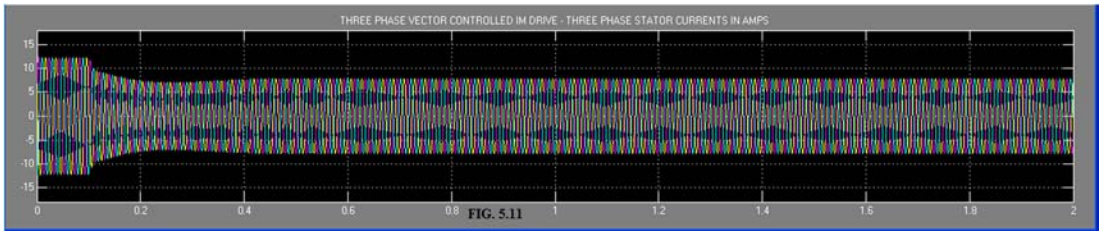


FIG. 5.11

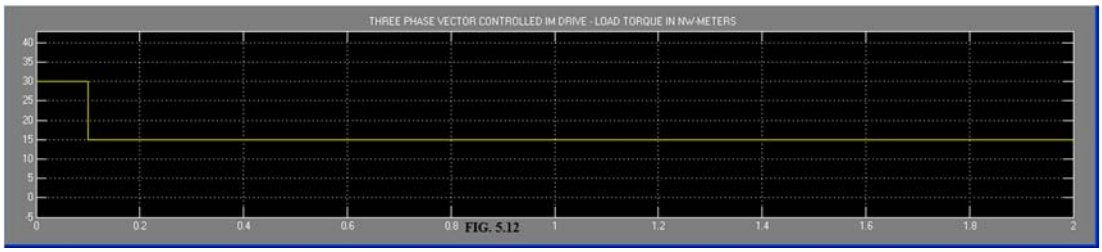


FIG. 5.12

fed by MC using all the above modulation algorithms is presented.

5.4.1: VECTOR CONTROLLED THREE PHASE IM DRIVE FED BY MC USING VENTURINI MODULATION ALGORITHM: The model of the vector controlled three phase IM drive fed by MC using Venturini modulation algorithm is shown in Fig. 5.13. Here unity input phase displacement factor is assumed. The model of the MC is already explained under section 3.3.3 of chapter III. The vector controlled three phase IM model is the one explained in Section 5.3 above. This vector controlled three phase IM model is used twice one to generate the gate pulses for the MC and the other to replace the hardware component of three Phase IM. The changes in the MC model is explained below:

Here modulation index q is calculated from the vector controlled three phase IM model. The reference value of dq-axis stator voltages vsd*, vsq* and theta_da_est are used to transform dq-axis stator voltage to abc-axis stator voltage as explained in Section 5.3 above. The stator voltage Va thus obtained is multiplied by 1.414 to obtain maximum output voltage per phase Vom. This value of Vom is then divided by maximum input voltage per phase Vim (400*√2 / √3 Volts from Table 5.1) to obtain the value of q. This q value is used in the Embedded MATLAB Function to generate the nine modulation functions for the MC switches. These nine modulation functions are compared with a

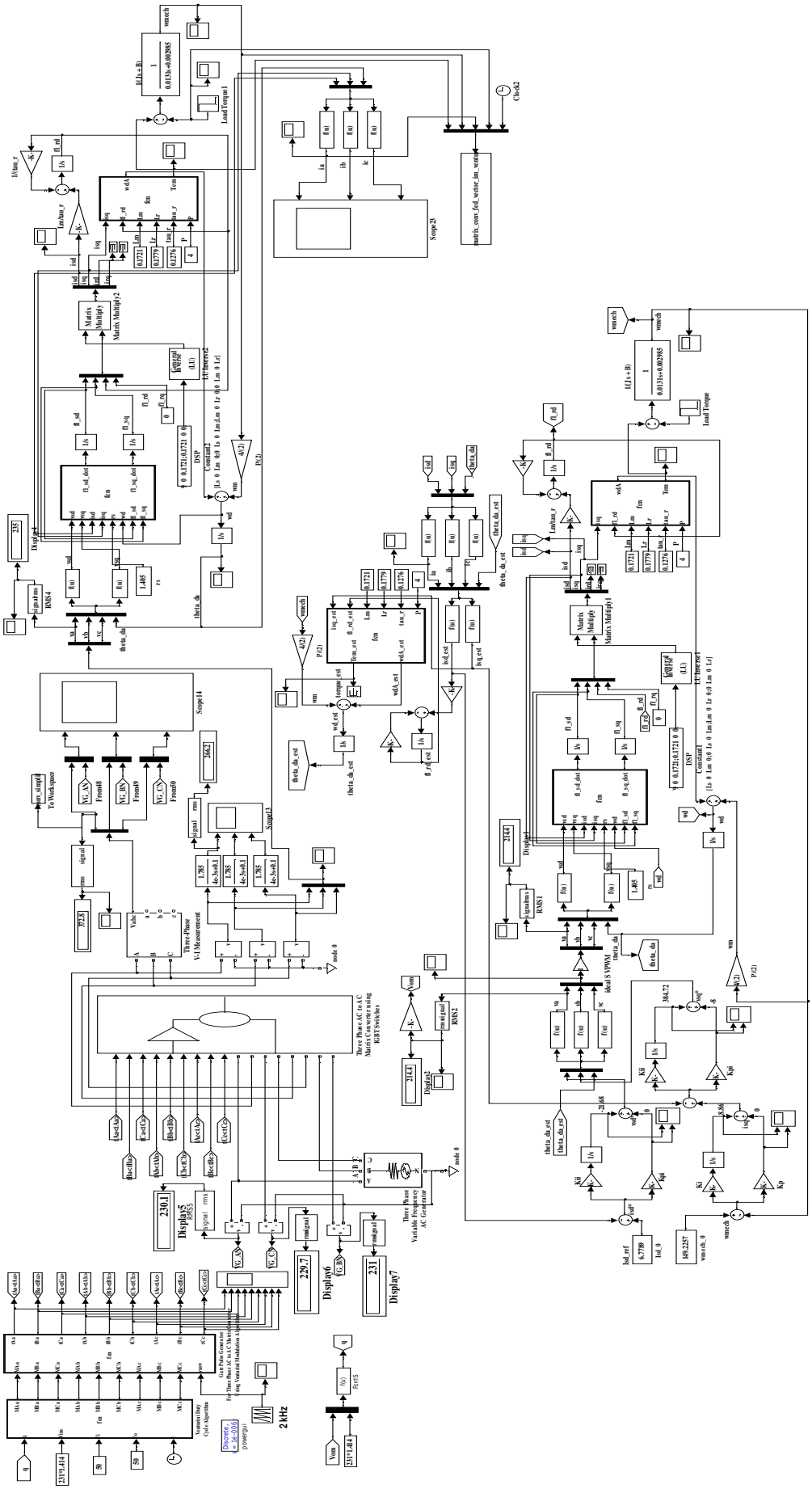


FIG. 5.13: VECTOR CONTROLLED THREE PHASE INDUCTION MOTOR DRIVE FED BY MATRIX CONVERTER USING VENTURINI ALGORITHM

2 kHz saw-tooth carrier and the gate pulses are generated using a second Embedded MATLAB Function as explained in Section 3.3.1 of Chapter III.

5.4.2 SIMULATION RESULTS: The simulation results using SIMULINK are shown in Fig. 5.14. [51]. The ode 23tb (Stiff/TR-BDF2) solver is used. From the simulation results it is seen that as the load torque varies from 30 to 15 Nw-M in 0.1 second, the Rotor E.M. torque after the initial transient settles to 15 Nw-M and the rotor speed reaches the set point of 149.2257 mech.radians per second. Rotor torque-speed curve also confirms this value.

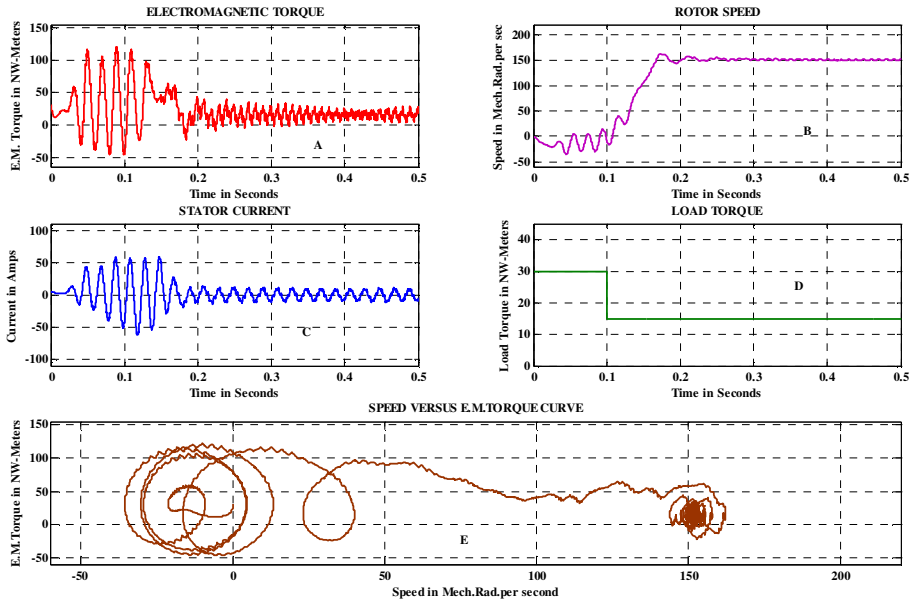


FIG. 5.14: VECTOR CONTROLLED THREE PHASE IM DRIVE FED BY MC USING VENTURINI ALGORITHM

5.4.3: VECTOR CONTROLLED THREE PHASE IM DRIVE FED BY MC USING SUNTER-CLARE MODULATION ALGORITHM: The model of the vector controlled three phase IM drive fed by MC using Sunter-Clare modulation algorithm is shown in Fig. 5.15. The model of the MC is already explained under section 4.2 of Chapter IV. The vector controlled three phase IM model is the one explained in Section 5.3 above. This vector controlled three phase IM model is used twice one to generate the gate pulses for the MC and the other to replace the hardware component of the three Phase IM. The changes in the MC model is explained below:

Here maximum output voltage per phase is calculated from the vector controlled three phase IM model. The reference values of dq-axis stator voltages vsd*, vsq* and theta_da_est are used to transform dq-axis stator voltage to abc-axis stator voltage as explained in Section 5.3 above. The stator voltage Va thus obtained is multiplied by 1.414 to obtain maximum output voltage per phase Vom. This Vom value is used in the Embedded MATLAB Function to generate the nine modulation functions for the MC switches. These nine modulation functions are compared with a 2 kHz saw-tooth carrier and the gate pulses are generated using the same Embedded MATLAB Function as explained in section 4.2.2 of Chapter IV.

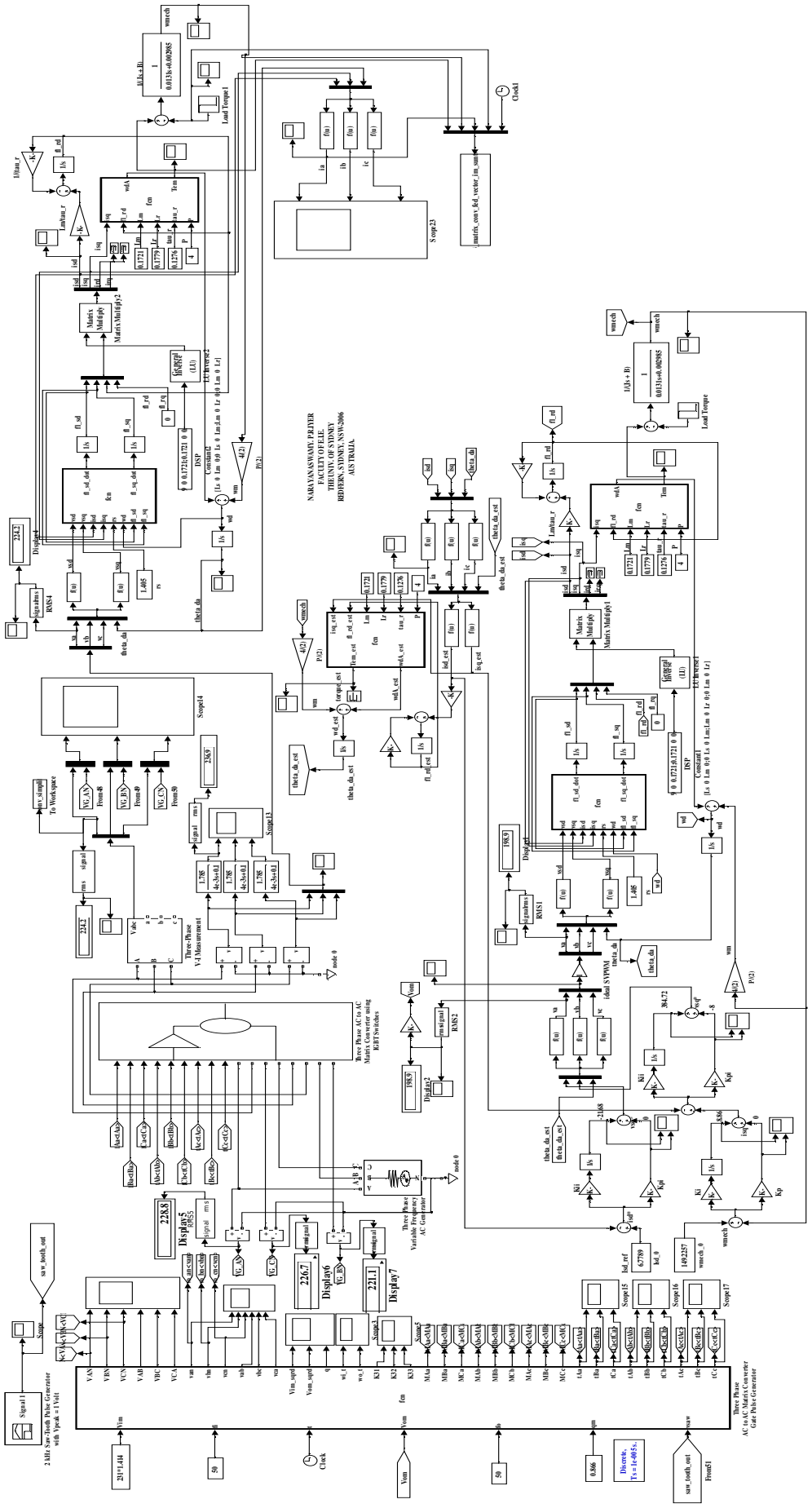


FIG. 5.15: MATRIX CONVERTER FED VECTOR CONTROLLED THREE PHASE INDUCTION MOTOR DRIVE USING SUNTER-CLARE ALGORITHM

5.4.4 SIMULATION RESULTS: The simulation results using SIMULINK are shown in Fig. 5.16 [51]. The ode 15s (Stiff/NDF) solver is used. From the simulation results it is seen that as the load torque varies from 30 to 15 Nw-M in 0.1 second, the Rotor E.M. torque after the initial transient settles to 15 Nw-M and the rotor speed reaches the set point of 149.2257 mech.radians per second. Rotor torque-speed curve also confirms this value.

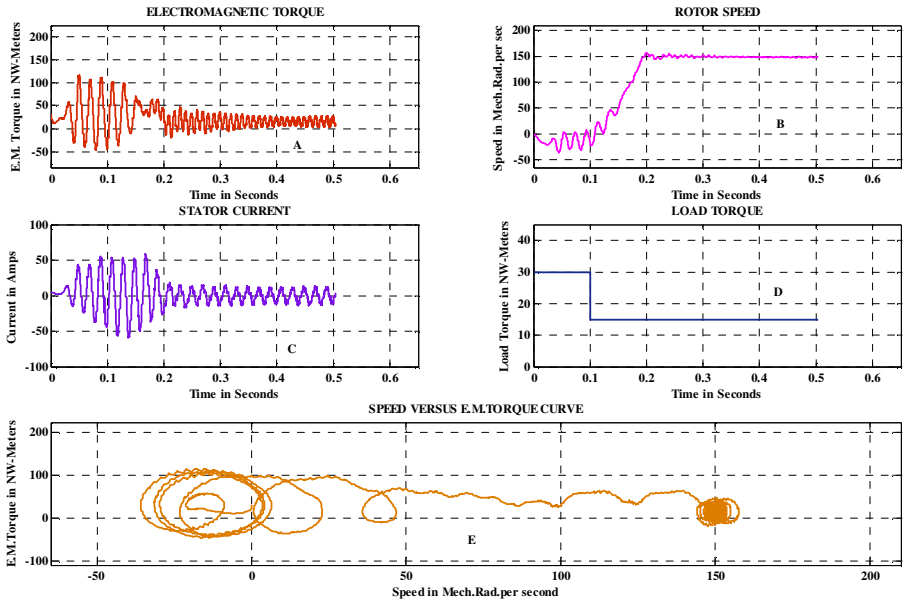


FIG. 5.16: VECTOR CONTROLLED THREE PHASE IM DRIVE FED BY MC USING SUNTER-CLARE ALGORITHM

5.4.5: VECTOR CONTROLLED THREE PHASE IM DRIVE FED BY MC USING NED MOHAN MODULATION ALGORITHM: The model of the vector controlled three phase IM drive fed by MC using Ned Mohan modulation algorithm is shown in Fig. 5.17. The model of the MC is already explained under section 4.4 of chapter IV. The vector controlled three phase IM model is the one explained in Section 5.3 above. This vector controlled three phase IM model is used twice one to generate the gate pulses for the MC and the other to replace the hardware component of the three Phase IM. The changes in the MC model is explained below:

Here output voltage per phase is calculated from the vector controlled three phase IM model. The reference values of dq-axis stator voltages vsd*, vsq* and theta_da_est are used to transform dq-axis stator voltages to abc-axis stator voltages as explained in Section 5.3 above. The stator voltage Va thus obtained is multiplied by 2/3 (0.6667) and then divided by maximum value of input voltage per phase Vim which is 326.56 from Table 5.1. This gives ka = k*sin(ωo.t) as per equation 4.33 of Chapter IV. This value of ka is made to phase lag by 6.667 milliseconds and 13.333 milliseconds, for a 50 Hz output voltage, using two transport delay modules to obtain kb and kc. These values of ka, kb and kc are given to two min-max units to find the minimum and maximum of these three values which are termed min_k_abc and max_k_abc respectively. The input power factor angle phi_i is zero. The input and output frequency from Table 5.1 along with ka, kb, kc, min_k_abc, max_k_abc, phi_i and time modules are given as input to the Embedded MATLAB Function to generate the nine modulation functions for the MC switches. These nine modulation functions are then compared with a 2 kHz

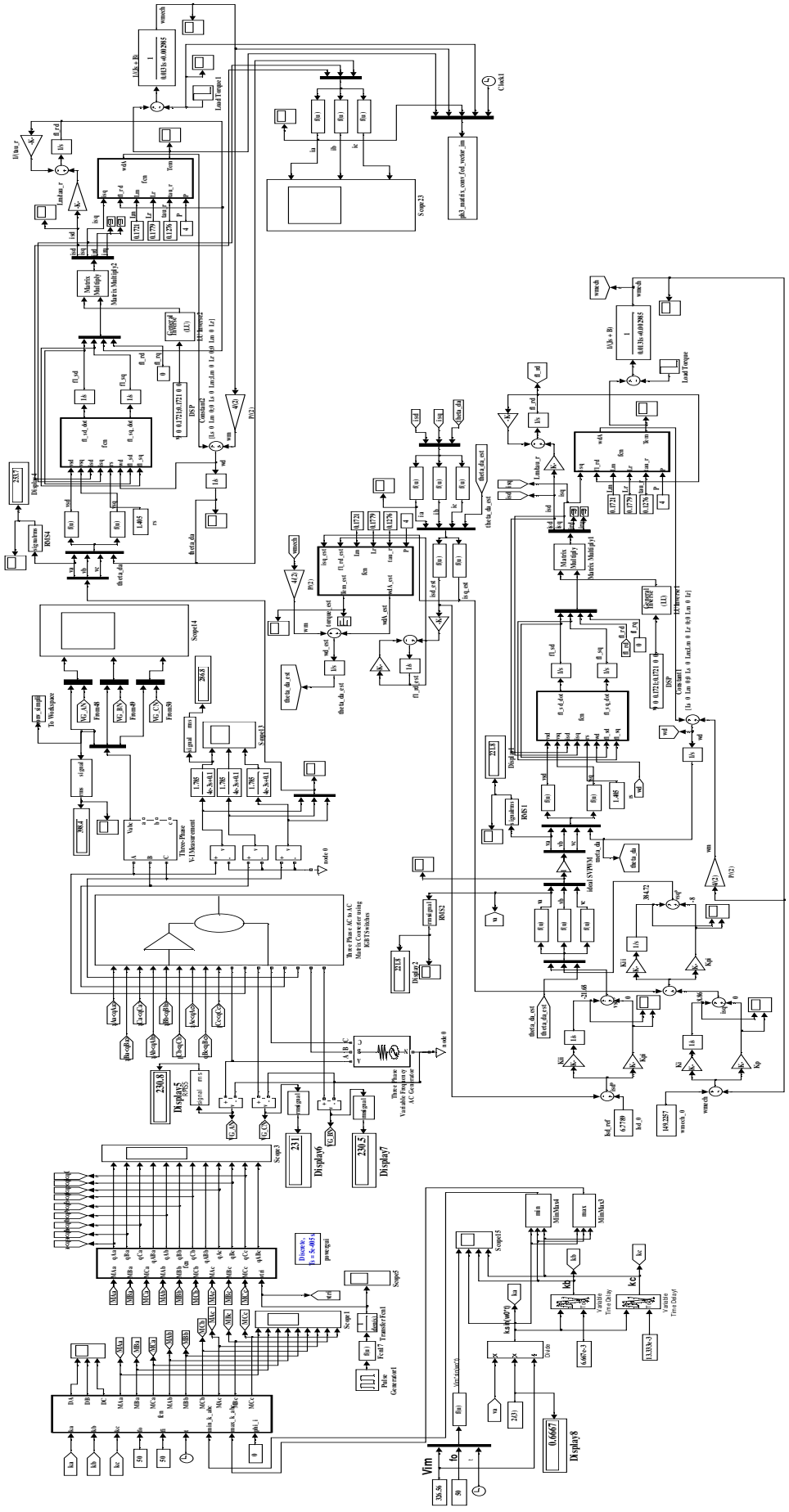


FIG. 5.17 : VECTOR CONTROLLED THREE PHASE INDUCTION MOTOR DRIVE FED BY MATRIX CONVERTER USING NED MOHAN ALGORITHM

triangle carrier and the gate pulses are generated using another Embedded MATLAB Function as explained in section 4.4.2 of Chapter IV.

5.4.6 SIMULATION RESULTS: The simulation results using SIMULINK are shown in Fig. 5.18 [51]. The ode 15s (Stiff/NDF) solver is used. From the simulation results it is seen that as the load torque varies from 30 to 15 Nw-M in 0.1 second, the Rotor E.M. torque after the initial transient settles to 15 Nw-M and the rotor speed, after the initial overshoot reaches the set point of 149.2257 mech.radians per second. Rotor torque-speed curve also confirms this value.

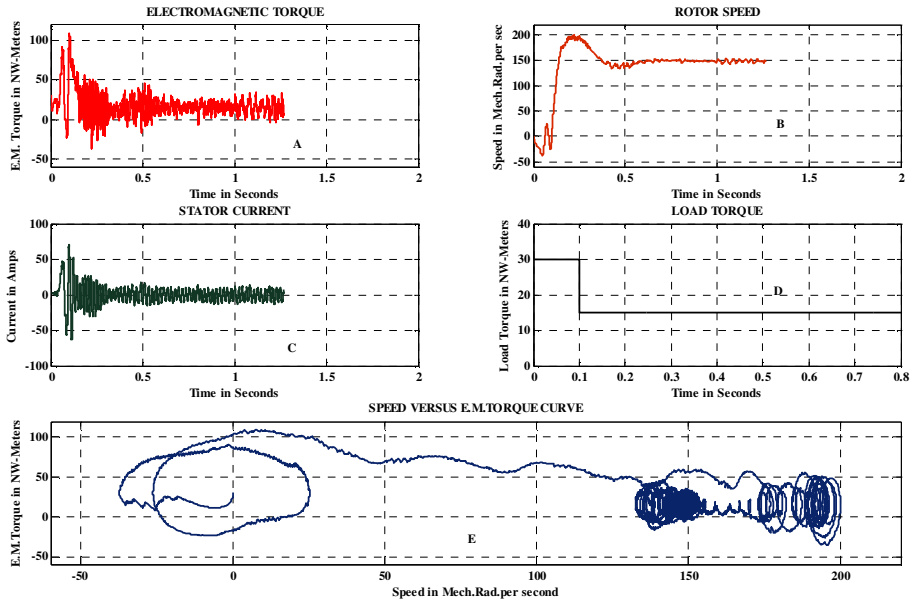


FIG. 5.18: VECTOR CONTROLLED THREE PHASE IM DRIVE FED BY MC USING NED MOHAN ALGORITHM

5.5 DISCUSSION OF RESULTS: The performance of the vector controlled IM drive when fed by MC which are switched by three carrier based modulation techniques such as by Venturini, Sunter-Clare and Ned Mohan algorithm is studied by model simulation. Although all these algorithms causes the rotor speed to reach their set point, it is seen that Sunter-Clare algorithm reaches set point of rotor speed without overshoot, Venturini algorithm with a small overshoot and Ned Mohan algorithm causing large initial overshoot.

5.6 CONCLUSIONS: It is seen by model simulation that the vector controlled three phase IM drive when fed by MC, reaches set point of rotor speed irrespective of the algorithms used for switching the MC bidirectional switches. Accurate control of speed irrespective of load variation is achieved.

A5.1 APPENDIX: The MATLAB m file for calculating the initial conditions and PI controller parameters for the speed control and current control loop of the three phase IM whose parameters are given in Table 5.1 is given below:

```
%%Calculation of Initial Conditions
%%Induction Motor Parameters
%%Narayanaswamy P.R.Iyer
%%Reference: Ned Mohan: "Advanced Electric Drives - Analysis, Control and
```

```
%%Modeling using SIMULINK", MNPERE, 2001.
Rs=1.405;  %%IM parameters in Table 5.1
Rr=1.395;
Xls=1.833446;
Xlr=1.833446;
Xm=54.07;
Jeq=0.0131;  %% Damping constant neglected being small.
p=4;  %%Number of Poles.
%%Power output Pout = 4 kVA.
% Steady State Operating Conditions
f=50; VLLrms= 400; s=0.05;                    % phase-a voltage is at its positive peak at t=0
Wsyn=2*pi*f;                                  % synchronous speed in electrical rad/s
Wm=(1-s)*Wsyn;                                % rotor speed in electrical rad/s

% Phasor Calculations
Va = VLLrms * sqrt(2)/ sqrt(3);               % Va phasor

% Space Vectors at time t=0 with stator a-axis as the reference
Vs_0 = (3/2) * Va;                            % Vs(0) space vector
Theta_Vs_0 = angle(Vs_0);                     % angle of Vs(0) space vector

% We will assume that at t=0, d-axis is aligned to the stator a-axis.  Therefore, Theta_da_0=0
Theta_da_0 = 0;
Vsd_0 = sqrt(2/3) * abs(Vs_0) * cos(Theta_Vs_0 - Theta_da_0);  %%Similar to Eq.5-26.
Vsq_0 = sqrt(2/3) * abs(Vs_0) * sin(Theta_Vs_0 - Theta_da_0);  %%Similar to Eq.5-27.

% Calculation of machine inductances
Ls = (Xls + Xm) / (2*pi*f);
Lm = Xm / (2*pi*f);
Lr = (Xlr + Xm) / (2*pi*f);
tau_r=Lr/Rr;

% Calculations of dq-winding currents
A = [Rs       -Wsyn*Ls      0        -Wsyn*Lm  ;...
    Wsyn*Ls    Rs           Wsyn*Lm    0       ;...
    0        -s*Wsyn*Lm     Rr       -s*Wsyn*Lr;...
    s*Wsyn*Lm  0           s*Wsyn*Lr  Rr];  %%Eq. 5-5 to 5-15.
Ainv = inv(A);
V_dq_0=[Vsd_0; Vsq_0; 0; 0];
I_dq_0=Ainv*V_dq_0;
Isd_0=I_dq_0(1)
Isq_0=I_dq_0(2)
Ird_0=I_dq_0(3)
Irq_0=I_dq_0(4)

% Electromagnetic Torque, which equals Load Torque in Initial Steady State
Tem_0 = (p/2) * Lm * (Isq_0 * Ird_0 - Isd_0 * Irq_0)
TL_0 = Tem_0

% Wmech = rotor speed in actual rad/s
Wmech_0=(2/p)*Wm

% Inductance matrix M in Eq. 5-24
M = [Ls 0  Lm 0 ;...
    0  Ls 0  Lm;...
    Lm 0  Lr 0 ;...
    0  Lm 0  Lr];

% dq winding Flux Linkages with the d-axis aligned with the stator a-axis
fl_dq_0 = M * [Isd_0; Isq_0; Ird_0; Irq_0];
```

```
fl_sd_0 = fl_dq_0(1)
fl_sq_0 = fl_dq_0(2)
fl_rd_0 = fl_dq_0(3)
fl_rq_0 = fl_dq_0(4)
[thetar, fl_r_dq_0]=cart2pol(fl_rd_0, fl_rq_0)
[thetas, fl_s_dq_0]=cart2pol(fl_sd_0, fl_sq_0)
[theta_Is_dq, Is_dq_0]=cart2pol(Isd_0, Isq_0)
[theta_Vs_dq, Vs_dq_0]=cart2pol(Vsd_0, Vsq_0)

% d-axis is now aligned with the rotor flux which results in the following new values:
fl_rd_0=fl_r_dq_0       %fl_rq_0 equals zero
[fl_sd_0, fl_sq_0]=pol2cart(thetas-thetar, fl_s_dq_0)
[Isd_0, Isq_0]=pol2cart(theta_Is_dq-thetar, Is_dq_0)
[Vsd_0, Vsq_0]=pol2cart(theta_Vs_dq-thetar, Vs_dq_0)

% Calculations for the controller
Wc=25; % crossover freq in rad/s
k=(p/2)*(Lm*Lm/Lr)*Isd_0;
PM=60*pi/180;                       % phase margin in rad/s
Wc_kp_by_ki=tan(PM);                % kp and ki are shown in Fig. 5-8
ki=Wc*Wc*Jeq/(k*sqrt(1+(tan(PM)^2)))
kp=ki*Wc_kp_by_ki/Wc

% check to show that at Wc,  GOLmag=1 and GOLang= (-180 degrees + phase margin of 60 degrees)
GOL=(kp+ki/(j*Wc))*k/(Jeq*j*Wc)         % open-loop transfer function
GOLmag=abs(GOL)
GOLang=angle(GOL)*180/pi

% PI in current loop
sigma=1-Lm*Lm/(Ls*Lr)       % Eq. 5-40
Wci=10*Wc                   % Current-loop bandwidth is ten times that of the speed loop
PMi=PM
Wci_kpi_by_kii=tan(PMi-pi/2+atan(Wci*Ls*sigma/Rs))
kii=Wci*sqrt(Rs*Rs+(Wci*Ls*sigma)^2)/sqrt(Wci_kpi_by_kii^2+1)
kpi=Wci_kpi_by_kii*kii/Wci

% check to show that at Wci,  GOLimag=1 and GOLiang= (-180 degrees + phase margin of 60
degrees)
GOLi=(kpi+kii/(j*Wci))/(Rs+j*Wci*Ls*sigma)
GOLimag=abs(GOLi)
GOLiang=angle(GOLi)*180/pi
```

The simulation results of the above MATLAB m file are given below:

```
Isd_0 =
   12.8478

Isq_0 =
   -8.0860

Ird_0 =
  -13.0734

Irq_0 =
    1.2962

Tem_0 =
   30.6555

TL_0 =
   30.6555
```

```
Wmech_0 =
  149.2257

fl_sd_0 =
    0.0362

fl_sq_0 =
   -1.2158

fl_rd_0 =
   -0.1151

fl_rq_0 =
   -1.1610

thetar =
   -1.6696

fl_r_dq_0 =
    1.1667

thetas =
   -1.5411

fl_s_dq_0 =
    1.2163

theta_Is_dq =
   -0.5617

Is_dq_0 =
   15.1806

theta_Vs_dq =
     0

Vs_dq_0 =
  400.0000

fl_rd_0 =
    1.1667

fl_sd_0 =
    1.2063

fl_sq_0 =
    0.1559

Isd_0 =
    6.7789

Isq_0 =
   13.5829

Vsd_0 =
  -39.4661

Vsq_0 =
  398.0483
```

```
ki =
    1.8139

kp =
    0.1257

GOL =
  -0.5000 - 0.8660i

GOLmag =
     1

GOLang =
 -120.0000

sigma =
    0.0645

Wci =
   250

PMi =
    1.0472

Wci_kpi_by_kii =
    0.6724

kii =
  662.9626

kpi =
    1.7831

GOLi =
  -0.5000 - 0.8660i

GOLimag =
    1.0000

GOLiang =
 -120.0000
--------------------------------------------------
```

Chapter VI

Real Time Hardware-in-the-Loop Simulation of A Three Phase AC to Single Phase AC Matrix Converter

6.1 INTRODUCTION: Hardware in the Loop (HIL) is a technique used in the development and testing of complex real time Embedded Systems. HIL simulation provides an effective platform by adding the complexity of the plant under control to the test platform. The complexity of the plant under control is included in test and development by adding a mathematical representation or model of all related system under consideration [55]. These mathematical representations are referred to as the "plant simulation". The embedded system to be tested interacts with this plant simulation [55]. The ability to design and automatically test power electronics systems with HIL simulations will reduce development cycle, increase efficiency, improve reliability and safety of these systems for large number of applications [55]. There are at least three strong reasons for using hardware-in-the-loop simulation for power electronics, namely: 1) reduction of development cycle, 2) demand to extensively test control hardware and software in order to meet safety and quality requirements, and 3) need to prevent costly and dangerous failures [55].

6.2 MODEL OF THREE PHASE AC TO SINGLE PHASE AC MATRIX CONVERTER: The

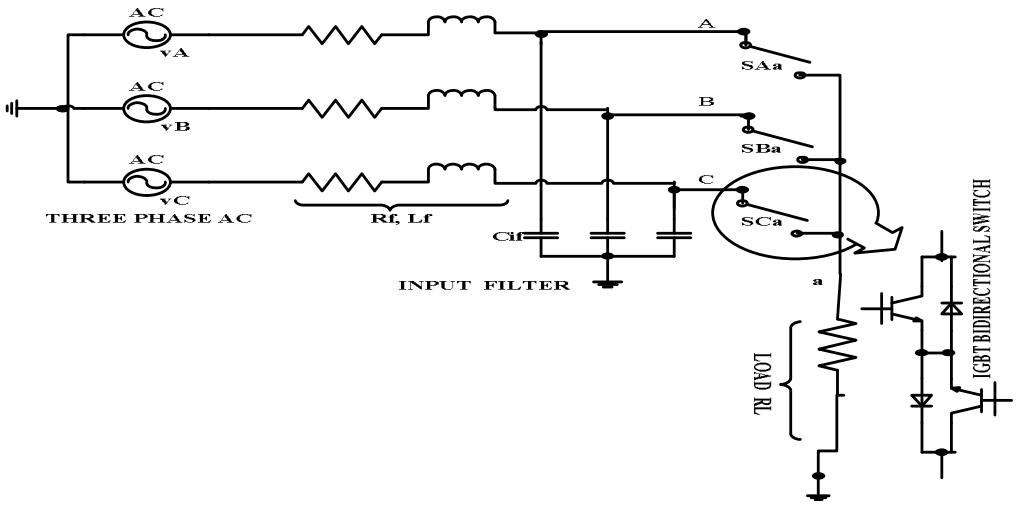


FIG. 6.1: THREE PHASE AC TO SINGLE PHASE AC MATRIX CONVERTER

model of the three phase AC to Single phase AC Matrix converter (MC) is developed using Venturini modulation algorithm assuming unity input phase displacement factor [1-4]. A schematic of the three phase AC to single phase AC MC is shown in Fig. 6.1. Here there are three bidirectional switches connected to each input phase A, B, C and all these switches are connected to one output phase a in series with a resistive load. The 3 X 1 matrix converter shown in Fig.6.1 connects the three phase ac source to the single phase load. The switching Function for a 3 X 1 matrix converter can be defined as follows [4-5]:

$$S_{Kj} = \begin{cases} 1 \ when \ S_{Kj} \ \ is \ closed \\ 0 \ when \ S_{Kj} \ \ is \ open \end{cases} \qquad (6.1)$$
$$K \in \{A, B, C\} \ and \ j \in \{a\}$$

The above constraint can be expressed in the following form:

$$S_{Aj} + S_{Bj} + S_{Cj} = 1 \qquad (6.2)$$
$$j \in \{a\}$$

Here the input-output voltage relation simplifies to the equation 6.3 below:

$$[v_a] = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \end{bmatrix} * \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} \qquad (6.3)$$

Similarly the input-output current relation can be expressed as in equation 6.4 below:

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} S_{Aa} \\ S_{Ba} \\ S_{Ca} \end{bmatrix} * [i_a] \qquad (6.4)$$

where va and iA, iB, iC are the output voltage and input currents respectively.

To determine the behaviour of the MC at output frequencies well below the switching frequency, a modulation duty cycle can be defined for each switch. The modulation duty cycle M_{Kj} for the switch S_{Kj} in Fig.6.1 is defined as in equation 6.5 below.

$$M_{Kj} = \frac{t_{Kj}}{T_S} \qquad (6.5)$$
$$K \in \{A, B, C\} \ and \ j \in \{a\}$$

where t_{Kj} is the on time for the switch S_{Kj} between input phase $K \in \{A, B, C\}$ and $j \in \{a\}$ and T_S is the period of the PWM switching signal or sampling period. In terms of the modulation duty cycle, equations 6.2, 6.3 and 6.4 can be rewritten as given below:

$$[v_a] = \begin{bmatrix} M_{Aa} & M_{Ba} & M_{Ca} \end{bmatrix} * \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} \qquad (6.6)$$

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} M_{Aa} \\ M_{Ba} \\ M_{Ca} \end{bmatrix} * [i_a] \qquad (6.7)$$

$$M_{Aj} + M_{Bj} + M_{Cj} = 1 \qquad (6.8)$$
$$j \in \{a\}$$

The Venturini modulation algorithm for a three phase AC to three phase AC MC is already presented in Section 3.2 of Chapter III. For unity input phase displacement factor, the modulation function can be expressed as in equation 6.9 below:

$$M_{Kj} = \frac{t_{Kj}}{T_s} = \left[\frac{1}{3} + \frac{2v_K.v_j}{3.V_{im}^2}\right] \qquad (6.9)$$
$$for \ K = A, B, C \ and \ j = a$$

6.3 MODEL DEVELOPMENT: To study the behaviour of the three phase AC to single phase AC MC using Venturini Modulation algorithm assuming unity input phase displacement factor, a model of this matrix converter is developed in SIMULINK [51]. The data shown in Table 6.1 are used to develop the model. The MC switching is developed based on equations 6.9. A resistive load of 4700 Ohms is used.

TABLE 6.1: Model Parameters

Sl.No.	Modulation Index q	RMS Line to Neutral Input Voltage (Volts)	Input Frequency Hz	Output Frequency Hz	Carrier Frequency kHz
1	0.5	123	50	50	5

6.3.1 MODEL OF THREE PHASE AC TO SINGLE PHASE AC MC USING VENTURINI ALGORITHM: The model of the three phase AC to single phase AC MC is developed using Venturini second method discussed in Section 3.3.3 of Chapter III. Unity input Phase Displacement factor is assumed. The model is developed using SIMULINK [51]. The data shown in Table 6.1 is used to develop the model. The model simulation is carried out for both three phase sine wave input voltages as well as for three phase square wave input voltages, for the parameters in Table 6.1. The model is shown in Fig. 6.2. The bidirectional switches are shown for both three phase sine wave and square wave inputs. The gate pulse for the three bidirectional switches are developed using Embedded MATLAB function, saw-tooth carrier and logic gates. Embedded MATLAB function is used to realize equations 3.9, 3.11 of Chapter III and the three modulation functions for output phase a, defined in equation 6.9. Using these three modulation functions and a 5 kHz saw-tooth carrier as inputs, gate timing pulses are generated using comparators and logic gates for the three bidirectional switches, as shown in Fig. 6.2. The three phase sine wave input has a RMS value of 123 Volts between line and neutral and frequency 50 Hz. In addition, model is shown to generate three phase 123 Volts (RMS), 50 Hz square wave input, using three threshold switches. When the second input to each of the threshold switches which are three phase 50 Hz sine wave voltages crosses zero and goes positive and negative, the output of the threshold switch goes +123 Volts and -123 Volts respectively. The modulation index and output frequency are set to 0.5 and 50 Hz respectively.

6.3.2 SIMULATION RESULTS: The simulation of the above model was carried out in SIMULINK [51]. The ode15S(Stiff/NDF) solver is used in both cases. Simulation results for three phase 50 Hz square wave input voltage and three phase sine wave input voltage are discussed below:

(a) Response to Three Phase Square Wave Input Voltage: The simulation result of the output voltage for the three phase 123 Volts(RMS), 50 Hz square wave input is shown in Fig. 6.3. The output voltage across the load resistor is found to be 123 Volts(RMS) which is shown in Fig. 6.5. The three Phase 50 Hz square wave input voltage is shown in Fig. 6.4 and its RMS value is shown in Fig. 6.6.

(b) Response to Three Phase Sine Wave Input Voltage: The response to the three phase 50 Hz sine wave input voltage is shown in Fig. 6.7 which shows the three phase sine wave input voltage, the output voltage across the resistive load and load current.

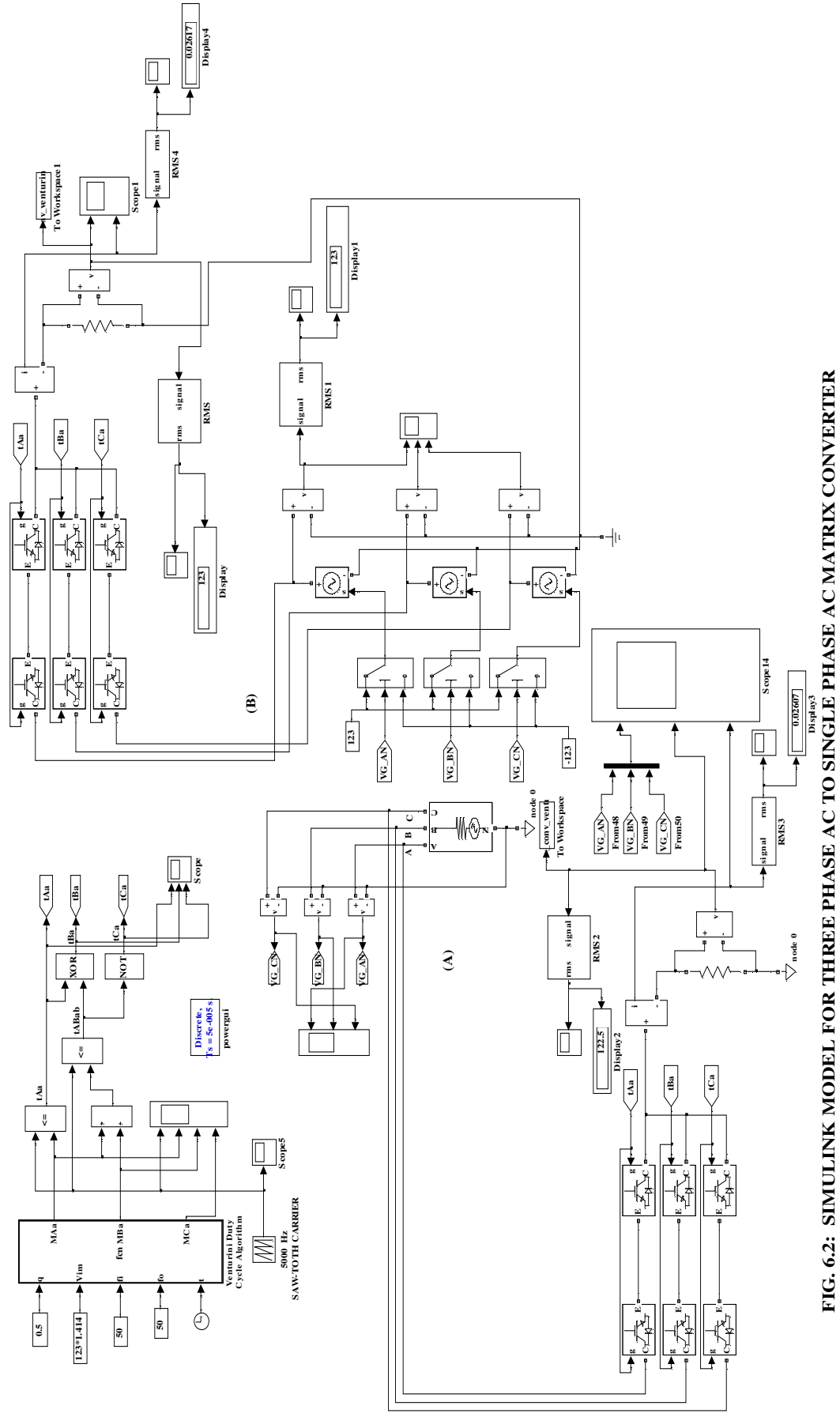


FIG. 6.2: SIMULINK MODEL FOR THREE PHASE AC TO SINGLE PHASE AC MATRIX CONVERTER
(A): Three Phase Sine Wave Input; (B): Three Phase Square Wave Input

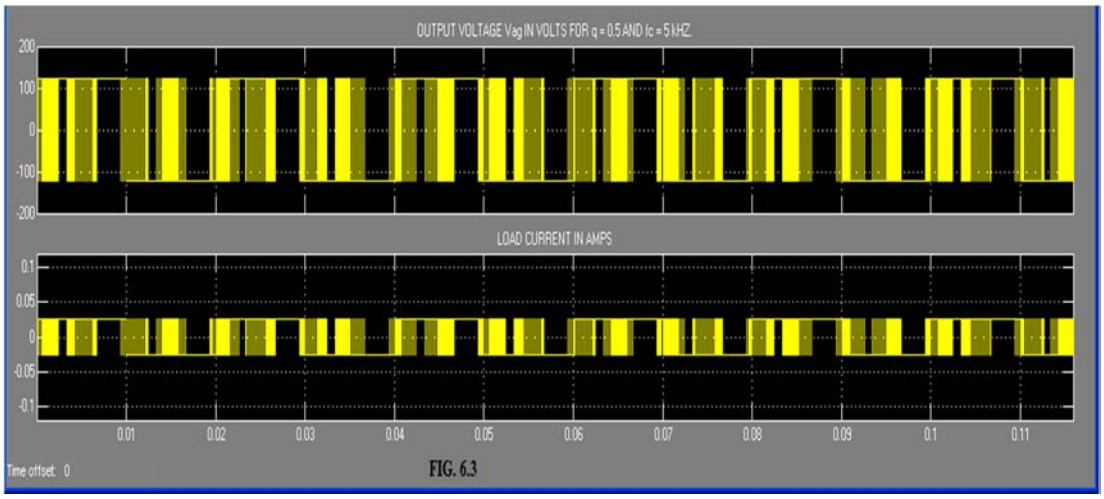


FIG. 6.3

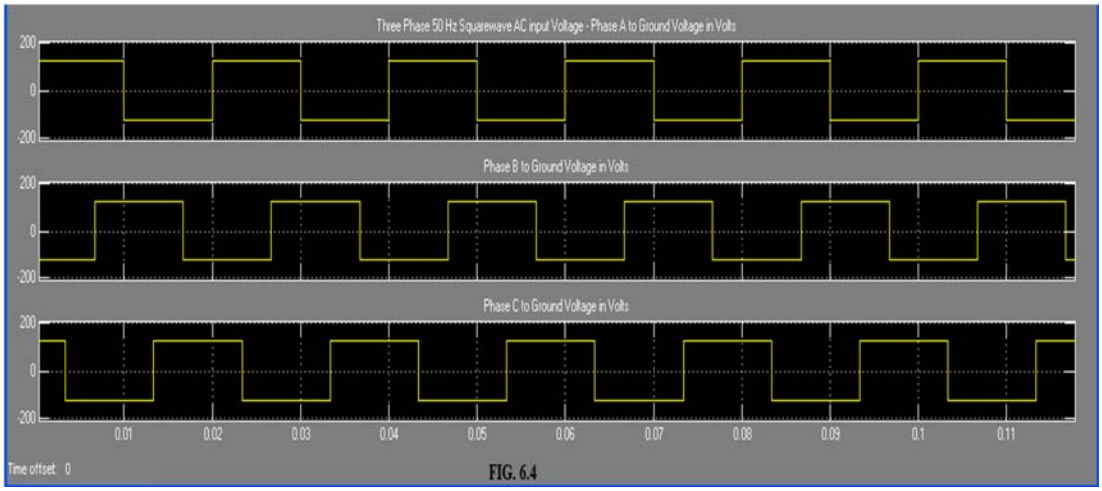


FIG. 6.4

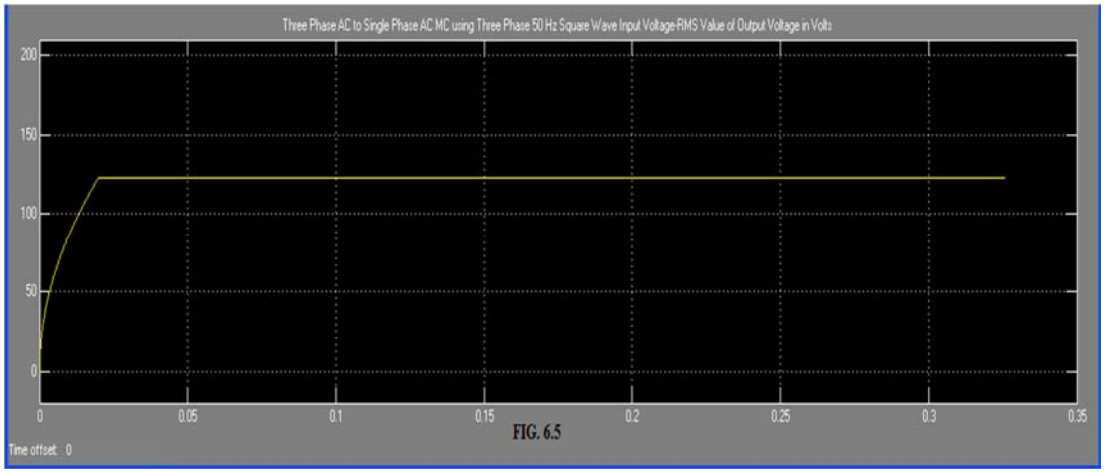


FIG. 6.5

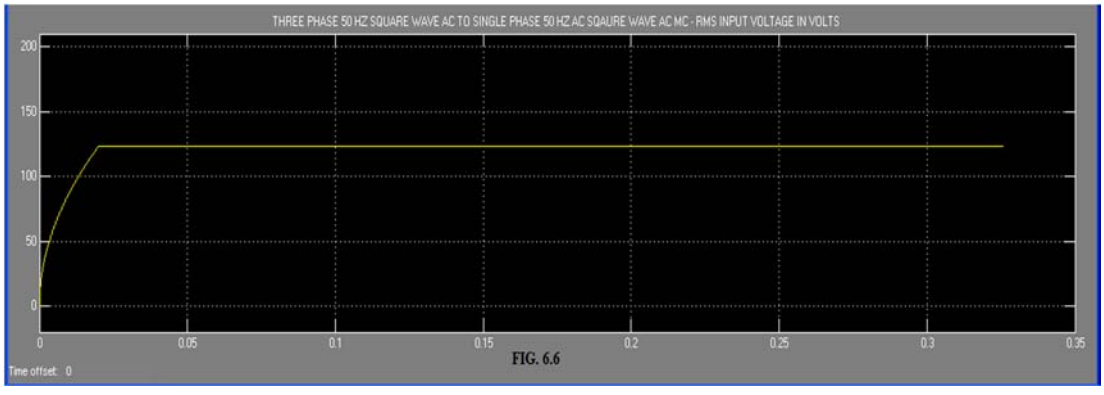


FIG. 6.6

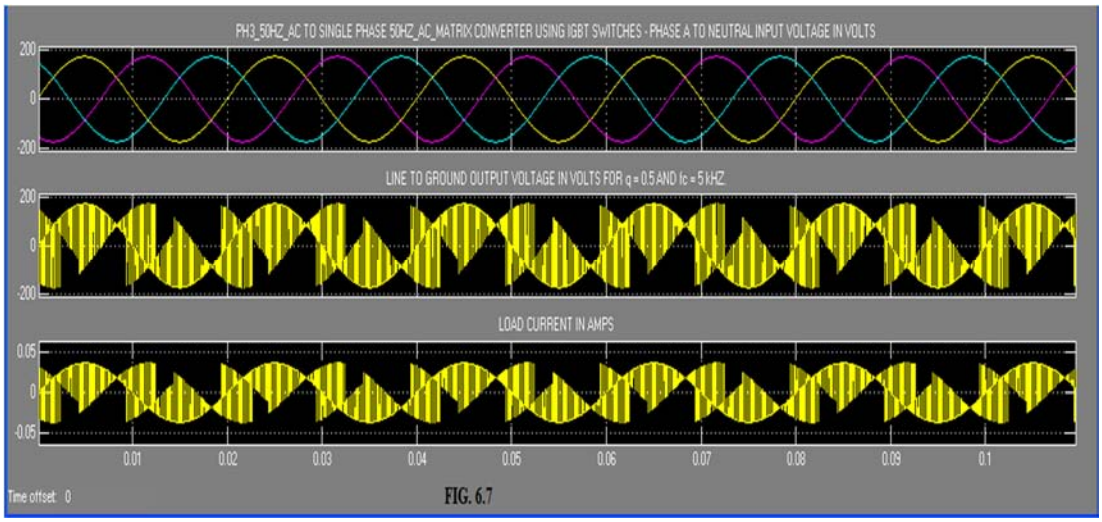


FIG. 6.7

Simulation results for the three phase 50 Hz square wave input voltage are tabulated in Table 6.2.

TABLE 6.2: SIMULINK Model Simulation Results

Sl.No.	Input Voltage			Output Voltage			Modulation Index
	Nature	Freeqency	RMS Value	Nature	Frequency	RMS Value	
1)	Three Phase Square Wave	50 Hz	123 V (L to N)	Single Phase Square Wave	50 Hz	123 V (L to G)	0.5

6.4 EXPERIMENTAL VERIFICATION USING DSPACE HARWARE CONTROLLER BOARD: The first experiment is developed using dSPACE DS1104 hardware controller board to study the gate drive waveforms for three phase 50 Hz AC to single phase 50 Hz AC MC [54]. The experimental set up is shown in the photograph in Fig. 6.8. The method of interfacing the


FIG. 6.8

dSPACE Experimental set up for the Gte Drive of a 3 X 1 Matrix Converter

dSPACE hardware controller board to the SIMULINK model of three phase AC to single phase AC MC is shown in Fig. 6.9. The DS1104 has a main processor MPC8240 and a slave DSP TMS320F240 [54]. In Fig. 6.9, the Embedded MATLAB Function generates the three modulation functions MAa, MBa and MCa. The comparator block, A<=B provides output HIGH when saw-tooth carrier VSAW input given to node A is less than or equal to the input given to node B. The comparator connected to VSAW and MAa produces output tAa and that connected to VSAW and

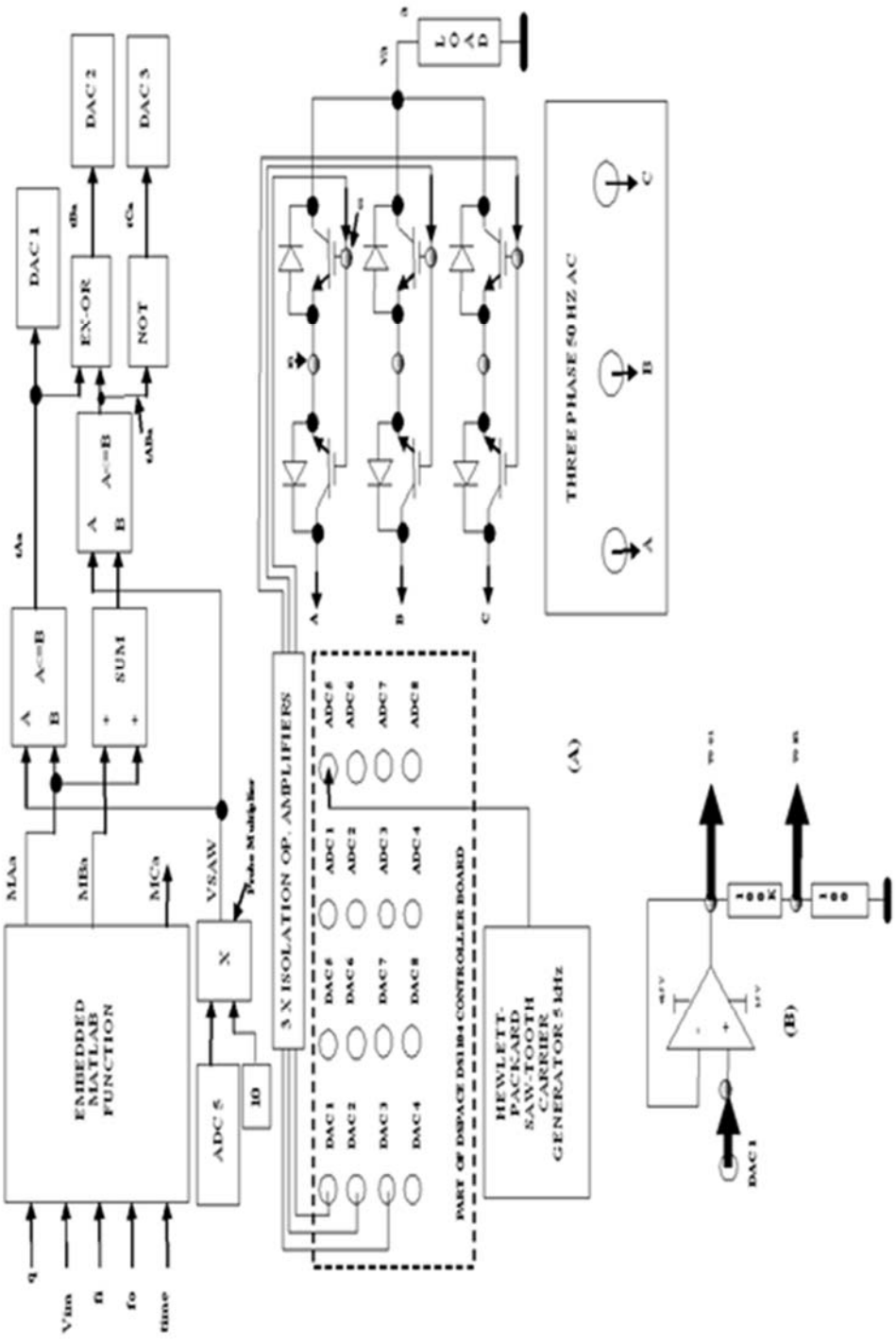


FIG. 6.9: DSPACE DS1104 HARWARE CONTROLLER BOARD INTERFACE TO THREE PHASE AC TO SINGLE PHASE AC MATRIX CONVERTER SIMULINK MODEL

(MAa+MBa) produces output tABa. The outputs tAa and tABa are connected to EXCLUSIVE-OR gate to obtain tBa and the output tABa is inverted using a NOT gate to obtain tCa. tAa, tBa and tCa form the gate pulses for the bidirectional switches connected between phases Aa, Ba and Ca respectively in Fig. 6.1. The photograph of the waveform of the gate drive obtained for the above experiment is shown in Fig. 6.10 and that using control desk is shown in Fig. 6.11.

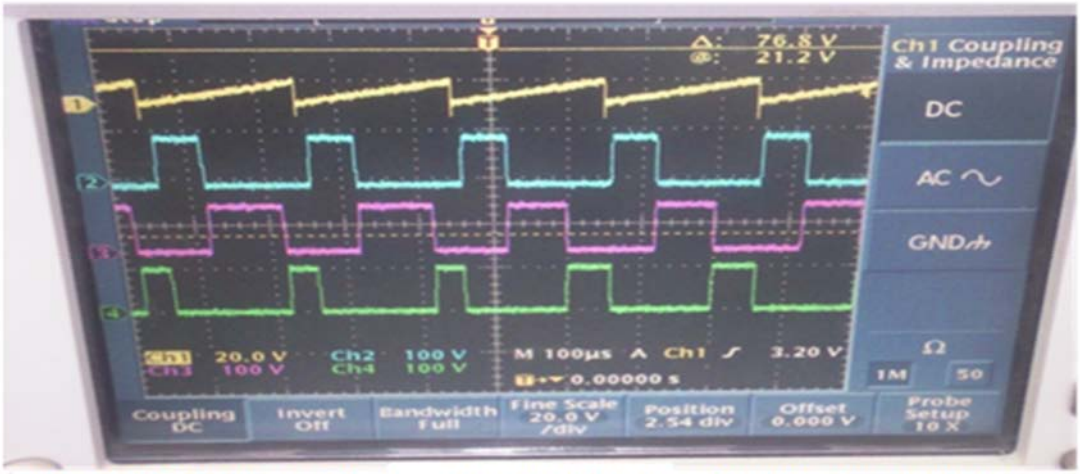


FIG. 6.10 **Oscilloscope Waveform of Saw-Tooth Carrier and Gate Drive for a 3 X 1 MC**

FIG. 6.11 **Control Desk Waveform of Saw-Tooth Carrier and the Gate Drive for a 3 X 1 MC**

The second experiment is developed to observe the performance of an actual Three phase 50 Hz AC to Single Phase AC MC when switching of bidirectional switches is done using the above gate pulse drive. The hardware set up for this experiment is shown in Fig. 6.12. Fig.6.9(B) which is a high input impedance op.amp. shows the method of connecting the output of DAC 1 of DS1104 hardware controller board to the bidirectional switch. Similar connections apply to DAC 2 and DAC 3 of DS1104 hardware controller board. All IGBTS used in the experiment were STGP14NC60KD with a voltage and current rating of 600 V, 25 A. This MC board is shown in Fig. 6.13. The Texas Instruments quad TL084 op.amp is used for isolation as this has a high input impedance of the order of 10^{12} Ohms and slew rate of the order of 13 V/μsec. Although Venturini algorithm is developed for three phase sine wave AC input voltage only, in this experiment, a three phase 50 Hz square wave AC input voltage is used. The magnitude of the input voltage used is 123 Volts (RMS) line to neutral.

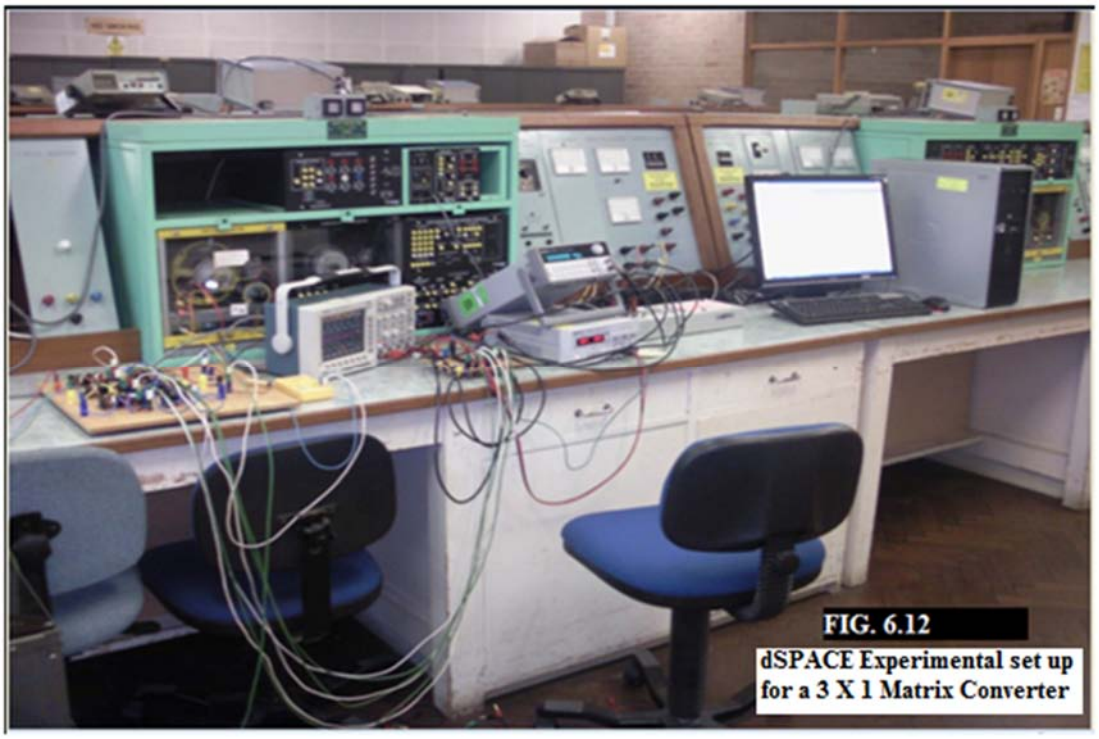


FIG. 6.12
dSPACE Experimental set up for a 3 X 1 Matrix Converter

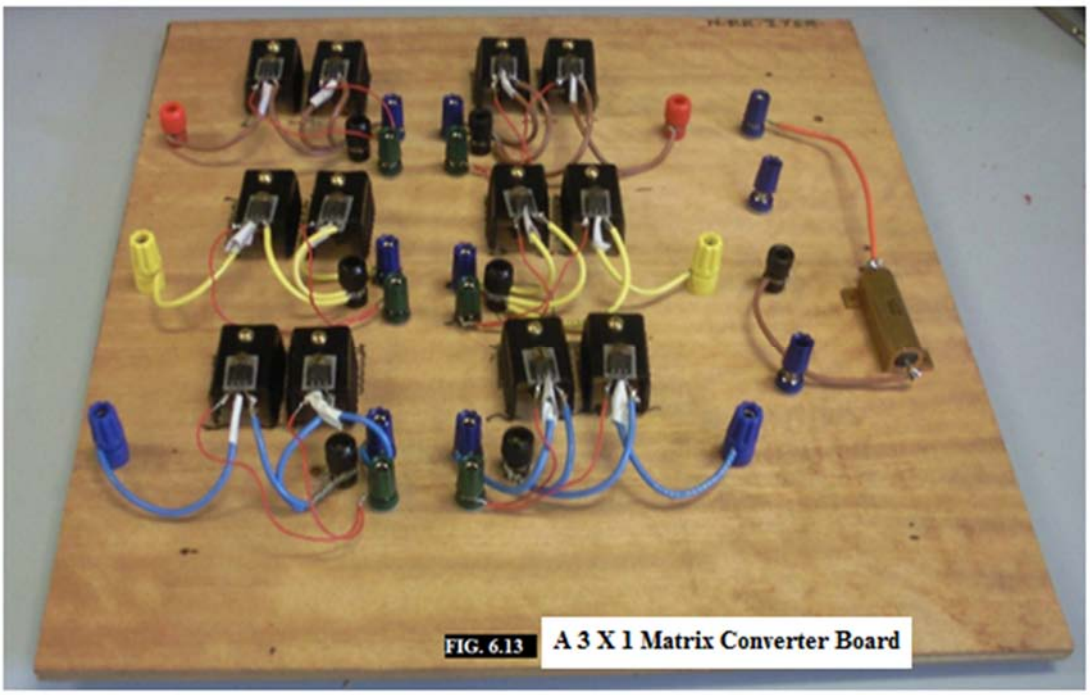


FIG. 6.13 A 3 X 1 Matrix Converter Board

The waveform of this input voltage for the reference phase is shown in Fig. 6.14 in both the channels. The gate drive pattern obtained is already shown in Fig. 6.10 and 6.11. The output voltage observed across the load resistor is found to be 86 Volts(RMS) and this waveform is shown in Fig. 6.15. In this experiment a modulation index of 0.5 is used. The dSPACE hardware controller board experimental result is tabulated in Table 6.3.

6.5 DISCUSSION OF RESULTS: The Real time Hardware in the Loop simulation of the above Three Phase AC to Single Phase AC MC is carried out using dSPACE [54]. The real time platform is

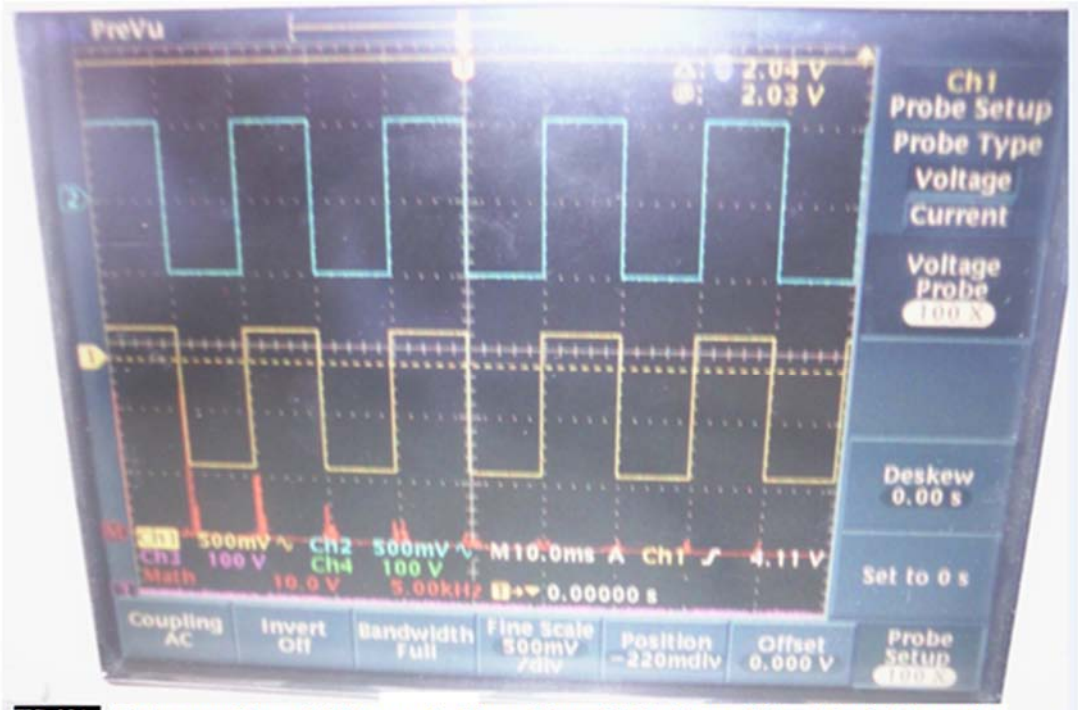


FIG. 6.14 Reference Phase A Voltage of a Three Phase 50 Hz Square Wave (Both Channels)

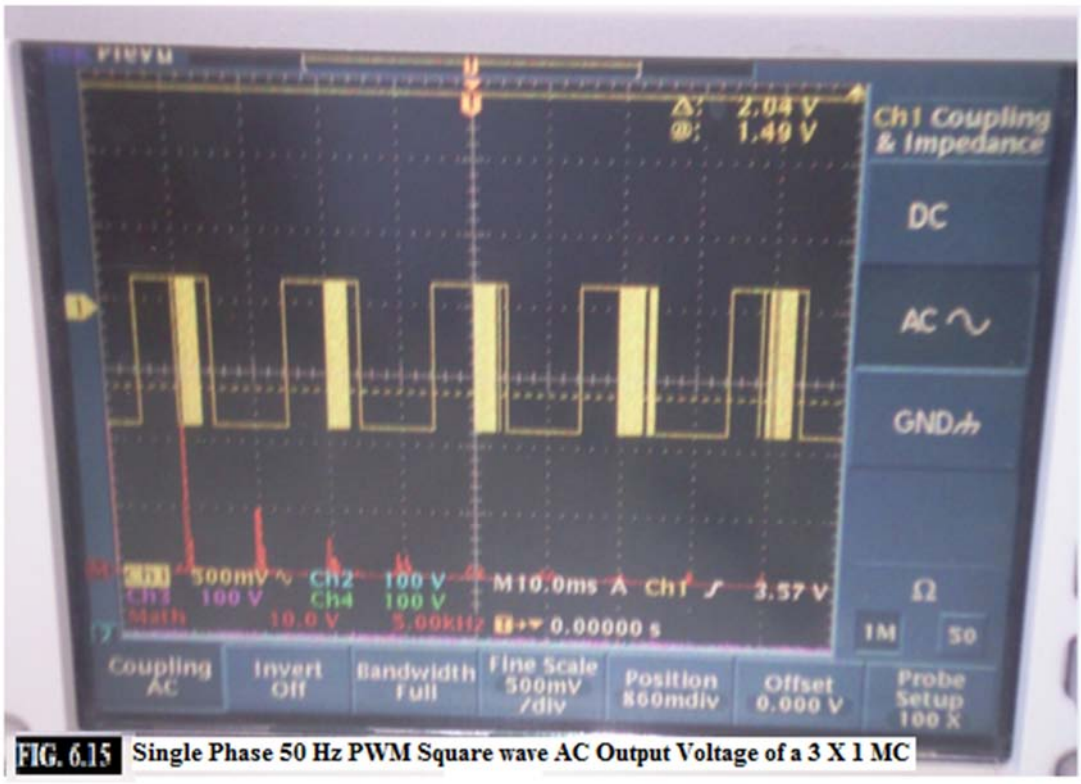


FIG. 6.15 Single Phase 50 Hz PWM Square wave AC Output Voltage of a 3 X 1 MC

TABLE 6.3: dSPACE Experimental Results

Sl.No.	Input Voltage			Output Voltage			Modulation Index
	Nature	Freeqency	RMS Value	Nature	Frequency	RMS Value	
1)	Three Phase Square Wave	50 Hz	123 V (L to N)	Single Phase Square Wave	50 Hz	86 V (L to G)	0.5

developed using dSPACE DS 1104 hardware controller board. In this dSPACE experiment, a three phase 50 Hz square wave AC from a three phase inverter is used as the input. A resistive load is used for this experiment. The experimental results obtained are shown. The experimental results are verified by simulation. Venturini modulation algorithm assuming unity input phase displacement factor is used for the real time experiment on the above MC and also for the verification by simulation.

6.6 CONCLUSIONS: The waveform observed using oscilloscope almost well agree with the one obtained by simulation of the model. However the RMS value of the output voltage by experiment has a variation of 30% compared to the one obtained by simulation of the model. The bidirectional IGBT switch models use RC snubber for convergence of simulation, whereas no such snubber is present in the IGBTs used for the experiment.

Chapter VII

Three Phase AC to Three Phase AC Capacitor Clamped Multilevel Matrix Converter

7.1 INTRODUCTION: Multilevel technology is a good solution for medium and high voltage power conversion [18-22]. There are three kinds of multilevel converters namely diode clamped [20], capacitor clamped [21-22] and cascade [23]. Among them, capacitor clamped multilevel converter is the most suitable topology for direct AC to AC conversion [21-22]. This chapter describes the multilevel matrix converter with a capacitor clamped or flying capacitor or multicell topology [18-19]. Venturini algorithm is used for generating gate pulses for multilevel matrix converter, the application of which is different from the conventional single cell matrix converter. Simulation results using the software SIMULINK are provided. The simulation results by SIMULINK are reviwed or re-examined and additional supplementary simulation results are provided using the software PSCAD.

7.2 MULTILEVEL MATRIX CONVERTER WITH THREE FLYING CAPACITORS PER OUTPUT PHASE: The three phase capacitor clamped multilevel matrix converter (MMC) with three flying capacitors (FC) per output phase is shown in Fig. 7.1 [18-19]. The IGBT switches in Fig. 7.1 are bidirectional. The analysis is given below:

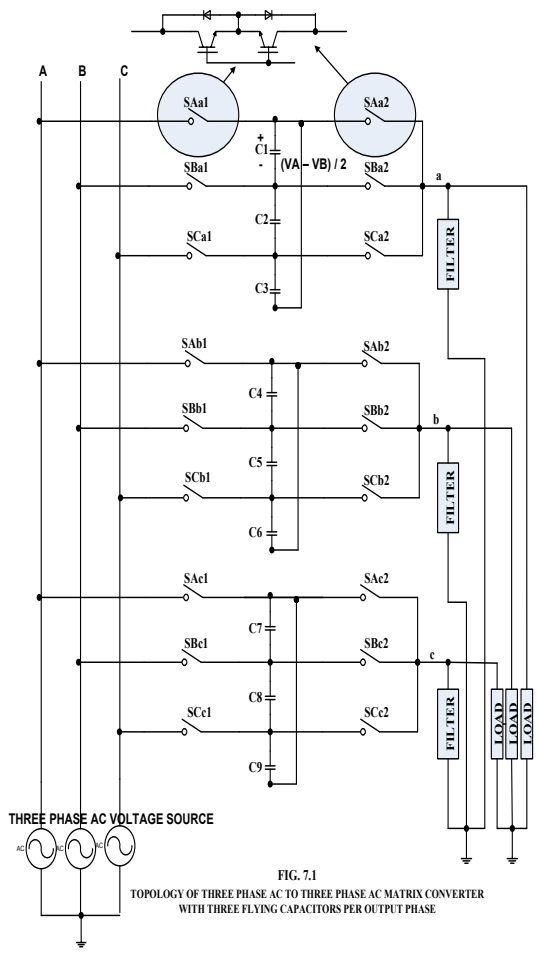


FIG. 7.1
TOPOLOGY OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER WITH THREE FLYING CAPACITORS PER OUTPUT PHASE

Consider switches SAa1, SAa2, SBa1 and SBa2 and capacitor C1. Let all the four switches be identical with off resistance Roff. With all four switches off, applying Kirchoff's law to the above four switches with C1 connected to supply V_{AB}, we can express the voltage V_{c1} across C1 as follows:

$$V_{c1} = \frac{V_{AB}}{4*R_{off}} * 2 * R_{off} = \frac{(V_A - V_B)}{2} \qquad (7.1)$$

where V_{c1} has the polarity positive at the top and negative at the bottom plate. The same analysis holds good for other flying capacitors C2 to C9. Thus $V_{c1} = V_{c4} = V_{c7}$, $V_{c2} = V_{c5} = V_{c8}$ and $V_{c3} = V_{c6} = V_{c9}$.

In Fig. 7.1, for the above switch combinations, Table 7.1 is valid. A detailed table for output

phase a is shown in Table 7.2 [18-19]. Capacitance of the flying capacitor is selected using equation 2 below:

$$C = \frac{I_o}{\Delta V_c \,.\, p.\, f_{sw}} \qquad (7.2)$$

where Io is the peak value of load current, p is the number of cells per output phase and f_{sw} is the switching frequency and ΔVc is the flying capacitor percentage voltage ripple [18-19]. The switching function for the bidirectional switches in Fig. 7.1 can be expressed as in equation 7.3 below:

TABLE 7.1: Truth Table PH3 MMC with Three FC
1 = Switch closed On ; 0 = Switch open Off

Sl. No.	SAa1	SAa2	SBa1	SBa2	Output Voltage va
1	1	1	0	0	VA
2	0	0	1	1	VB
3	1	0	0	1	$(VA + VB)/2$
4	0	1	1	0	$(VA + VB)/2$

TABLE 7.2: Complete Truth Table for PH3 MMC with Three FC
1 = Switch closed on; 0 = Switch open off

Sl. No.	SAa1	SAa2	SBa1	SBa2	SCa1	SCa2	Output Voltage va
1	1	1	0	0	0	0	VA
2	1	0	0	1	0	0	$(VA + VB)/2$
3	0	1	1	0	0	0	$(VA + VB)/2$
4	0	0	1	1	0	0	VB
5	0	0	1	0	0	1	$(VB + VC)/2$
6	0	0	0	1	1	0	$(VB + VC)/2$
7	0	0	0	0	1	1	VC
8	0	1	0	0	1	0	$(VA + VC)/2$
9	1	0	0	0	0	1	$(VA + VC)/2$

$$\left.\begin{aligned} S_{ijk} &= \begin{cases} 0 \;\; when \;\; switch \;\; open \\ 1 \;\; when \;\; switch \;\; closed \end{cases} \\ S_{Ajk} + S_{Bjk} + S_{Cjk} &= 1 \end{aligned}\right] \qquad (7.3)$$

$i \in Input\ Phase \quad A, B, C;\ j \in Output\ Phase \quad a, b, c \quad and \quad k = Switch\ Column\ Count \quad 1,\ 2$

The modelling equation referring to Table 7.2 for the output voltage can be expressed as in equation 7.4 and referring to Fig. 7.1, the modelling equation for the three phase input currents can be expressed as in equation 7.5 below:

7.3 CONTROL OF MULTILEVEL MATRIX CONVERTER WITH THREE FLYING CAPACITORS PER OUTPUT PHASE BY VENTURINI METHOD: Let the input and output voltages be expressed as in equation 3.9 and 3.11 in Chapter III. For unity input phase displacement factor, the nine modulation functions for a three phase AC to three phase AC conventional matrix converter is given in equation 3.17 and its validity for three phase cosine wave and sine wave input and output voltages is proved in A3.3 Appendix in Chapter III. Here the modified modulation function assuming unity input phase displacement factor for the three phase MMC with eighteen bidirectional switches shown in Fig. 7.1, is given in equation 7.6 below:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} & S_{C1} & S_{C2} & S_{C3} \\ S_{Ab} & S_{Bb} & S_{Cb} & S_{C4} & S_{C5} & S_{C6} \\ S_{Ac} & S_{Bc} & S_{Cc} & S_{C7} & S_{C8} & S_{C9} \end{bmatrix} * \begin{bmatrix} v_A \\ v_B \\ v_C \\ (v_A + v_B)/2 \\ (v_C + v_B)/2 \\ (v_A + v_C)/2 \end{bmatrix}$$

where

$S_{Aa} = S_{Aa1} \cap S_{Aa2}; S_{Ba} = S_{Ba1} \cap S_{Ba2}; S_{Ca} = S_{Ca1} \cap S_{Ca2}$

$S_{C1} = S_{Aa1} \cap S_{Ba2} \cup S_{Ba1} \cap S_{Aa2}; S_{C2} = S_{Ba1} \cap S_{Ca2} \cup S_{Ca1} \cap S_{Ba2}; S_{C3} = S_{Aa1} \cap S_{Ca2} \cup S_{Ca1} \cap S_{Aa2}$

$S_{Ab} = S_{Ab1} \cap S_{Ab2}; S_{Bb} = S_{Bb1} \cap S_{Bb2}; S_{Cb} = S_{Cb1} \cap S_{Cb2}$

$S_{C4} = S_{Ab1} \cap S_{Bb2} \cup S_{Bb1} \cap S_{Ab2}; S_{C5} = S_{Bb1} \cap S_{Cb2} \cup S_{Cb1} \cap S_{Bb2}; S_{C6} = S_{Ab1} \cap S_{Cb2} \cup S_{Cb1} \cap S_{Ab2}$

$S_{Ac} = S_{Ac1} \cap S_{Ac2}; S_{Bc} = S_{Bc1} \cap S_{Bc2}; S_{Cc} = S_{Cc1} \cap S_{Cc2}$

$S_{C7} = S_{Ac1} \cap S_{Bc2} \cup S_{Bc1} \cap S_{Ac2}; S_{C8} = S_{Bc1} \cap S_{Cc2} \cup S_{Cc1} \cap S_{Bc2}; S_{C9} = S_{Ac1} \cap S_{Cc2} \cup S_{Cc1} \cap S_{Ac2}$

1= Switch closed

0= Switch open

$\cap$ = *Logical AND operator*

$\cup$ = *Logical OR operator* (7.4)

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} (S_{Aa} \cup S_{ABa} \cup S_{ACa}) & (S_{Ab} \cup S_{ABb} \cup S_{ACb}) & (S_{Ac} \cup S_{ABc} \cup S_{ACc}) \\ (S_{Ba} \cup S_{BAa} \cup S_{BCa}) & (S_{Bb} \cup S_{BAb} \cup S_{BCb}) & (S_{Bc} \cup S_{BAc} \cup S_{BCc}) \\ (S_{Ca} \cup S_{CAa} \cup S_{CBa}) & (S_{Cb} \cup S_{CAb} \cup S_{CBb}) & (S_{Cc} \cup S_{CAc} \cup S_{CBc}) \end{bmatrix} * \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (7.5)$$

where

$S_{Aa} = S_{Aa1} \cap S_{Aa2}$ $S_{ABa} = S_{Aa1} \cap S_{Ba2}$ $S_{ACa} = S_{Aa1} \cap S_{Ca2}$

$S_{Ba} = S_{Ba1} \cap S_{Ba2}$ $S_{BAa} = S_{Ba1} \cap S_{Aa2}$ $S_{BCa} = S_{Ba1} \cap S_{Ca2}$

$S_{Ca} = S_{Ca1} \cap S_{Ca2}$ $S_{CAa} = S_{Ca1} \cap S_{Aa2}$ $S_{CBa} = S_{Ca1} \cap S_{Ba2}$

$S_{Ab} = S_{Ab1} \cap S_{Ab2}$ $S_{ABb} = S_{Ab1} \cap S_{Bb2}$ $S_{ACb} = S_{Ab1} \cap S_{Cb2}$

$S_{Bb} = S_{Bb1} \cap S_{Bb2}$ $S_{BAb} = S_{Bb1} \cap S_{Ab2}$ $S_{BCb} = S_{Bb1} \cap S_{Cb2}$

$S_{Cb} = S_{Cb1} \cap S_{Cb2}$ $S_{CAb} = S_{Cb1} \cap S_{Ab2}$ $S_{CBb} = S_{Cb1} \cap S_{Bb2}$

$S_{Ac} = S_{Ac1} \cap S_{Ac2}$ $S_{ABc} = S_{Ac1} \cap S_{Bc2}$ $S_{ACc} = S_{Ac1} \cap S_{Cc2}$

$S_{Bc} = S_{Bc1} \cap S_{Bc2}$ $S_{BAc} = S_{Bc1} \cap S_{Ac2}$ $S_{BCc} = S_{Bc1} \cap S_{Cc2}$

$S_{Cc} = S_{Cc1} \cap S_{Cc2}$ $S_{CAc} = S_{Cc1} \cap S_{Ac2}$ $S_{CBc} = S_{Cc1} \cap S_{Bc2}$

1= switch closed; 0 = switch open; $\cap$ *= Logical AND operator;* $\cup$ *= Logical OR operator*

$$M_{ijk} = \frac{t_{ijk}}{T_s} = \left[\frac{1}{3} + \frac{2v_i.v_j}{3.V_{im}^2}\right] \qquad (7.6)$$

for i $\in$ A, B, C and j $\in$ a, b, c and k $\in$ 1, 2.

Signals controlling switches in individual cells of the converter should be shifted with respect to each other by an angle of 2π/p, where p is the number of switching cells which in this case is two. Displacement of carrier signals involved in the control of switches S_{ij1} and S_{ij2} is $T_{sw}/2$, where $T_{sw} = 1/f_{sw}$ is the carrier switching period. Duty cycles for switch group S_{ij1} are by comparison of modula - tion function with the saw-tooth carrier starting from the origin and that for switch group S_{ij2} are by comparison of the modulation functions with the saw-tooth carrier phase shifted by $T_{sw}/2$ or π radians [19].

7.4 OUTPUT FILTER: The output filter circuit shown in Fig. 7.1 is a RLC circuit, with R_f, L_f and C_f connected in series whose resonant frequency matches with the carrier switching frequency f_{sw} [19], as given below:

$$f_{SW} = \frac{1}{\left(2\pi.\sqrt{L_f.C_f}\right)} \qquad (7.7)$$

7.5 MODEL DEVELOPMENT: The model of the three phase AC to three Phase AC MMC with three flying capacitors per output phase using SIMULINK [51] is shown in Fig. 7.2. The model parameters are shown in Table 7.3. The modulation function shown in equation 7.6 is used to calcu -

TABLE 7.3: PH3 MMC with Three FC Model Parameters

Sl.No.	Parameter	Value	Unit
1	RMS Line to Neutral Input Voltage Vi	220	Volts
2	Input Frequency fi	50	Hertz
3	Output Frequency fo	50	Hertz
4	q	0.5	-----
5	Carrier Switching Frequency fsw	5	kHz
6	Flying Capacitor C1 to C9	10	micro Farad
7	Series RLC Output Filter Rf, Lf, Cf	10, 2e-3, 0.50712e-6	Ohms, H, F
8	RL load	50, 0.5	Ohms, H

late the duty-cycle for the bidirectional switches. In Fig. 7.2, the Embedded MATLAB Function with the inputs q, Vim, fi, fo and time module calculates the nine modulation for the three phase input and output voltages defined in equation 3.9 and 3.11 of Chapter III, each phase voltage corresponding to input and output duly phase shifted by π/2 radians. The switching pulses for the nine switches starting from SAa1 to SCc1 in the first column of Fig. 7.1 are obtained by comparison of the respective modulation functions with a 5 kHz saw-tooth waveform VSAW1 and applying logic operation using a second Embedded MATLAB Function. The same for the other group of bidirectional switches SAa2 to SCc2 in the second column of Fig. 7.1 are obtained by comparing the respective modulation functions with another 5kHz saw-tooth waveform VSAW2 which is phase shifted by π radians or Tsw/2 seconds (1/(2*fsw)) from the first saw-tooth waveform VSAW1 and applying logic operation using a third Embedded MATLAB Function. The source code for the logic operation to generate the gate pulses for the two groups of nine bidirectional switches is the same as in section 3.3.1 of Chapter III. The only difference is that the second Embedded MATLAB Function compares the nine modulation functions with saw-tooth carrier VSAW1 and performs logic operation to generate gate pulses tAa1 to tCc1 for the nine switches in the first column of Fig. 7.1 and the third Embedded MATLAB Function compares the nine modulation functions with saw-tooth carrier VSAW2 and performs logic operation to generate gate pulses tAa2 to tCc2 for the nine switches in the second column of Fig. 7.1. The output filter parameter is chosen by assuming a 10 Ohms resistance, 2 milli Henry inductance and the output filter capacitor using equation 7.7 for the carrier switching frequency fsw in Table 7.3. The flying capacitor C1 to C9 in Fig. 7.1 is selected by assuming a peak value of

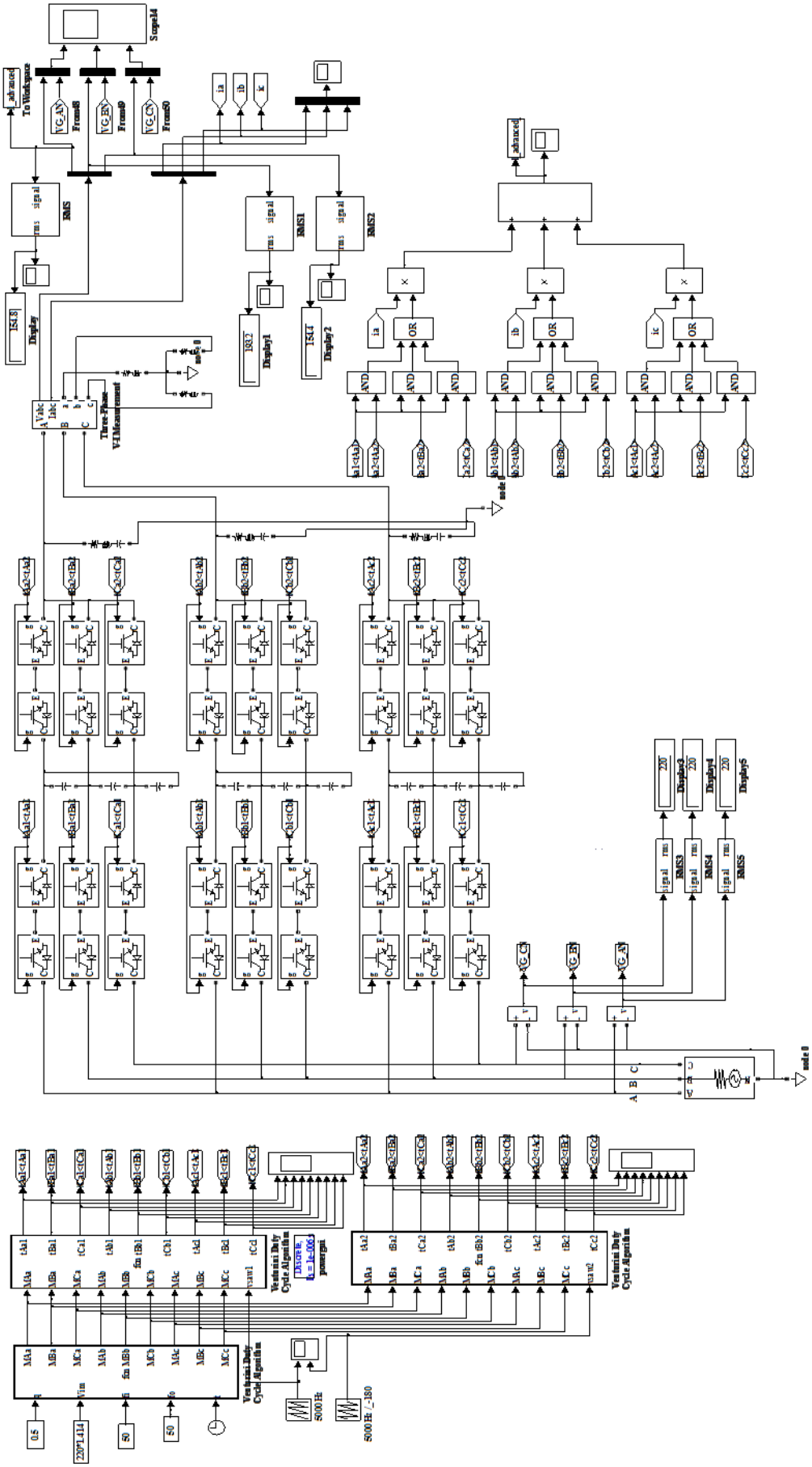


FIG. 7.2: MODEL OF THREE PHASE AC TO THREE PHASE AC MULTILEVEL MATRIX CONVERTER WITH THREE FLYING CAPACITORS PER OUTPUT PHASE

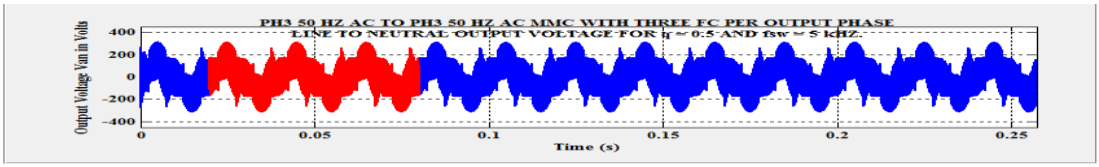
load current of 2 Amps, a voltage ripple of ΔVc of 20% for the carrier switching frequency fsw in Table 7.3.

7.5.1 SIMULATION RESULTS: The simulation of the three phase MMC with three FC per output phase for the data in Table 7.3 is carried out using SIMULINK [51]. The Fixed step ode5 (Dormand-Prince) solver is used. Harmonic Spectrum of the Line to neutral output voltage, Phase A Input Current and Line to Line output voltage are shown in Fig. 7.3. to Fig. 7.5 respectively. The simulation results for the three phase Line to neutral output voltage , Phase A input current, three phase Line to Line output voltage and three phase load current are shown in Fig. 7.6 to Fig. 7.9 respectively. The two 5 kHz saw-tooth carrier and the gate pulse for the nine group of bidirectional switches in the first and second column of Fig. 7.1 are shown in Fig. 7.10 and 7.11(A) and (B) respectively. The simulation results from the Harmonic Spectrum are tabulated in Table 7.4.

7.5.2 DISCUSSION OF RESULTS: The simulation results for the line to neutral and line to line output voltage indicate severe voltage unbalance for output phase b for the former case and the phase b-c for the later. This in turn has caused load current unbalance. Therefor the model for the above MMC with three FC per output phase has been reviewed or re-examined using the software PSCAD.

7.6 SIMULATION OF THREE PHASE MULTILEVEL MATRIX CONVERTER WITH THREE FLYING CAPACITORS PER OUTPUT PHASE USING PSCAD: The simulation of the three phase MMC with three FC has been re-examined here using the software PSCAD [53] for reasons mentioned in section 7.5.2. The parameters given in Table 7.3 is used. The complete model of the above mentioned MMC is shown in Fig. 7.12 using PSCAD [53]. The three phase sine wave input and output voltages to develop nine modulation functions are developed using the AM/FM/PM modulator in the Continuous System Model Functions (CSMF) library. The nine modulation functions for the bidirectional switches are also developed using adders, multipliers and dividers in the CSMF library. The two saw-tooth carrier signals VSAW1 and VSAW2 having switching frequency fsw of 5 kHz with a phase difference of π radians (1/(2*fsw) seconds) are developed using two X-Y Transfer Function block also in the CSMF library. The voltmeter, ammeter, FFT and THD measurement blocks are from the Meters library. The three phase AC source for the MMC is from the sources library, the elements resistor, inductor, capacitor are from Passive Elements library and the bidirectional IGBT switches are from the HVDC, FACTS and Power Electronics library.

The gate pulse for the group of switches in the first column of Fig. 7.1 is by comparison with saw-tooth carrier VSAW1 and that for the second column is by comparison with VSAW2. To generate gate pulse for switch SAa1 in Fig. 7.1, the modulation function MAa is compared with VSAW1. The comparator output tAa1 is HIGH if VSAW1 is less than or equal to MAa, else its output is LOW. Similarly the sum of the modulation functions (MAa + MBa) is compared with VSAW1 in a second comparator whose output tABa1 is HIGH if VSAW1 is less than or equal to (MAa + MBa), else its



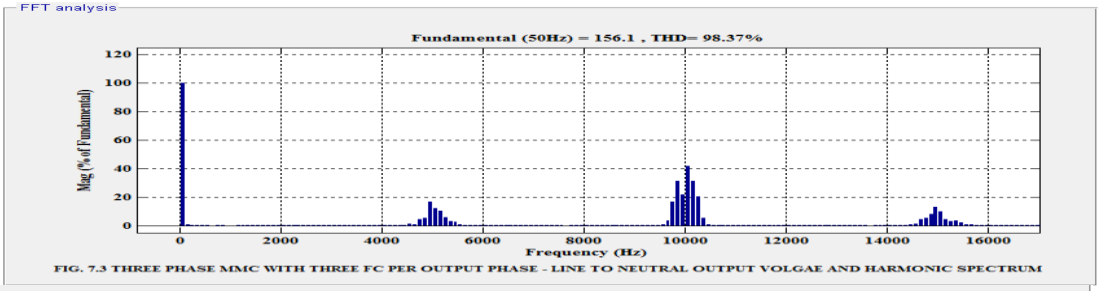
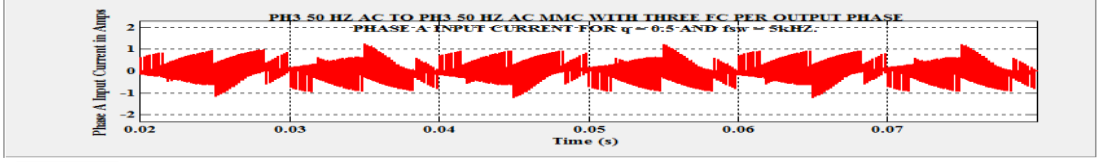


FIG. 7.3 THREE PHASE MMC WITH THREE FC PER OUTPUT PHASE - LINE TO NEUTRAL OUTPUT VOLGAE AND HARMONIC SPECTRUM



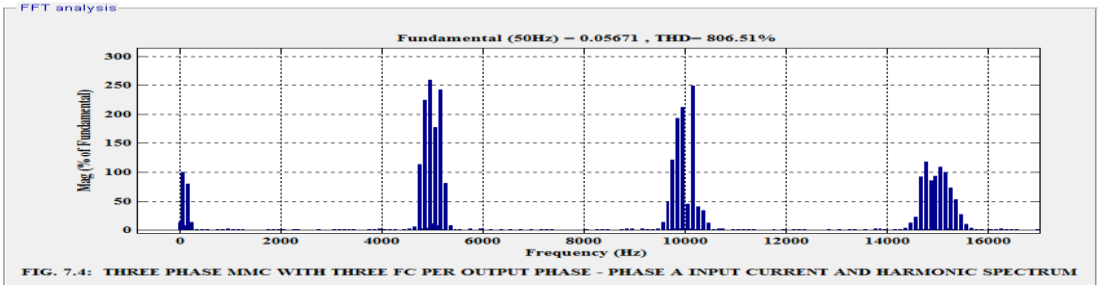
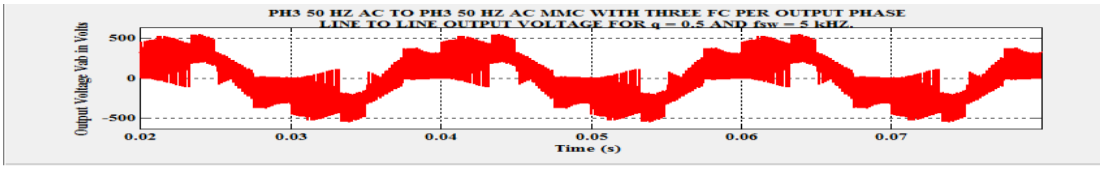


FIG. 7.4: THREE PHASE MMC WITH THREE FC PER OUTPUT PHASE - PHASE A INPUT CURRENT AND HARMONIC SPECTRUM



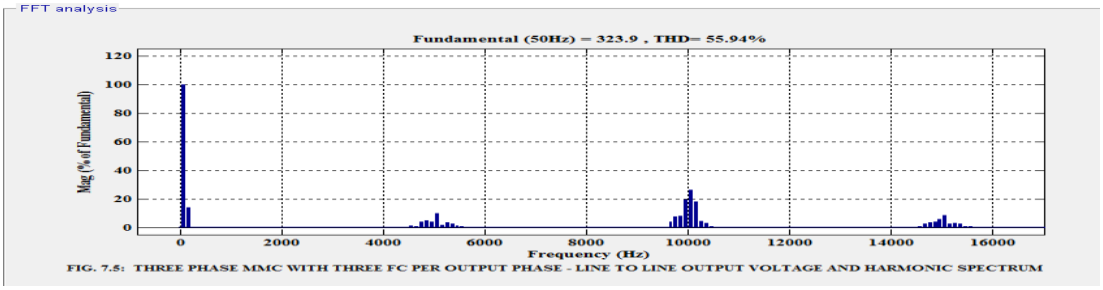


FIG. 7.5: THREE PHASE MMC WITH THREE FC PER OUTPUT PHASE - LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM

TABLE 7.4: PH3 MMC with Three FC – SIMULINK Simulation Results

Sl. No.	Topology	Parameters	Line to Neutral Output Voltage		Line to Line Output Voltage		Phase A Input Current	
			Peak Funda-mental (Volts)	T.H.D. (p.u.)	Peak Funda-mental (Volts)	T.H.D. (p.u.)	Peak Funda-mental (Amps)	T.H.D. (p.u.)
1)	Three phase MMC With THREE FC	Table 7.3	156.1	0.9837	323.9	0.5594	0.0567	8.065

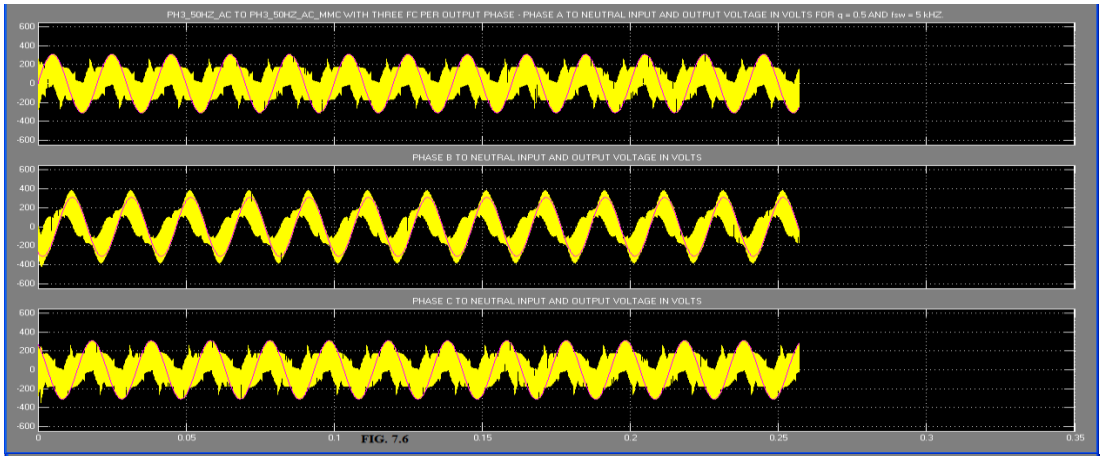


FIG. 7.6

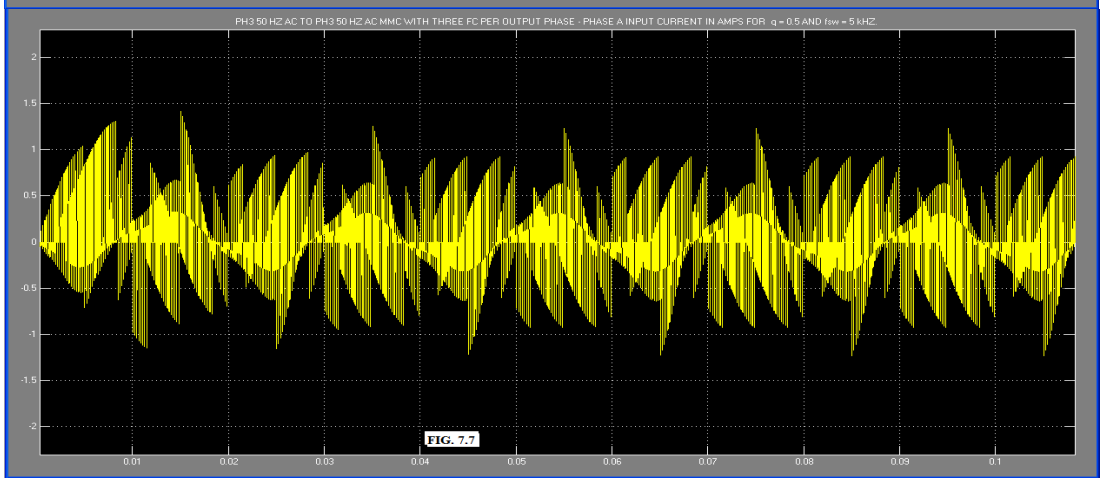


FIG. 7.7

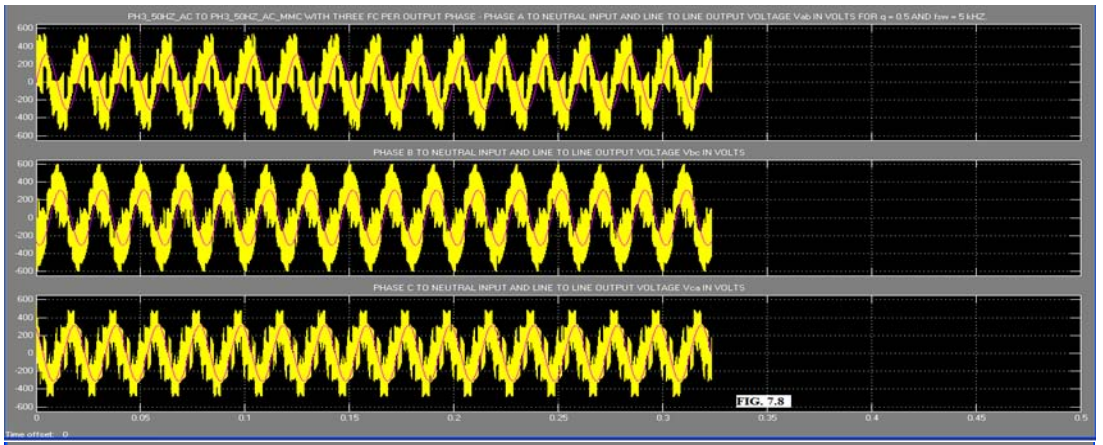


FIG. 7.8

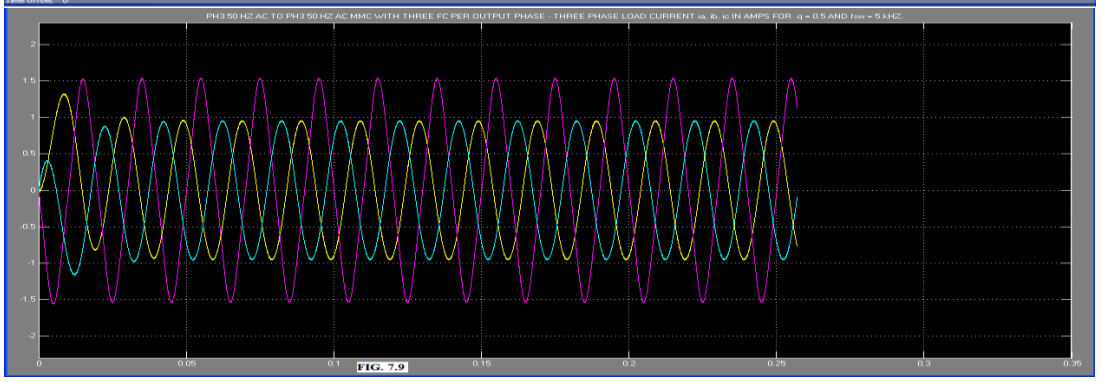


FIG. 7.9

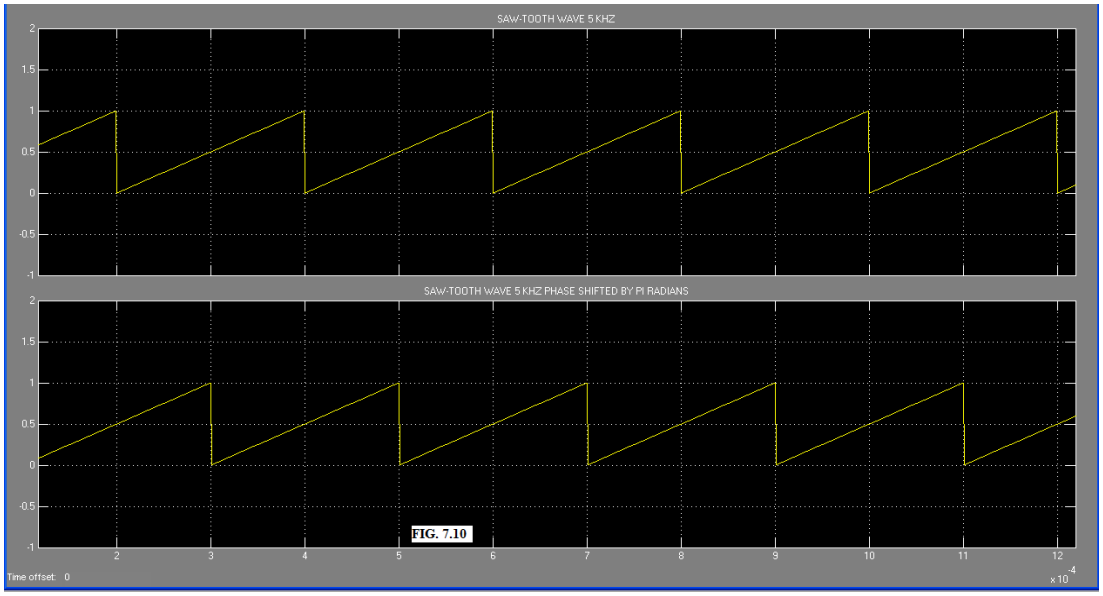


FIG. 7.10

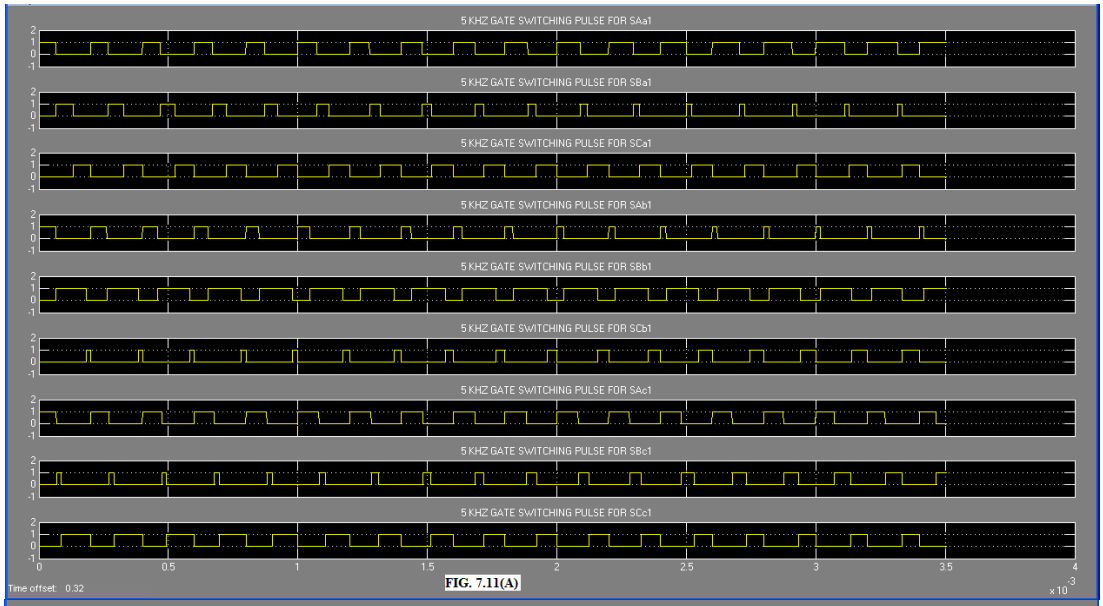


FIG. 7.11(A)

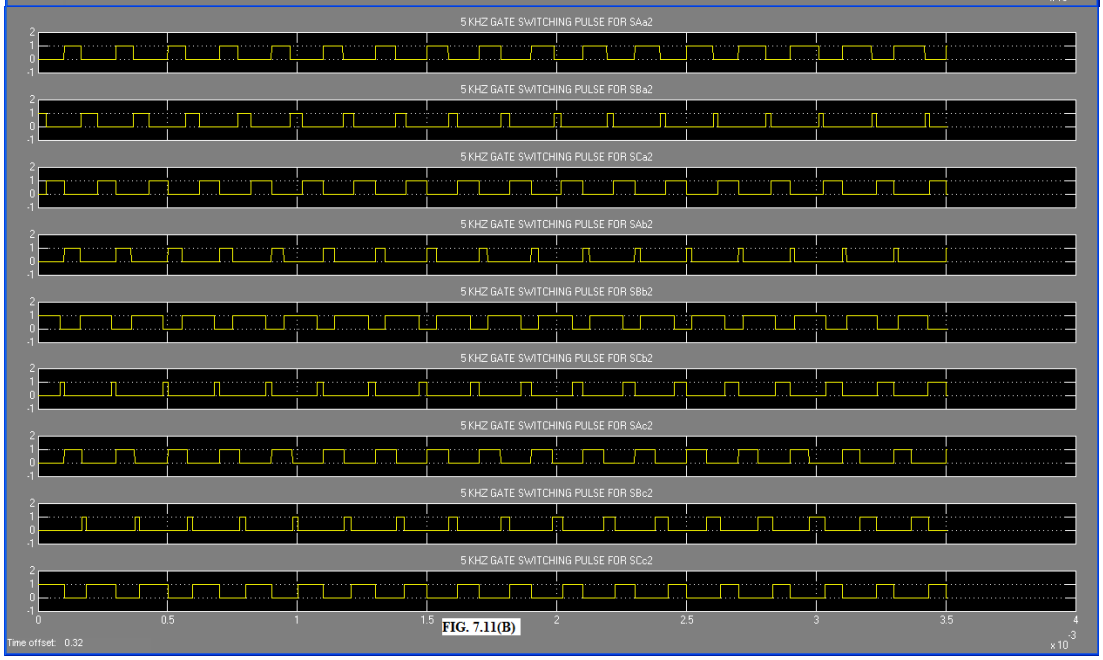


FIG. 7.11(B)

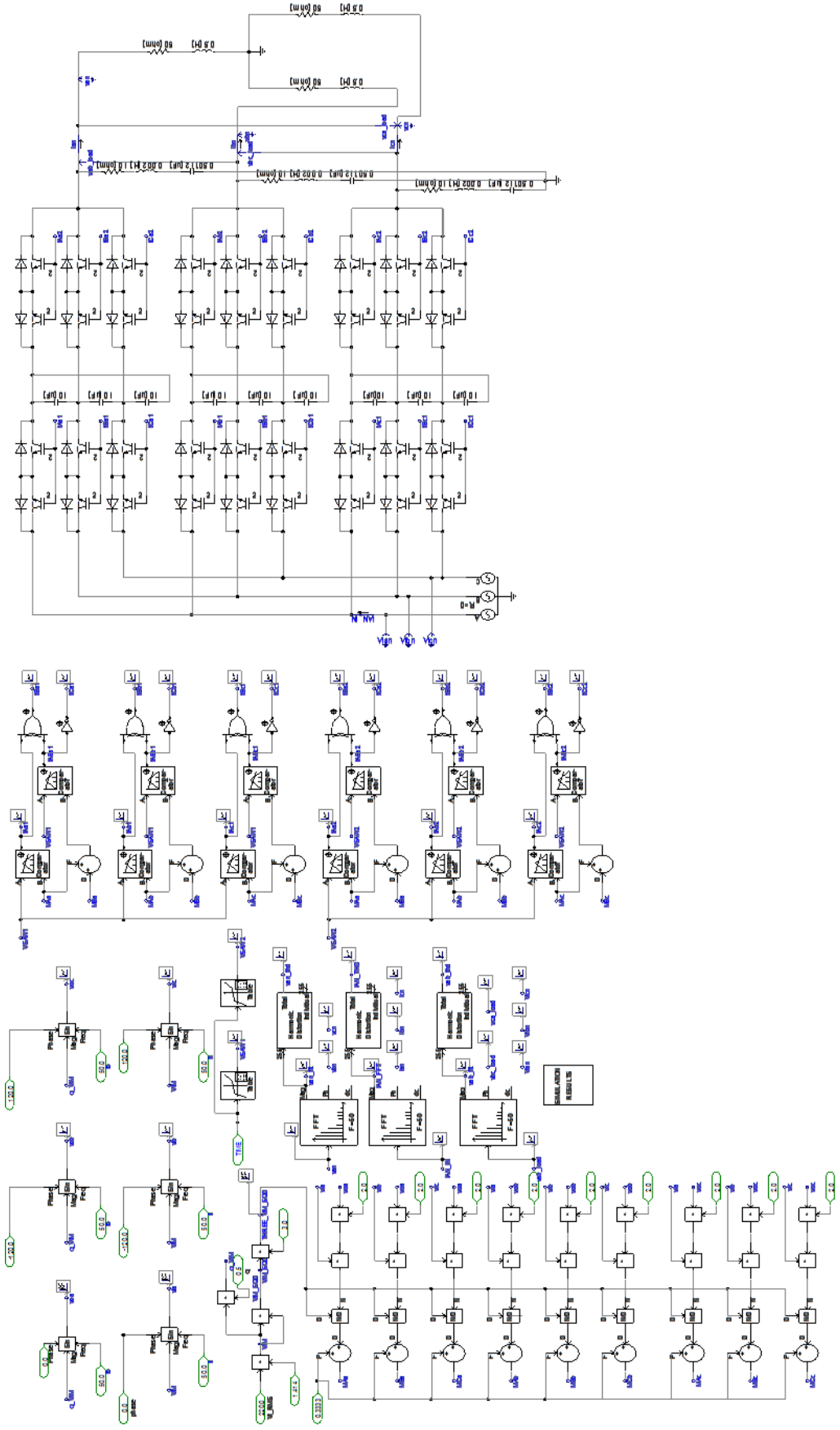


FIG 7.12: MODEL OF THREE PHASE AC TO THREE PHASE AC MULTILEVEL MATRIX CONVERTER

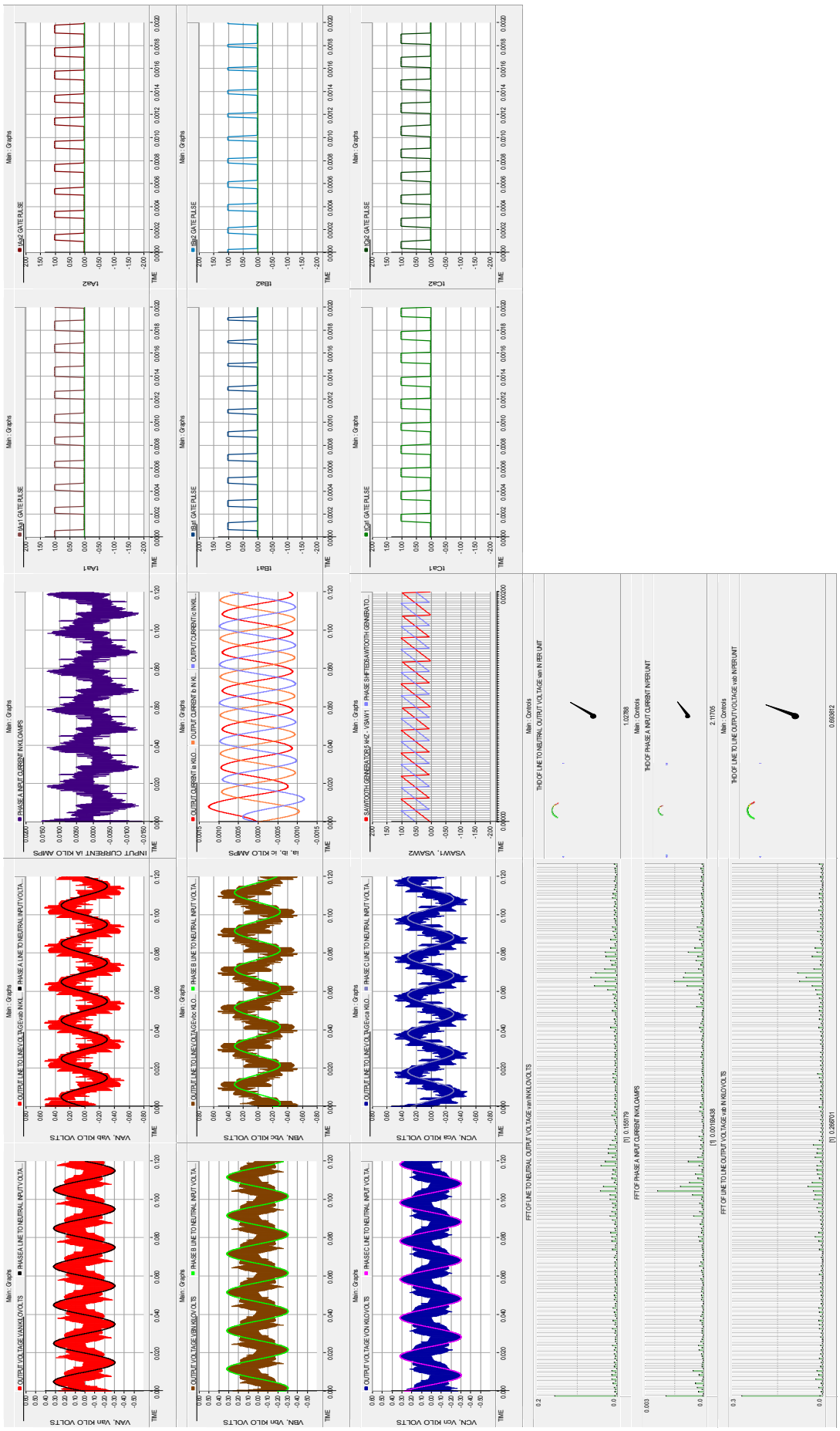


FIG. 7.13 : THREE PHASE MMC WITH THREE FC - SIMULATION RESULTS

output is LOW. The pulse outputs tAa1 and tABa1 are given to EXCLUSIVE-OR gate to obtain gate pulse tBa1. Gate pulse tCa1 is obtained by inverting tABa1 using a NOT gate. Similar method is adopted with VSAW2 for the group of bidirectional switches in the second column of Fig. 7.1.

7.6.1 SIMULATION RESULTS: The simulation results for the three phase line to neutral and line output voltages, Phase A input current, Load current, Harmonic spectrum and THD of line to neutral, line to line output voltages and input current, and the gate pulses to the three groups of switches in the first and second column of Fig. 7.1 corresponding to output phase a are shown in Fig. 7.13. The simulation results are tabulated in Table 7.5.

TABLE 7.5: PH3 MMC with Three FC – PSCAD Simulation Results

Sl.No.	Topology	Parameters	Line to Neutral Output Voltage		Line to Line Output Voltage		Phase A Input Current	
			Peak Fundamental (Volts)	T.H.D. (p.u.)	Peak Fundamental (Volts)	T.H.D. (p.u.)	Peak Fundamental (Amps)	T.H.D. (p.u.)
1)	Three Phase MMC With THREE FC	Table 7.3	155.17	1.0278	266.7	0.6936	1.934	2.117

7.7 DISCUSSION OF RESULTS: Examination of the waveforms for all the three phases relating to line to neutral output voltage, line to line output voltage, input current, load current and the peak fundamental magnitude and THD of the first three quantities above obtained by simulation of the model using SIMULINK and PSCAD reveals that there is a serious error with regard to the simulation results using SIMULINK. The simulation results using PSCAD indicate a closely well balanced line to neutral, line to line voltages and load current.

7.8 MULTILEVEL MATRIX CONVERTER WITH SIX FLYING CAPACITORS PER OUTPUT PHASE: This section on capacitor clamped three phase AC to three phase AC Multilevel Matrix Converter (MMC) with SIX flying capacitors (FC) per output phase is a development based on the method of analysis for three phase AC to three phase AC MMC with three FC presented in section 7.2 above. The above mentioned MMC with six FC is shown in Fig. 7.14. This topology has a total of nine bidirectional switches in each output phase. Three bidirectional switches are in series between each input phase and the output phase. A total of six flying capacitors per output phase, three in series in two groups are connected as in Fig. 7.14. The analysis is carried out below:

Referring to Fig. 7.15, assume that all the nine bidirectional switches connected to each output phase are identical having an off resistance of Roff. Then a total resistance of 6*Roff is coming in series across the input line to line voltage VAB, a resistance of 2*Roff and 4*Roff are coming in series across the voltage of flying capacitors C11 and C12 in the output phase a of Fig. 7.14, where VAB is (VA – VB). Then by potential divider action the voltage across flying capacitor C11 and C12 are

(VAB/3) and (2*VAB/3) respectively, with polarity positive at the top and negative at the bottom plate. This voltage levels are shown in Fig. 7.15. Then applying KVL to the groups of switches connected between input phase A, B and the output phase a, the truth table shown in Table 7.6 is valid. Table 7.6 is derived in Appendix A7.1.

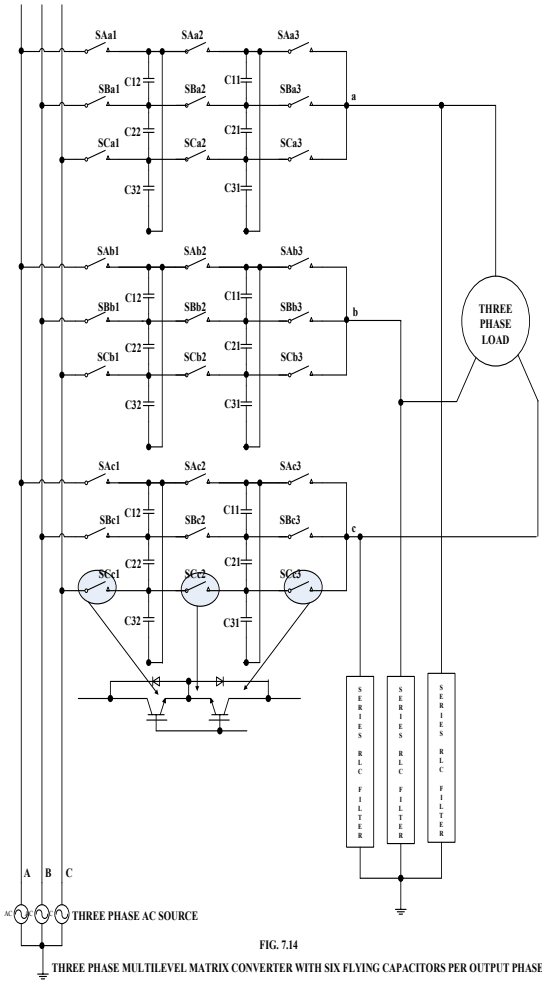


FIG. 7.14

THREE PHASE MULTILEVEL MATRIX CONVERTER WITH SIX FLYING CAPACITORS PER OUTPUT PHASE

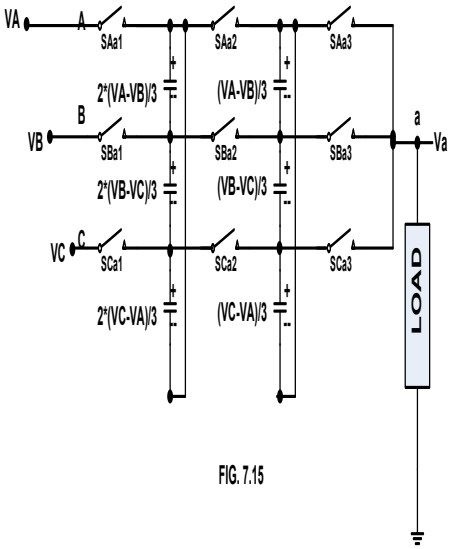


FIG. 7.15

The complete truth table for all the bidirectional switches connected between input phase A, B and C and the output phase a is shown in Table 7.7. From Table 7.7, it is clear that the output phase to neutral voltage has ten voltage levels. The flying capacitor is selected according to equation 7.2 [19].

TABLE 7.6: Truth Table for PH3 MMC with Six FC
1 = SWITCH CLOSED. 0 = SWITCH OPEN.

Sl.No.	SAa1	SAa2	SAa3	SBa1	SBa2	SBa3	Output Voltage Van (Volts)
1	1	1	1	0	0	0	VA
2	1	1	0	0	0	1	(2VA+VB)/3
3	1	0	0	0	1	1	(VA+2VB)/3
4	1	0	1	0	1	0	(2VA+VB)/3
5	0	0	0	1	1	1	VB

TABLE 7.7: Complete Truth Table for PH3 MMC with Six FC 1 = SWITCH CLOSED. 0 = SWITCH OPEN										
Sl.No.	SAa1	SAa2	SAa3	SBa1	SBa2	SBa3	SCa1	SCa2	SCa3	Output Voltage van (Volts)
1	1	1	1	0	0	0	0	0	0	VA
2	1	1	0	0	0	1	0	0	0	(2VA+VB)/3
3	1	0	0	0	1	1	0	0	0	(VA+2VB)/3
4	1	0	1	0	1	0	0	0	0	(2VA+VB)/3
5	1	0	0	0	1	0	0	0	1	(VA+VB+VC)/3
6	1	0	0	0	0	1	0	1	0	(VA+VB+VC)/3
7	0	0	0	1	1	1	0	0	0	VB
8	0	0	1	1	1	0	0	0	0	(VA+2VB)/3
9	0	1	1	1	0	0	0	0	0	(2VA+VB)/3
10	0	1	0	1	0	1	0	0	0	(VA+2VB)/3
11	0	0	0	1	1	0	0	0	1	(2VB+VC)/3
12	0	0	0	1	0	0	0	1	1	(VB+2VC)/3
13	0	0	0	1	0	1	0	1	0	(2VB+VC)/3
14	0	0	1	1	0	0	0	1	0	(VA+VB+VC)/3
15	0	1	0	1	0	0	0	0	1	(VA+VB+VC)/3
16	0	0	0	0	0	0	1	1	1	VC
17	0	0	0	0	0	1	1	1	0	(VB+2VC)/3
18	0	0	0	0	1	1	1	0	0	(2VB+VC)/3
19	0	0	0	0	1	0	1	0	1	(VB+2VC)/3
20	0	0	1	0	0	0	1	1	0	(VA+2VC)/3
21	0	1	1	0	0	0	1	0	0	(2VA+VC)/3
22	0	1	0	0	0	0	1	0	1	(VA+2VC)/3
23	1	1	0	0	0	0	0	0	1	(2VA+VC)/3
24	1	0	0	0	0	0	0	1	1	(VA+2VC)/3
25	1	0	1	0	0	0	0	1	0	(2VA+VC)/3
26	0	1	0	0	0	1	1	0	0	(VA+VB+VC)/3
27	0	0	1	0	1	0	1	0	0	(VA+VB+VC)/3

7.8.1 CONTROL OF MULTILEVEL MATRIX CONVERTER WITH SIX FLYING CAPACITORS PER OUTPUT PHASE BY VENTURINI METHOD: Let the input and output voltages be expressed as in equation 3.9 and 3.11 in Chapter III. For Unity input phase displacement factor, the nine modulation functions for a three phase AC to three phase AC conventional matrix converter is given in equation 3.17 and its validity for three phase cosine wave and sine wave input and output voltages is proved in A3.3 Appendix in Chapter III. Here the modified modulation function assuming unity input phase displacement factor for the twenty seven bidirectional switches of the three phase MMC shown in Fig. 7.14 is given below:

$$M_{ijk} = \frac{t_{ijk}}{T_s} = \left[\frac{1}{3} + \frac{2v_i.v_j}{3.V_{im}^2}\right] \qquad (7.8)$$

$$\text{for i} \in \text{A, B, C and j} \in \text{a, b, c and k} \in 1, 2, 3.$$

Signals controlling switches in individual cells of the converter should be shifted with respect to each other by an angle of $2\pi/p$, where p is the number of switching cells which in this case is three. Displacement of carrier signals involved in the control of switches S_{ij1}, S_{ij2} and S_{ij3} is $T_{sw}/3$ and $2T_{sw}/3$ respectively where $T_{sw} = 1/f_{sw}$ is the carrier switching period. Duty cycles for switch group S_{ij1} are by comparison of modulation function with the saw-tooth carrier starting from the origin, that for switch group S_{ij2} and S_{ij3} are by comparison of the modulation functions with the saw-tooth carrier phase shifted by $T_{sw}/3$ or $2\pi/3$ radians and $2T_{SW}/3$ or $4\pi/3$ radians respectively [19].

The output filter is a R-L-C series circuit which is set to resonate at the carrier switching frequency and whose values are selected according to equation 7.7 [19].

7.8.2 SIMULATION OF THREE PHASE MULTILEVEL MATRIX CONVERTER WITH SIX FLYING CAPACITORS PER OUTPUT PHASE USING PSCAD: The simulation of the three phase MMC with six FC has been carried out here using the software PSCAD [53] for reasons mentioned in section 7.5.2. The parameters given in Table 7.3 is used. The complete model of the above mentioned MMC is shown in Fig. 7.16 using PSCAD [53]. The three phase sine wave input and output voltage modules for generating the modulation functions and the method of generation of the nine modulation functions for the bidirectional switches are already explained in section 7.6 above. The three saw-tooth carrier signals VSAW1, VSAW2 and VSAW3 having switching frequency fsw of 5 kHz with a phase difference of $2\pi/3$ and $4\pi/3$ radians (1/(3*fsw) seconds and 2/(3*fsw) seconds) are developed using three X-Y Transfer Function block also in the CSMF library. The gate pulse for the group of switches in the first column of Fig. 7.14 is by comparison of the modulation functions MAa and (MAa+MBa) with saw-tooth carrier VSAW1 using two comparators and giving the output of these two comparators to logic gates which is already explained in section 7.6 above. For the group of switches in the second and third column of Fig. 7.14, the above modulation functions are compared with saw-tooth carrier VSAW2 and VSAW3 respectively using two comparators and the method of generating the gate pulse using logic gates is the same as explained in section 7.6 above.

7.8.3 SIMULATION RESULTS: The simulation results for the three phase line to neutral and line output voltages, Phase A input current, Load current, Harmonic spectrum and THD of line to neutral, line to line output voltages and input current, the three saw-tooth carrier waveforms and the gate pulses to the three groups of switches in the first, second and third column of Fig. 7.14 corresponding to output phase a are shown in Fig. 7.17. The simulation results are tabulated in Table 7.8.

TABLE 7.8: PH3 MMC with Six FC – PSCAD Simulation Results

Sl.No.	Topology	Parameters	Line to Neutral Output Voltage		Line to Line Output Voltage		Phase A Input Current	
			Peak Funda-mental (Volts)	T.H.D. (p.u.)	Peak Funda-mental (Volts)	T.H.D. (p.u.)	Peak Funda-mental (Amps)	T.H.D. (p.u.)
1)	Three Phase MMC With SIX FC	Table 7.3	152.74	0.879	270.336	0.5809	1.567	1.598

7.9 DISCUSSION OF RESULTS: Comparison of the simulation results using PSCAD shown in Table 7.5 with that of Table 7.8 shows that the three phase MMC with six FC per output phase has a lower value of THD for the line to neutral output voltage, line to line output voltage and phase A input current compared to the three phase MMC with three FC per output phase. The percentage decrease in THD for the former topology compared to the later one is 14.47%, 16.24% and 24.5% respectively for the line to neutral output voltage, line to line output voltage and phase A input current.

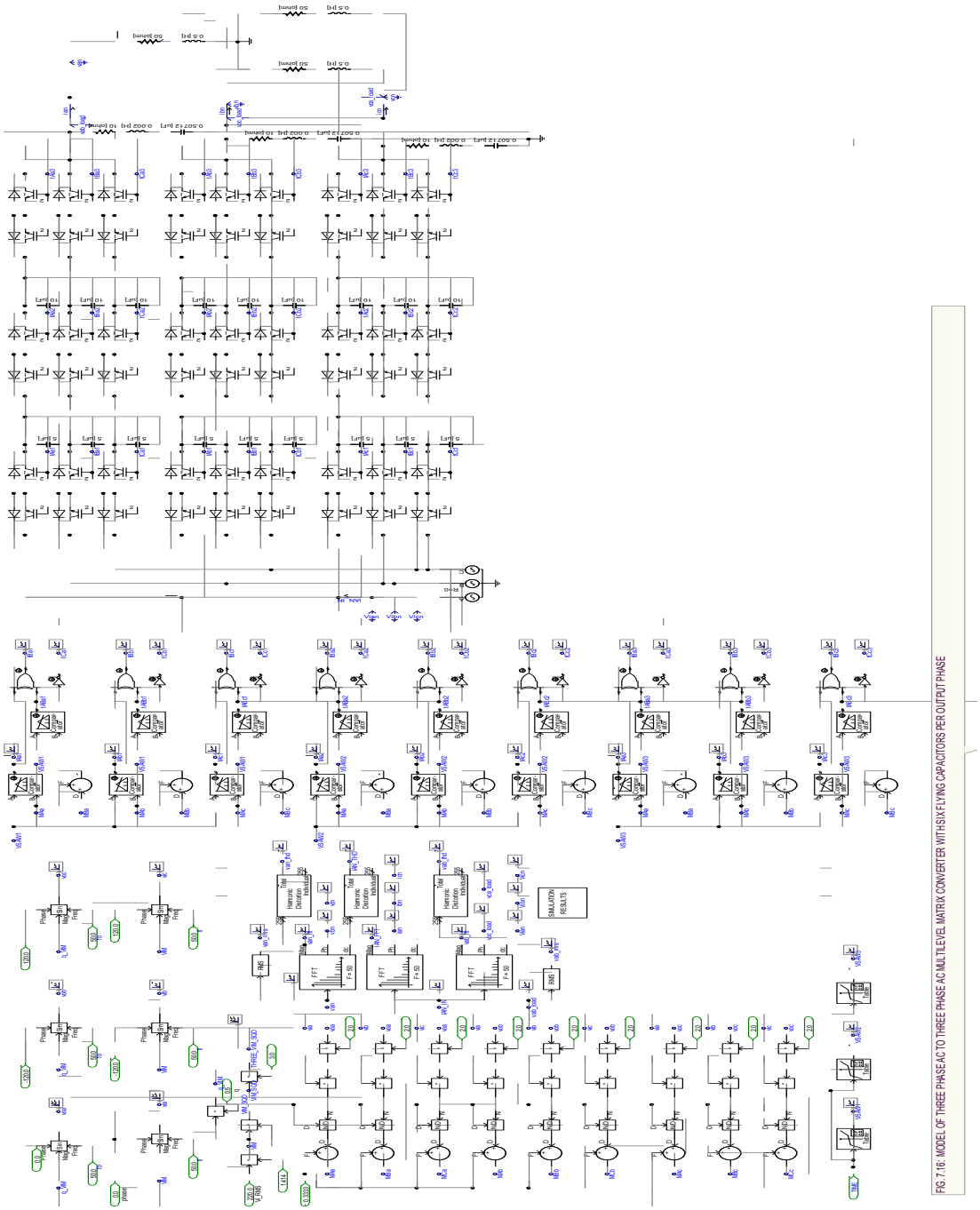


FIG. 7.16: MODEL OF THREE PHASE AC TO THREE PHASE AC MULTILEVEL MATRIX CONVERTER WITH SIX FLYING CAPACITORS PER OUTPUT PHASE

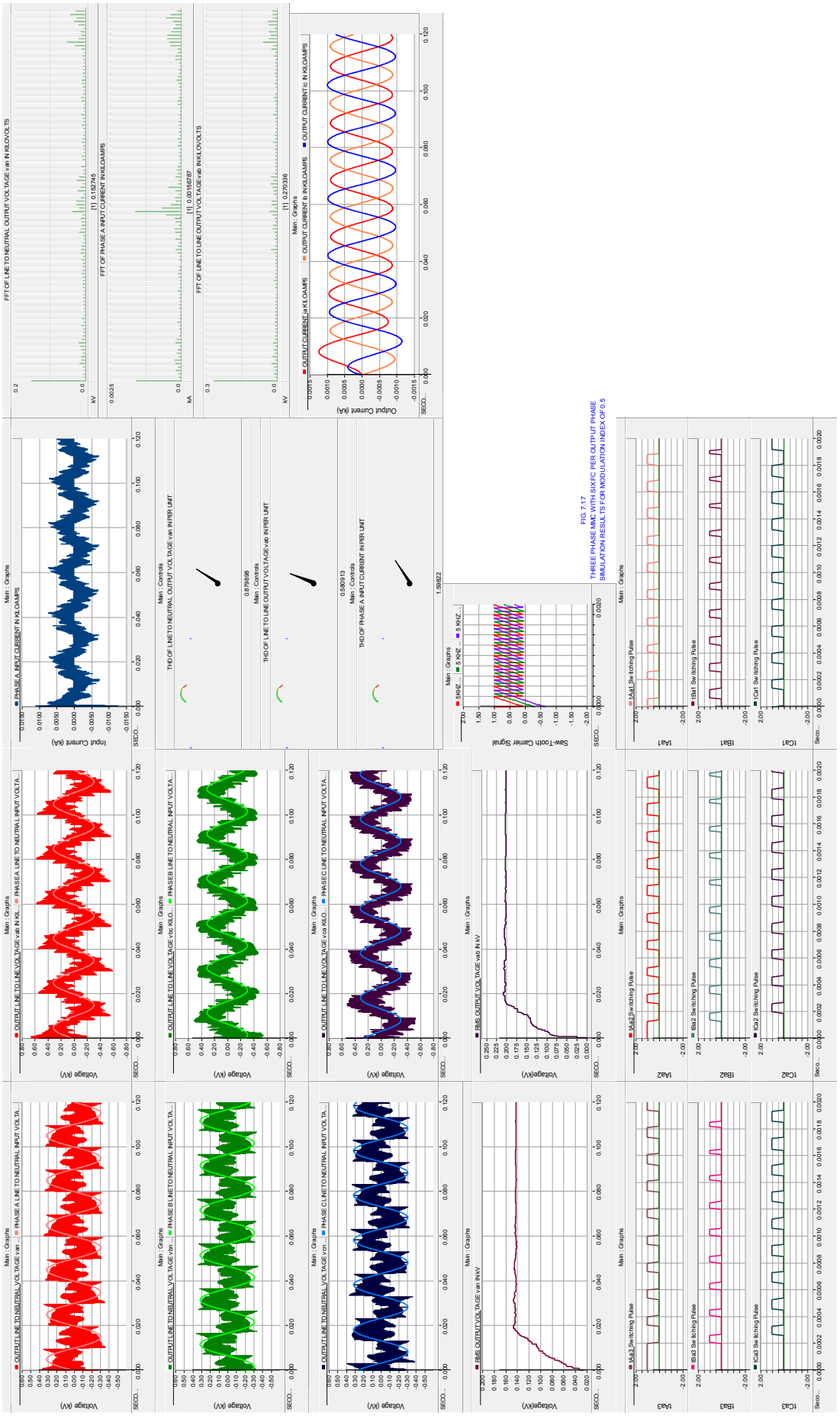


FIG. 7.17
THREE PHASE MC WITH SIXFIC PER OUTPUT PHASE
SIMULATION RESULTS FOR MODULATION INDEX OF 0.5

7.10 CONCLUSIONS: The modelling and simulation aspects of the three phase AC to three phase AC MMC with three FC and that with six FC per output phase have been explored in this chapter using two software packages SIMULINK and PSCAD for the former topology and with PSCAD for the later topology. Obviously the SIMULINK model gives erroneous performance compared to that with PSCAD for the former topology. Comparison of the values in Table 7.5 and 7.8 indicate that as the number of flying capacitors per output phase increases from three to six, the T.H.D. of line to neutral, line to line output voltages and input current decreases, which highlights the advantage of using more number of flying capacitors per output phase for the three phase matrix converter.

A7.1 APPENDIX: The entries in Table 7.6 are derived below. Referring to Fig. 7.15, the following analysis using KVL holds good:

$$1)\ \mathrm{SAa1} = 1; \mathrm{SAa2} = 1; \mathrm{SAa3} = 1.\ \text{All other switches 0.}$$

The output va is directly connected to the input phase voltage VA. $va = VA.\ (A7.1)$

$$2)\ \mathrm{SAa1} = 1; \mathrm{SAa2} = 1; \mathrm{SBa3} = 1.\ \text{All other switches 0.}$$

$$va = VA\ -\ (VA - VB)/3 =\ (2VA + VB)/3 \quad (A7.2)$$

$$3)\ \mathrm{SAa1} = 1; \mathrm{SBa2} = 1; \mathrm{SBa3} = 1.\ \text{All other switches 0.}$$

$$va = VA\ -\ 2 * (VA - VB)/3 =\ (VA + 2VB)/3 \quad (A7.3)$$

$$4)\ \mathrm{SAa1} = 1; \mathrm{SBa2} = 1; \mathrm{SAa3} = 1.\ \text{All other switches 0.}$$

$$va = VA\ -\ 2 * (VA - VB)/3 +\ (VA - VB)/3 =\ (2VA + VB)/3 \quad (A7.4)$$

$$5)\ \mathrm{SBa1} = 1; \mathrm{SBa2} = 1; \mathrm{SBa3} = 1.\ \text{All other switches 0.}$$

The output va is directly connected to the input phase voltage VB. $va = VB.\ (A7.5)$

Chapter VIII
Direct Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter

8.1 INTRODUCTION: The most used modulation strategy for Matrix Converter is the Space Vector Modulation since it is well suitable for digital implementation [31-35]. It provides full exploitation of the input voltage and good load current quality [31-35]. The Space vector modulation approach has advantages with respect to the traditional carrier based modulation technique such as a) Immediate comprehension of the required commutation process. b) Simplified control algorithm. c) Maximum voltage transfer without adding third harmonic components and avoiding a fictitious DC link and d) No synchronisation requirements with input voltage waveform. Moreover, the proposed switching algorithm allows to reduce the number of switching devices involved in a commutation process with respect to conventional switching strategies. As the modulation strategy is defined in terms of the output waveform amplitude and phase angle, it is readily adapted to high-performance motor drive applications such as field-oriented control [31-35]. The algorithm is based on the instantaneous space vector representation of input and output voltages and currents. It analyses all the possible switching configurations available in three-phase MCs and does not need the concept of a virtual dc link. This modulation technique is also known as Direct Space Vector Modulation (DSVM). In this chapter the models of the three phase AC to three phase AC MC using Direct Asymmetrical and Direct Symmetrical Space Vector modulation algorithm have been developed using SIMULINK and the results obtained by simulation are presented.

8.2 DIRECT SPACE VECTOR MODULATION ALGORITHM: The three phase AC to three phase AC MC and the twenty seven switching states are shown in Fig. 3.1 and Table 3.1 respectively in Chapter III. Direct Space Vector Modulation (DSVM) algorithm uses 21 of 27 possible states that can be generated by the matrix of bidirectional switches and can fully control both the output voltage vector and input current displacement angle [25-38]. These states are presented in Table 8.1. The meaning of Table 8.1 is given in A8.1 Appendix. The Space Vector Modulation (SVM) technique is explained below [31].

The output voltage and input current space vector hexagon are shown in Fig. 8.1(A) and (B). At any sampling instant, the output voltage vector v_o and the input current displacement angle φ_i are known as reference quantities [Fig. 8.2(a) and (b)]. The input line-to-neutral voltage vector v_i is imposed by the source voltages and is known by measurements. Then, the control of φ_i can be achieved controlling the phase angle β of the input current vector. In principle, the SVM algorithm is based on the selection of four active switching configurations that are applied for suitable time intervals within each sampling period T_S. The zero configurations are applied to complete T_S [31] .

TABLE 8.1: DSVM Switching States

SL.NO.	STATES a b c	SWITCHES ON	OUTPUT PHASE VOLTAGE $\lvert V_O \rvert$	$/\underline{\alpha_o}$	INPUT CURRENT $\lvert I_i \rvert$	$/\underline{\beta_i}$
1	ABB +1	S_{Aa} S_{Bb} S_{Bc}	$\frac{2.v_{AB}}{3}$	0	$\frac{2.i_a}{\sqrt{3}}$	$\frac{-\pi}{6}$
2	BAA -1	S_{Ba} S_{Ab} S_{Ac}	$\frac{-2.v_{AB}}{3}$	0	$\frac{-2.i_a}{\sqrt{3}}$	$\frac{-\pi}{6}$
3	BCC +2	S_{Ba} S_{Cb} S_{Cc}	$\frac{2.v_{BC}}{3}$	0	$\frac{2.i_a}{\sqrt{3}}$	$\frac{\pi}{2}$
4	CBB -2	S_{Ca} S_{Bb} S_{Bc}	$\frac{-2.v_{BC}}{3}$	0	$\frac{-2.i_a}{\sqrt{3}}$	$\frac{\pi}{2}$
5	CAA +3	S_{Ca} S_{Ab} S_{Ac}	$\frac{2.v_{CA}}{3}$	0	$\frac{2.i_a}{\sqrt{3}}$	$\frac{7\pi}{6}$
6	ACC -3	S_{Aa} S_{Cb} S_{Cc}	$\frac{-2.v_{CA}}{3}$	0	$\frac{-2.i_a}{\sqrt{3}}$	$\frac{7\pi}{6}$
7	BAB +4	S_{Ba} S_{Ab} S_{Bc}	$\frac{2.v_{AB}}{3}$	$\frac{2\pi}{3}$	$\frac{2.i_b}{\sqrt{3}}$	$\frac{-\pi}{6}$
8	ABA -4	S_{Aa} S_{Bb} S_{Ac}	$\frac{-2.v_{AB}}{3}$	$\frac{2\pi}{3}$	$\frac{-2.i_b}{\sqrt{3}}$	$\frac{-\pi}{6}$
9	CBC +5	S_{Ca} S_{Bb} S_{Cc}	$\frac{2.v_{BC}}{3}$	$\frac{2\pi}{3}$	$\frac{2.i_b}{\sqrt{3}}$	$\frac{\pi}{2}$
10	BCB -5	S_{Ba} S_{Cb} S_{Bc}	$\frac{-2.v_{BC}}{3}$	$\frac{2\pi}{3}$	$\frac{-2.i_b}{\sqrt{3}}$	$\frac{\pi}{2}$
11	ACA +6	S_{Aa} S_{Cb} S_{Ac}	$\frac{2.v_{CA}}{3}$	$\frac{2\pi}{3}$	$\frac{2.i_b}{\sqrt{3}}$	$\frac{7\pi}{6}$
12	CAC -6	S_{Ca} S_{Ab} S_{Cc}	$\frac{-2.v_{CA}}{3}$	$\frac{2\pi}{3}$	$\frac{-2.i_b}{\sqrt{3}}$	$\frac{7\pi}{6}$
13	BBA +7	S_{Ba} S_{Bb} S_{Ac}	$\frac{2.v_{AB}}{3}$	$\frac{4\pi}{3}$	$\frac{2.i_c}{\sqrt{3}}$	$\frac{-\pi}{6}$
14	AAB -7	S_{Aa} S_{Ab} S_{Bc}	$\frac{-2.v_{AB}}{3}$	$\frac{4\pi}{3}$	$\frac{-2.i_c}{\sqrt{3}}$	$\frac{-\pi}{6}$
15	CCB +8	S_{Ca} S_{Cb} S_{Bc}	$\frac{2.v_{BC}}{3}$	$\frac{4\pi}{3}$	$\frac{2.i_c}{\sqrt{3}}$	$\frac{\pi}{2}$
16	BBC -8	S_{Ba} S_{Bb} S_{Cc}	$\frac{-2.v_{BC}}{3}$	$\frac{4\pi}{3}$	$\frac{-2.i_c}{\sqrt{3}}$	$\frac{\pi}{2}$
17	AAC +9	S_{Aa} S_{Ab} S_{Cc}	$\frac{2.v_{CA}}{3}$	$\frac{4\pi}{3}$	$\frac{2.i_c}{\sqrt{3}}$	$\frac{7\pi}{6}$
18	CCA -9	S_{Ca} S_{Cb} S_{Ac}	$\frac{-2.v_{CA}}{3}$	$\frac{4\pi}{3}$	$\frac{-2.i_c}{\sqrt{3}}$	$\frac{7\pi}{6}$
19	AAA 0_1	S_{Aa} S_{Ab} S_{Ac}	0	0	0	0
20	BBB 0_2	S_{Ba} S_{Bb} S_{Bc}	0	0	0	0
21	CCC 0_3	S_{Ca} S_{Cb} S_{Cc}	0	0	0	0

To explain the SVM algorithm, referring to Fig. 8.2(A) and (B), both output voltage vector v_o and input current vector i_i are assumed to be in sector I. The reference voltage vector v_o is resolved into the components $v_{o\alpha}$ and $v_{o\beta}$ along the two adjacent vector directions. The component $v_{o\beta}$ can be synthesized using two voltage vectors having the same direction of $v_{o\beta}$. Among the six possible switching configurations, ± 7, ±8, ±9 shown in Fig. 2(A), the ones that allow also the modulation of the input current direction must be selected. It is seen that this constraint allows the elimination of two switching configurations, +8 and -8 in this case. Among the remaining four switching configurations for sector I, the application of the positive switching configurations +7 and +9 are assumed which are common to both output voltage and input current sectors. With similar considerations, the switching configurations required to synthesize the component $v_{o\alpha}$ which are common to both output voltage and input current sectors can be found as +1 and +3 respectively [31].

Using the same procedure, it is possible to determine the four switching configurations related to any possible combination of output voltage and input current sectors, leading to the results summarized in Table 8.2. Four symbols (I, II, III, IV) are also introduced in the last row of Table 8.2 to identify the four general switching configurations, valid for any combination of input current and output voltage sectors [31-38].

Now it is possible to write in a general form, the four basic equations of the SVM algorithm, which satisfy simultaneously the requirements of the reference output voltage vector and input current displacement angle. With reference to the output voltage vector, the following two equations can be written:

$$\underrightarrow{v_{o\beta}} = \underrightarrow{v_o^I} * \delta^I + \underrightarrow{v_o^{II}} * \delta^{II} = \frac{2}{\sqrt{3}} * v_o * \cos\left(\alpha - \frac{\pi}{3}\right) * e^{j\left[(S_v-1).\frac{\pi}{3}+\frac{\pi}{3}\right]} \ldots (8.1)$$

$$\underrightarrow{v_{o\alpha}} = \underrightarrow{v_o^{III}} * \delta^{III} + \underrightarrow{v_o^{IV}} * \delta^{IV} = \frac{2}{\sqrt{3}} * v_o * \cos\left(\alpha + \frac{\pi}{3}\right) * e^{j\left[(S_v-1).\frac{\pi}{3}\right]} \ldots (8.2)$$

With reference to the input current displacement angle, two equations are obtained by imposing on the vectors $(\underrightarrow{i_i^I} * \delta^I + \underrightarrow{i_i^{II}} * \delta^{II})$ and $(\underrightarrow{i_i^{III}} * \delta^{III} + \underrightarrow{i_i^{IV}} * \delta^{IV})$ the direction defined by β. This can be achieved by imposing a null value on the two-vector component along the direction perpendicular to $e^{j\beta}$(i.e., $je^{j\beta}$), leading to the following equations:

$$(\underrightarrow{i_i^I} * \delta^I + \underrightarrow{i_i^{II}} * \delta^{II}) * je^{j\beta} * e^{j(S_i-1).\frac{\pi}{3}} = 0 \ldots (8.3)$$

$$(\underrightarrow{i_i^{III}} * \delta^{III} + \underrightarrow{i_i^{IV}} * \delta^{IV}) * je^{j\beta} * e^{j(S_i-1).\frac{\pi}{3}} = 0 \ldots (8.4)$$

$\delta^I, \delta^{II}, \delta^{III}$ and δ^{IV} are the duty cycles (i.e., $\delta^I = t^I/Ts$) of the four switching configurations, $S_v = 1, 2 \ldots .6$ represents the output voltage sector, and $S_i = 1, 2 \ldots . .6$ represents the input current sector. $\underrightarrow{v_o^I}, \underrightarrow{v_o^{II}}, \underrightarrow{v_o^{III}}, \underrightarrow{v_o^{IV}}$ are the output voltage vectors associated respectively with the switching configurations I, II, III, IV given in Table II. The same convention hold good for the input current vectors.

FIG.8.1(A): OUTPUT VOLTAGE SPACE VECTOR HEXAGON

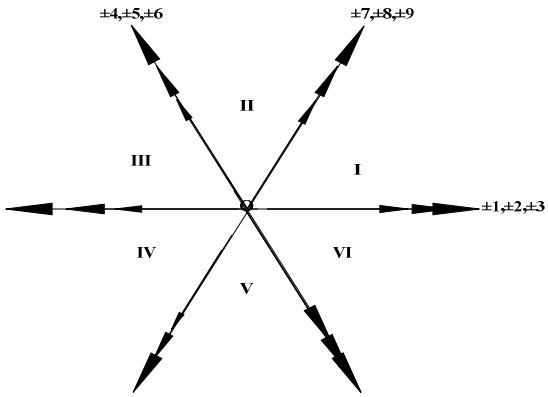
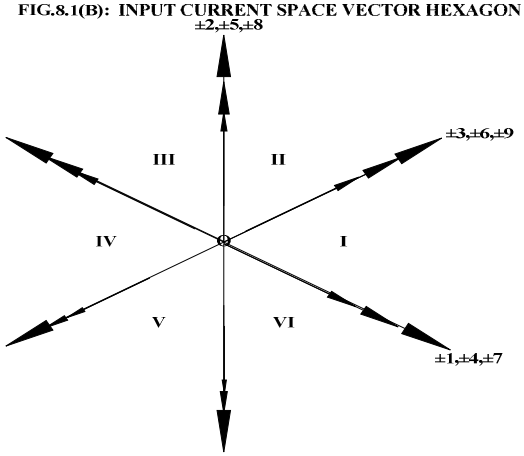


FIG.8.1(B): INPUT CURRENT SPACE VECTOR HEXAGON



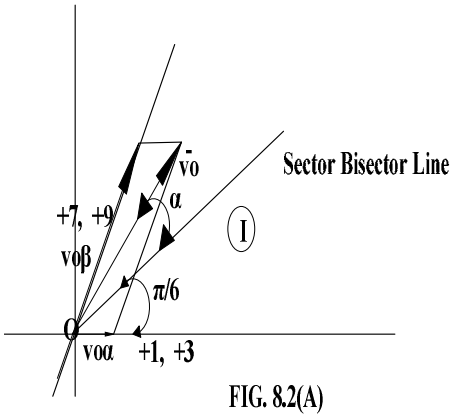


FIG. 8.2(A)

OUTPUT VOLTAGE VECTORS MODULATION PRINCIPLE

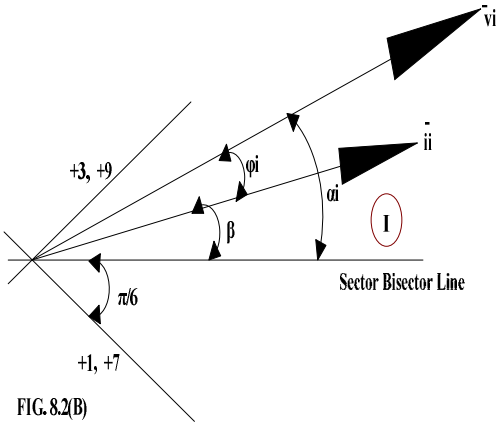


FIG. 8.2(B)

INPUT CURRENT VECTORS MODULATION PRINCIPLE

TABLE 8.2: DSVM – Active Vectors Configurations

		SECTOR OF OUTPUT VOLTAGE											
		1 or 4				2 or 5				3 or 6			
SECTOR OF INPUT CURRENT	1 or 4	9	7	3	1	6	4	9	7	3	1	6	4
	2 or 5	8	9	2	3	5	6	8	9	2	3	5	6
	3 or 6	7	8	1	2	4	5	7	8	1	2	4	5
		I	II	III	IV	I	II	III	IV	I	II	III	IV

Solving equations 8.1 to 8.4 leads to the following equations for the duty cycles:

$$\delta^I = (-1)^{(S_v + S_i)} . \frac{2q}{\sqrt{3}} . \frac{\cos\left(\alpha - \frac{\pi}{3}\right) . \cos\left(\beta - \frac{\pi}{3}\right)}{\cos(\varphi_i)} \ldots (8.5)$$

$$\delta^{II} = (-1)^{(S_v + S_i + 1)} . \frac{2q}{\sqrt{3}} . \frac{\cos\left(\alpha - \frac{\pi}{3}\right) . \cos\left(\beta + \frac{\pi}{3}\right)}{\cos(\varphi_i)} \ldots (8.6)$$

$$\delta^{III} = (-1)^{(S_v + S_i + 1)} . \frac{2q}{\sqrt{3}} . \frac{\cos\left(\alpha + \frac{\pi}{3}\right) . \cos\left(\beta - \frac{\pi}{3}\right)}{\cos(\varphi_i)} \ldots (8.7)$$

$$\delta^{IV} = (-1)^{(S_v + S_i)} . \frac{2q}{\sqrt{3}} . \frac{\cos\left(\alpha + \frac{\pi}{3}\right) . \cos\left(\beta + \frac{\pi}{3}\right)}{\cos(\varphi_i)} \ldots (8.8)$$

A proof of equations 8.1, 8.2, 8.5 and 8.6 are given in A8.2 Appendix. Furthermore, for the feasibility of the control strategy, the sum of the absolute values of the four duty-cycles must be lower than unity.

$$\text{i.e., } |\delta^I| + |\delta^{II}| + |\delta^{III}| + |\delta^{IV}| \leq 1 \ldots (8.9)$$

The zero configurations are applied to complete the sampling period Ts, as shown below:

$$\delta^0 = 1 - \delta^I - \delta^{II} - \delta^{III} - \delta^{IV} \ldots (8.10)$$

In equations 8.5 to 8.8, negative value appears which corresponds to the corresponding negative switching state given in Table 8.1.

Switching strategies deal with the switching configuration sequence, that is, the order in which the active and zero vectors are applied along the commutation period. Here both the Asymmetrical SVM (ASVM) and Symmetrical SVM (SSVM) are analyzed in detail and a simulation models are developed.

The ASVM uses only one of the three zero configurations in the middle of the sequence so that minimum switch commutations are achieved between one switching state and the next one. Using this technique the switching commutations are up to eight for each commutation period. This way switching losses are minimized.

Two simple rules are proposed for both ASVM and SSVM which are given below [31-38]:

Rule 1: If (SV + SI) is even, then the order of the switching sequence is : $\delta^{III}, \delta^I, \delta^{II}, \delta^{IV}$.
Rule 2: If (SV + SI) is odd, then the order of the switching sequence is : $\delta^I, \delta^{III}, \delta^{IV}, \delta^{II}$.

Also referring to equations 8.5 to 8.8, if (SV + SI) is even, δ^{II} *and* δ^{III} have a negative sign and if (SV + SI) is odd, δ^I *and* δ^{IV} have a negative sign. This negative sign corresponds to the negative switching state in Table 8.1.

With regard to zero configuration for ASVM, Table 8.3 shown below can be used. For example, considering output voltage vector in sector 1 and input current vector in sector 4 (i.e., SV = 1; SI = 4) within their respective hexagons, it can be seen that (SV + SI) is odd, rule 2 applies with δ^I *and* δ^{IV}

having negative sign. Also using Table 8.3, the following is the only possible double-sided sequences that can be generated for ASVM technique:

TABLE 8.3: Zero Configuration for ASVM

I_i sector	Vo sector 1, 2, 3, 4, 5 or 6
1 or 4	AAA
2 or 5	CCC
3 or 6	BBB

-9, +3, -1, +7 which from table 8.1 is given below:

CCA – CAA – AAA – BAA – BBA ׀ BBA – BAA – AAA – CAA – CCA

׀←----------Ts/2---------- →׀←----------Ts/2----------→׀

where Ts is the sampling period.

The gate pulse pattern for ASVM using Tables 8.1 to 8.3, rules 1 and 2 is shown in Table 8.4.

TABLE 8.4 ASVM Switching Pattern

Sl.No.	SV, SI	(SV+SI)	SSF_X HIGH	BIDIRECTIONAL SWITCH GATE PULSE PATTERN				
				ta	tb	t0	tc	td
1	1, 1 or 4, 4	Even	ssf1	ACC	AAC	AAA	AAB	ABB
2	1, 4 or 4, 1	Odd	ssf2	CCA	CAA	AAA	BAA	BBA
3	1, 5 or 4, 2	Even	ssf3	CBB	CCB	CCC	CCA	CAA
4	1, 2 or 4, 5	Odd	ssf4	BBC	BCC	CCC	ACC	AAC
5	1, 3 or 4, 6	Even	ssf5	BAA	BBA	BBB	BBC	BCC
6	1, 6 or 4, 3	Odd	ssf6	AAB	ABB	BBB	CBB	CCB
7	2, 4 or 5, 1	Even	ssf7	CCA	ACA	AAA	ABA	BBA
8	2, 1 or 5, 4	Odd	ssf8	CAC	AAC	AAA	AAB	BAB
9	2, 2 or 5, 5	Even	ssf9	BBC	CBC	CCC	CAC	AAC
10	2, 5 or 5, 2	Odd	ssf10	BCB	CCB	CCC	CCA	ACA
11	2, 6 or 5, 3	Even	ssf11	AAB	BAB	BBB	BCB	CCB
12	2, 3 or 5, 6	Odd	ssf12	ABA	BBA	BBB	BBC	CBC
13	3, 1 or 6, 4	Even	ssf13	CAC	CAA	AAA	BAA	BAB
14	3, 4 or 6, 1	Odd	ssf14	ACC	ACA	AAA	ABA	ABB
15	3, 5 or 6, 2	Even	ssf15	BCB	BCC	CCC	ACC	ACA
16	3, 2 or 6, 5	Odd	ssf16	CBB	CBC	CCC	CAC	CAA
17	3, 3 or 6, 6	Even	ssf17	ABA	ABB	BBB	CBB	CBC
18	3, 6 or 6, 3	Odd	ssf18	BAA	BAB	BBB	BCB	BCC

With regard to zero configuration for SSVM, Table 8.5 shown below can be used.

TABLE 8.5: Zero Configuration for SSVM

I_i sector	Vo sector 1, 2, 3, 4, 5 or 6
1 or 4	CCC – AAA – BBB
2 or 5	BBB – CCC – AAA
3 or 6	AAA – BBB - CCC

For example, considering output voltage vector in sector 1 and input current vector in sector 4 (i.e., SV = 1; SI = 4) within their respective hexagons, it can be seen that (SV + SI) is odd, rule 2 applies

with δ^I *and* δ^{IV} having negative sign. Also using Table 8.5, the following is the only possible double-sided sequences that can be generated for SSVM technique.

-9, +3, -1, +7 which from table 1 is given below:

CCC-CCA–CAA–AAA–BAA–BBA-BBB|BBB-BBA–BAA–AAA–CAA–CCA-CCC

|←----------Ts/2----------→|←----------Ts/2----------→|

The gate pulse pattern for SSVM using Tables 8.1 to 8.3, rules 1 and 2 is shown in Table 8.6 below:

TABLE 8.6 SSVM Switching Pattern

Sl.No.	SV, SI	(SV+SI)	SSF_X HIGH	BIDIRECTIONAL SWITCH GATE PULSE PATTERN						
				t01	ta	tb	t02	tc	td	t03
1	1, 1 or 4, 4	Even	ssf1	CCC	ACC	AAC	AAA	AAB	ABB	BBB
2	1, 4 or 4, 1	Odd	ssf2	CCC	CCA	CAA	AAA	BAA	BBA	BBB
3	1, 5 or 4, 2	Even	ssf3	BBB	CBB	CCB	CCC	CCA	CAA	AAA
4	1, 2 or 4, 5	Odd	ssf4	BBB	BBC	BCC	CCC	ACC	AAC	AAA
5	1, 3 or 4, 6	Even	ssf5	AAA	BAA	BBA	BBB	BBC	BCC	CCC
6	1, 6 or 4, 3	Odd	ssf6	AAA	AAB	ABB	BBB	CBB	CCB	CCC
7	2, 4 or 5, 1	Even	ssf7	CCC	CCA	ACA	AAA	ABA	BBA	BBB
8	2, 1 or 5, 4	Odd	ssf8	CCC	CAC	AAC	AAA	AAB	BAB	BBB
9	2, 2 or 5, 5	Even	ssf9	BBB	BBC	CBC	CCC	CAC	AAC	AAA
10	2, 5 or 5, 2	Odd	ssf10	BBB	BCB	CCB	CCC	CCA	ACA	AAA
11	2, 6 or 5, 3	Even	ssf11	AAA	AAB	BAB	BBB	BCB	CCB	CCC
12	2, 3 or 5, 6	Odd	ssf12	AAA	ABA	BBA	BBB	BBC	CBC	CCC
13	3, 1 or 6, 4	Even	ssf13	CCC	CAC	CAA	AAA	BAA	BAB	BBB
14	3, 4 or 6, 1	Odd	ssf14	CCC	ACC	ACA	AAA	ABA	ABB	BBB
15	3, 5 or 6, 2	Even	ssf15	BBB	BCB	BCC	CCC	ACC	ACA	AAA
16	3, 2 or 6, 5	Odd	ssf16	BBB	CBB	CBC	CCC	CAC	CAA	AAA
17	3, 3 or 6, 6	Even	ssf17	AAA	ABA	ABB	BBB	CBB	CBC	CCC
18	3, 6 or 6, 3	Odd	ssf18	AAA	BAA	BAB	BBB	BCB	BCC	CCC

8.3 MODEL OF DIRECT ASYMMETRICAL SPACE VECTOR MODULATED THREE PHASE MATRIX CONVERTER: The SIMULINK model of the Direct Asymmetrical Space Vector Modulated (DASVM) three phase AC to three phase AC MC is shown in Fig. 8.3. The power circuit of the model is developed using the SimPowerSystems blockset in SIMULINK [51]. This mainly consists of three phase AC voltage source, bidirectional switch matrix, output filter and R-L load. The arrangement of the bidirectional switch matrix using IGBTs is the same as shown in Fig. 3.2 of Chapter III.

The modulation algorithm is developed in several sub units using Embedded MATLAB Function, MATLAB Function, Math Function, Logical and Bit Operator and using Sources block set in SIMULINK [51]. The various sub units are explained below:

8.3.1 DUTY-CYCLE SEQUENCE AND SECTOR SWITCH FUNCTION GENERATOR: This is developed using Embedded MATLAB Function block in SIMULINK, as shown in Fig. 8.3 . With peak line to neutral input voltage, desired peak output phase voltage, input frequency, output frequency, time, angular frequency of reference frame ωc as input parameters, the three phase output voltage can be resolved into dq-axis component voltages [42] and the absolute value of the angle of the output phase voltage, vout_angle can be calculated using the function atan2(voq,vod). Using input voltage and input phase displacement angle, a similar procedure is used to calculate the absolute value of the input current angle, i_in_angle. The value of reference frame frequency ωc is zero. This is illustrated in Program segment I below:

```
PROGRAM SEGMENT  I
%%Narayanaswamy. P.R. Iyer
function [voa,vob,voc,ViA,ViB,ViC,q,voq,vod,Viq,Vid,vout_angle,i_in_angle,….] =
fcn(vom,fo,t,vim,fi,wc,phi_i,….)
voa = vom*sin(2*pi*fo*t);
vob = vom*sin(2*pi*fo*t - 2*pi/(3));
voc = vom*sin(2*pi*fo*t + 2*pi/(3));
ViA = vim*sin(2*pi*fi*t);
ViB = vim*sin(2*pi*fi*t - 2*pi/(3));
ViC = vim*sin(2*pi*fi*t + 2*pi/(3));
%%phi_i is the input p.f. i.e.Iin_A = k*vim*sin(2*pi*fi*t - phi_i)
%%q is the ratio of vo/vi or vom/vim
q = vom/vim;
voq = (2/(3))*(voa*cos(wc*t)+ vob*cos(wc*t - (2*pi/(3))) + voc*cos(wc*t + (2*pi/(3))));
vod = (2/(3))*(voa*sin(wc*t)+ vob*sin(wc*t - (2*pi/(3))) + voc*sin(wc*t + (2*pi/(3))));
Viq = (2/(3))*(ViA*cos(wc*t)+ ViB*cos(wc*t - (2*pi/(3))) + ViC*cos(wc*t + (2*pi/(3))));
Vid = (2/(3))*(ViA*sin(wc*t)+ ViB*sin(wc*t - (2*pi/(3))) + ViC*sin(wc*t + (2*pi/(3))));
vout_angle = atan2(voq,vod);
i_in_angle = atan2(Viq,Vid);
```

These two values of vout_angle and i_in_angle are used to calculate the output voltage sector sv, input current sector si, α and β values for output voltage and input current using MATLAB function, REM functions and SUBTRACT modules.

Program segment II illustrates the MATLAB code for duty cycle sequencing and sector switch function generation. Duty-cycle dI, dII, dIII, dIV and d0 are calculated using equations 8.5 to 8.8 and 8.10 assuming unity input power factor. With (sv+si) even and odd, rule 1 and 2 for duty cycle are followed with zero vector duty cycle d0 introduced at the middle of the four duty cycles, dI, dII, dIII, dIV. This is used to calculate the timing A, B, C, D and E, by comparison of the cumulative sector timing with a triangle carrier Vtri as shown in Program Segment II. This triangle carrier Vtri has a period Ts, peak value Ts/2 Volts and minimum value zero, as shown in Fig. 8.4. Cumulative sector timing is obtained by appropriately adding the value of duty-ratio and multiplying by Ts/2, as per rules 1 and 2 given above. Sector switch functions ssf1 to ssf18 are determined using if-then-else statement. For example sector switch function ssf1 is HIGH only when sv = si =1 or sv = si = 4 and is LOW otherwise.

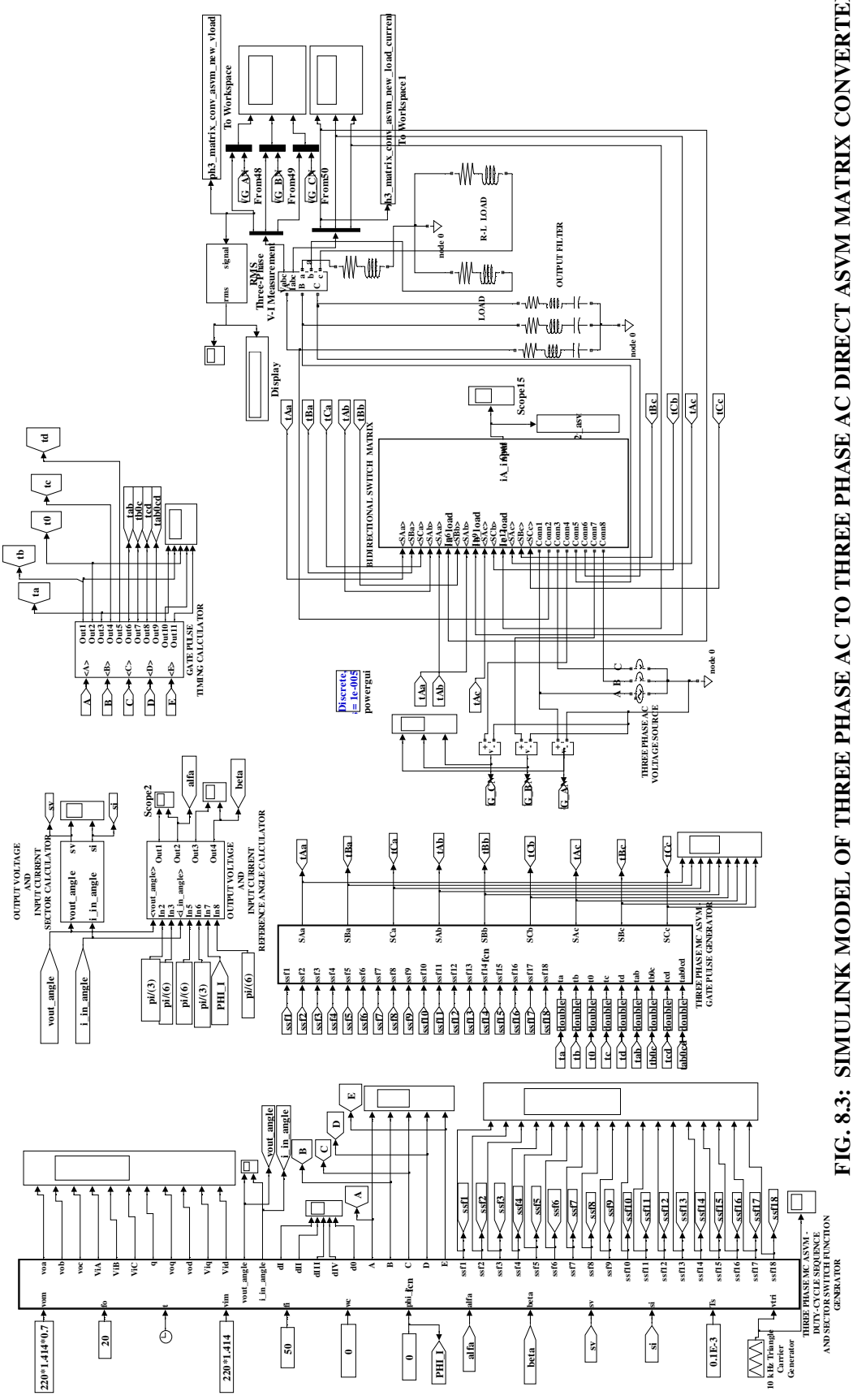


FIG. 8.3: SIMULINK MODEL OF THREE PHASE AC TO THREE PHASE AC DIRECT ASVM MATRIX CONVERTER

PROGRAM SEGMENT II

```
%%Narayanaswamy. P.R. Iyer
function(q,dI,dII,dIII,dIV,d0,A,B,C,D,E,ssf1,ssf2,ssf3,…ssf18) =
fcn(Vom,fo,t,Vim,fi,wc,ph_i,alfa,beta,sv,si,Ts,vtri)
q = Vom/Vim  %%Duty cycle calculations
dI = (2*q*cos(alfa - pi/(3))*cos(beta - pi/(3))/(sqrt(3)*cos(phi_i)));
dII = (2*q*cos(alfa - pi/(3))*cos(beta + pi/(3))/(sqrt(3)*cos(phi_i)));
dIII = (2*q*cos(alfa+ pi/(3))*cos(beta - pi/(3))/(sqrt(3)*cos(phi_i)));
dIV =(2*q*cos(alfa+pi/(3))*cos(beta + pi/(3))/(sqrt(3)*cos(phi_i)));
d0 = (1 - dI - dII - dIII - dIV);
if (rem((sv+si),2) == 0) %%even sequence
    if ( vtri <= dIII*Ts/(2))
    A = 1;    else
    A = 0;
    end
    if ( vtri <= (dIII + dI)*Ts/(2))
    B = 1;    else
    B = 0;
    end
    if ( vtri <= (dIII + dI + d0)*Ts/(2))
    C = 1;    else
    C = 0;
    end
    if ( vtri <= (dIII + dI + d0 + dII)*Ts/(2))
    D = 1;    else
    D = 0;
    end
    if ( vtri <= (dIII + dI + d0 + dII + dIV)*Ts/(2))
    E = 1;    else
    E = 0;
    end
else
    if ( vtri <= dI*Ts/(2)) %%odd sequence
    A = 1;    else
    A = 0;
    end
    if ( vtri <= (dIII + dI)*Ts/(2))
    B = 1;    else
    B = 0;
    end
    if ( vtri <= (dIII + dI + d0)*Ts/(2))
    C = 1;    else
    C = 0;
    end
    if ( vtri <= (dIII + dI + d0 + dIV)*Ts/(2))
    D = 1;    else
    D = 0;
    end
    if ( vtri <= (dIII + dI + d0 + dII + dIV)*Ts/(2))
    E = 1;    else
    E = 0;
    end
end
if (sv == 1 && si == 1 || sv == 4 && si == 4)
    ssf1 = 1; else
    ssf1 = 0;
end
if ( sv == 4 && si == 1  ||  sv == 1 && si == 4 )
    ssf2 = 1; else
    ssf2 = 0;
end
%%similar statements for ssf3 to ssf18.
.
.
.
if ( sv == 3 && si == 6  ||  sv == 6 && si == 3 )
   ssf18 = 1; else
    ssf18 = 0;
end
```

PROGRAM SEGMENT III

```
function [y] = fcn(u)
%%Narayanaswamy. P.R. Iyer
vout_angle = u(1);
i_in_angle = u(2);
if (vout_angle > -pi && vout_angle <= -2*pi/(3))
    y(1) = 4;
else if (vout_angle > -2*pi/(3) && vout_angle <=
-pi/(3))
       y(1) = 5;
else if (vout_angle > -pi/(3) && vout_angle <= 0)
          y(1) = 6;
else if (vout_angle > 0 && vout_angle <= pi/(3))
             y(1) = 1;
else if (vout_angle > pi/(3) && vout_angle <=
2*pi/(3))
                y(1) = 2;
else if (vout_angle > 2*pi/(3) && vout_angle <=
pi)
                   y(1) = 3;
                end
             end
          end
       end
    end
end
if (i_in_angle > -pi && i_in_angle <= -2*pi/(3))
    y(2) = 4;
else if (i_in_angle > -2*pi/(3) && i_in_angle <=
 -pi/(3))
       y(2) = 5;
else if (i_in_angle > -pi/(3) && i_in_angle <= 0)
          y(2) = 6;
else if (i_in_angle > 0 && i_in_angle <= pi/(3))
             y(2) = 1;
else if (i_in_angle > pi/(3) && i_in_angle <=
2*pi/(3))
                y(2) = 2
else if (i_in_angle > 2*pi/(3) && i_in_angle <= pi)
                   y(2) = 3;
                end
             end
          end
       end
    end
end
sv = y(1);
si = y(2);
```

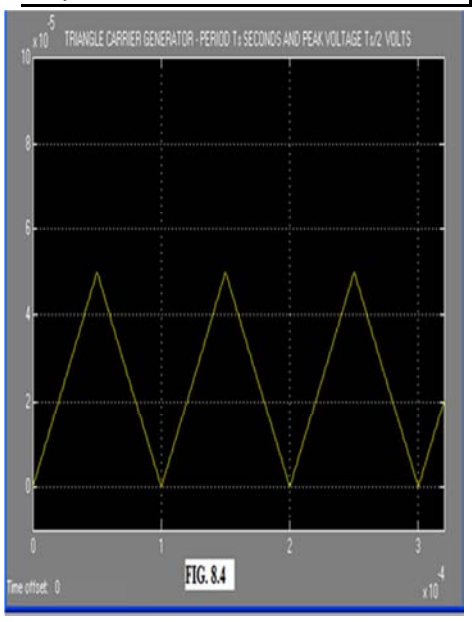


FIG. 8.4

8.3.2 OUTPUT VOLTAGE AND INPUT CURRENT SECTOR CALCULATOR: This is developed using MATLAB Function, a mux and a demux as shown in Fig. 8.5. The input to the mux are vout_angle and i_in_angle. The output from the demux are SV and SI. The source code to determine SV and SI is shown in Program Segment III.

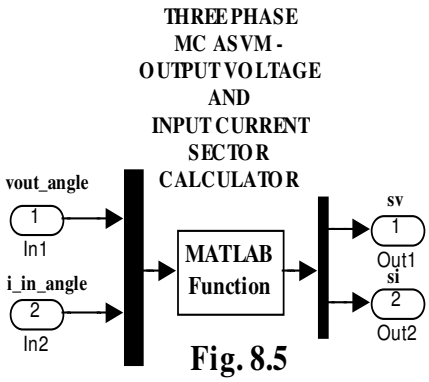


Fig. 8.5

8.3.3 OUTPUT VOLTAGE AND INPUT CURRENT REFERENCE ANGLE CALCULATOR: This is shown in Fig. 8.6. This uses two REM function blocks and SUBTRACT modules. The first REM block has the inputs v_out_angle and pi/(3). The second REM block has the inputs i_in_angle and pi/(3). The output of the first REM block is subtracted from pi/(6) to obtain angle alfa defined in Fig. 8.2(A). The output of the second REM block is subtracted from pi/(6), input p.f. angle phi_i and once again from pi/(6) to obtain beta as per the configuration defined in Fig. 8.2(B).

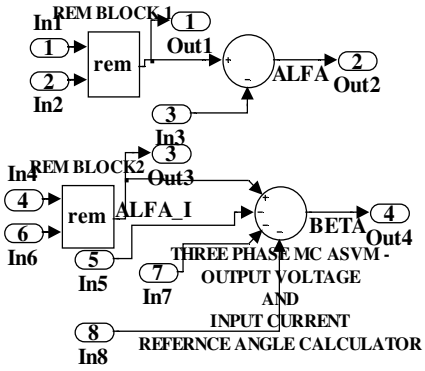


Fig. 8.6

8.3.4 GATE PULSE TIMING CALCULATOR: This is shown in Fig. 8.7. The inputs in1 to in5 are A, B, C, D and E respectively. The individual gate pulse timing, ta, tb, t0, tc and td are respectively dIII*Ts/(2), dI*Ts/(2), d0*Ts/(2), dII*Ts/(2) and dIV*Ts/(2) when (SV+SI) is even and dI*Ts/(2), dIII*Ts/(2), d0*Ts/(2), dIV*Ts/(2) and dII*Ts/(2) when (SV+SI) is odd. This individual gate pulse duration is obtained as shown in equation 8.11 below:

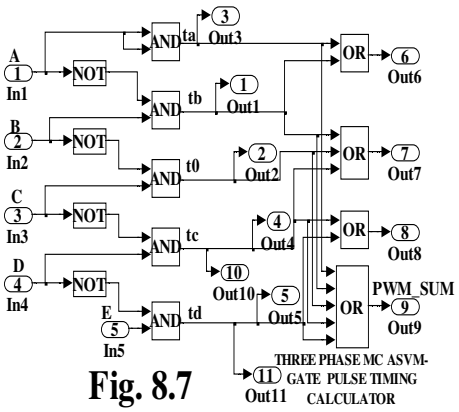


Fig. 8.7

$$t_a = (A \,\&\, A)$$
$$t_b = (\sim A \,\&\, B)$$
$$t_0 = (\sim B \,\&\, C)$$
$$t_c = (\sim C \,\&\, D)$$
$$t_d = (\sim D \,\&\, E) \ldots \qquad (8.11)$$

In equation 8.11, symbols (&) represents logical AND and (~) represents NOT operation respectively. To easily generate the MC gate pulse, the timing pulse in equation 8.11 are given to OR gates to obtain the following additional timing pulse:

$$t_{ab} = (t_a || t_b)$$

$$t_{b0c} = (t_b||t_0||t_c)$$
$$t_{cd} = (t_c||t_d)$$
$$t_{ab0cd} = (t_a||t_b||t_0||t_c||t_d) \ldots\ldots (8.12)$$

In equation 8.12, symbol (||) represents logical OR operation.

The complete gate timing for the nine bidirectional switches using Direct ASVM algorithm is given in Table 8.5 below:

TABLE 8.5: ASVM Gate Pulse Timing

Sl. No	SV,SI	SSF_X HIGH	SAa	SBa	SCa	SAb	SBb	SCb	SAc	SBc	SCc
1	1, 1 or 4, 4	ssf1	tab0cd	0	0	tb0c	td	ta	t0	tcd	tab
2	1, 4 or 4, 1	ssf2	t0	tcd	tab	tb0c	td	ta	tab0cd	0	0
3	1, 5 or 4, 2	ssf3	0	0	tab0cd	td	ta	tb0c	tcd	tab	t0
4	1, 2 or 4, 5	ssf4	tcd	tab	t0	td	ta	tb0c	0	0	tab0cd
5	1, 3 or 4, 6	ssf5	0	tab0cd	0	ta	tb0c	td	tab	t0	tcd
6	1, 6 or 4, 3	ssf6	tab	t0	tcd	ta	tb0c	td	0	tab0cd	0
7	2, 4 or 5, 1	ssf7	tb0c	td	ta	t0	tcd	tab	tab0cd	0	0
8	2, 1 or 5, 4	ssf8	tb0c	td	ta	tab0cd	0	0	t0	tcd	tab
9	2, 2 or 5, 5	ssf9	td	ta	tb0c	tcd	tab	t0	0	0	tab0cd
10	2, 5 or 5, 2	ssf10	td	ta	tb0c	0	0	tab0cd	tcd	tab	t0
11	2, 6 or 5, 3	ssf11	ta	tb0c	td	tab	t0	tcd	0	tab0cd	0
12	2, 3 or 5, 6	ssf12	ta	tb0c	td	0	tab0cd	0	tab	t0	tcd
13	3, 1 or 6, 4	ssf13	t0	tcd	tab	tab0cd	0	0	tb0c	td	ta
14	3, 4 or 6, 1	ssf14	tab0cd	0	0	t0	tcd	tab	tb0c	td	ta
15	3, 5 or 6, 2	ssf15	tcd	tab	t0	0	0	tab0cd	td	ta	tb0c
16	3, 2 or 6, 5	ssf16	0	0	tab0cd	tcd	tab	t0	td	ta	tb0c
17	3, 3 or 6, 6	ssf17	tab	t0	tcd	0	tab0cd	0	ta	tb0c	td
18	3, 6 or 6, 3	ssf18	0	tab0cd	0	tab	t0	tcd	ta	tb0c	td

8.3.5 GATE PULSE GENERATOR: The gate pulse generator for the MC is developed using Embedded MATLAB as shown in Fig. 8.3. The sector switch functions ssf1 to ssf18, gate pulse timing calculator outputs defined in equations 8.11 and 8.12 form the input modules and the outputs are the gate pulses for the nine bidirectional switches of the MC. In Table 8.5, the gate timing for the nine bidirectional switches are shown. The gate timing for switch SAa can be combined by logically ANDing the respective value with sector switch function ssf_x and ORing the value for each sector. Thus the gate timing pulse for switch SAa can be expressed as in equation 8.13 below:

$$SAa = ssf1\&(tab0cd)||ssf2\&(t0)|| \ldots ||ssf18\&(0).. (8.13)$$

Program segment IV gives the method of generating the gate timing pulses for the nine bidirectional switches using the calculated sector timings given in Table 8.5.

8.4 SIMULATION RESULTS: The simulation of the Three Phase ASVM Matrix Converter was carried out in SIMULINK [51]. The parameters used for simulation are shown in Table 8.6. The ode15S(Stiff/NDF) solver was used. Simulation of the above three phase AC to three phase AC direct

ASVM of MC was carried out for two different output frequencies with all other parameters constant. The simulation results of the harmonic spectrum of line to neutral output voltage, input current, load current and line to line output voltage for a 50 Hz AC output voltage are shown in Fig. 8.8(A) to (D) and the oscilloscope wave of the above in order are shown in Fig. 8.9(A) to (D). Similarly the harmonic spectrum of the above in order for a 20 Hz AC output voltage are shown in Fig. 8.10(A) to (D) and the oscilloscope waveform of the above in order are shown in Fig. 8.11(A) to (D). The simulation results are tabulated in Table 8.7.

TABLE 8.6: Model Parameters

Sl.No.	Parameter	Value	Unit
1	RMS Line to Neutral Input Voltage	220	V
2	Input Frequency fi	50	Hz
3	Modulation Index q	0.7	--
4	Output Frequency fo	50, 20	Hz
5	Carrier Sampling Frequency fsw	10	kHz
6	R-L-C Output Filter	10, 0.01e-3, 25.356e-6	Ω, H, F
7	R-L Load	100, 500e-3	Ω, H
8	Input Phase Displacement φi	0	Radians

PROGRAM SEGMENT IV

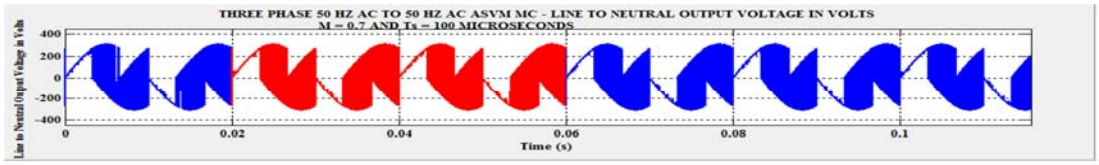
```
function [SAa,SBa,SCa,SAb,SBb,SCb,SAc,SBc,SCc] =
fcn(ssf1,ssf2,ssf3,ssf4,ssf5,ssf6,ssf7,ssf8,ssf9,ssf10,ssf11,ssf12,ssf13,ssf14,ssf15,ssf16,ssf17,ssf18,ta,
tb,t0,tc,td,tab,tb0c,tcd,tab0cd)
%%Narayanaswamy. P.R.Iyer.
SAa = ssf1&(tab0cd)||ssf2&(t0)||ssf3&(0)||ssf4&(tcd)||ssf5&(0)||ssf6&(tab)||ssf7&(tb0c)||ssf8&(tb0c)||ssf9&
(td)||ssf10&(td)||ssf11&(ta)||ssf12&(ta)||ssf13&(t0)||ssf14&(tab0cd)||ssf15&(tcd)||ssf16&(0)||ssf17& (tab)||ssf18&(0);
SBa = ssf1&(0)||ssf2&(tcd)||ssf3&(0)||ssf4&(tab)||ssf5&(tab0cd)||ssf6&(t0)||ssf7&(td)||ssf8&(td)||ssf9&(ta)||
ssf10&(ta)||ssf11&(tb0c)||ssf12&(tb0c)||ssf13&(tcd)||ssf14&(0)||ssf15&(tab)||ssf16&(0)||ssf17&(t0)|| ssf18&(tab0cd);
SCa = ssf1&(0)||ssf2&(tab)||ssf3&(tab0cd)||ssf4&(t0)||ssf5&(0)||ssf6&(tcd)||ssf7&(ta)||ssf8&(ta)||ssf9&(tb0c)
||ssf10&(tb0c)||ssf11&(td)||ssf12&(td)||ssf13&(tab)||ssf14&(0)||ssf15&(t0)||ssf16&(tab0cd)||ssf17& (tcd)||ssf18&(0);
SAb = ssf1&(tb0c)||ssf2&(tb0c)||ssf3&(td)||ssf4&(td)||ssf5&(ta)||ssf6&(ta)||ssf7&(t0)||ssf8&(tab0cd)||ssf9&
(tcd)||ssf10&(0)||ssf11&(tab)||ssf12&(0)||ssf13&(tab0cd)||ssf14&(t0)||ssf15&(0)||ssf16&(tcd)||ssf17& (0)||ssf18&(tab);
SBb = ssf1&(td)||ssf2&(td)||ssf3&(ta)||ssf4&(ta)||ssf5&(tb0c)||ssf6&(tb0c)||ssf7&(tcd)||ssf8&(0)||ssf9&(tab)||
ssf10&(0)||ssf11&(t0)||ssf12&(tab0cd)||ssf13&(0)||ssf14&(tcd)||ssf15&(0)||ssf16&(tab)||ssf17& (tab0cd)||ssf18&(t0);
SCb = ssf1&(ta)||ssf2&(ta)||ssf3&(tb0c)||ssf4&(tb0c)||ssf5&(td)||ssf6&(td)||ssf7&(tab)||ssf8&(0)||ssf9&(t0)||
ssf10&(tab0cd)||ssf11&(tcd)||ssf12&(0)||ssf13&(0)||ssf14&(tab)||ssf15&(tab0cd)||ssf16&(t0)||ssf17& (0)||ssf18&(tcd);
SAc = ssf1&(t0)||ssf2&(tab0cd)||ssf3&(tcd)||ssf4&(0)||ssf5&(tab)||ssf6&(0)||ssf7&(tab0cd)||ssf8&(t0)||ssf9&
(0)||ssf10&(tcd)||ssf11&(0)||ssf12&(tab)||ssf13&(tb0c)||ssf14&(tb0c)||ssf15&(td)||ssf16&(td)||ssf17& (ta)||ssf18&(ta);
SBc = ssf1&(tcd)||ssf2&(0)||ssf3&(tab)||ssf4&(0)||ssf5&(t0)||ssf6&(tab0cd)||ssf7&(0)||ssf8&(tcd)||ssf9&(0)||
ssf10&(tab)||ssf11&(tab0cd)||ssf12&(t0)||ssf13&(td)||ssf14&(td)||ssf15&(ta)||ssf16&(ta)||ssf17&(tb0c)||ssf18&(tb0c);
SCc = ssf1&(tab)||ssf2&(0)||ssf3&(t0)||ssf4&(tab0cd)||ssf5&(tcd)||ssf6&(0)||ssf7&(0)||ssf8&(tab)||ssf9&
(tab0cd)||ssf10&(t0)||ssf11&(0)||ssf12&(tcd)||ssf13&(ta)||ssf14&(ta)||ssf15&(tb0c)||ssf16&(tb0c)|| ssf17&(td)||ssf18&(td);
```

TABLE 8.7: ASVM Simulation Results 1

Sl.No.	Three Phase ASVM MC Input – Output Frequency Hz	Line to Line Output Voltage THD p.u.	Line to Neutral Output Voltage THD p.u.	Input Current THD p.u.	Load Current THD p.u.
1)	50 – 50	1.0271	1.6083	1.9736	0.2926
2)	50 – 20	0.9559	1.1765	1.4765	0.3678

8.5 MODEL OF DIRECT SYMMETRICAL SPACE VECTOR MODULATED THREE PHASE MATRIX CONVERTER: The SIMULINK model of the Direct Symmetrical Space Vector Modulated (DSSVM) three phase AC to three phase AC MC is shown in Fig. 8.12. The power circuit of the model is developed using the SimPowerSystems blockset in SIMULINK [51]. This mainly consists of three phase AC voltage source, bidirectional switch matrix, output filter and R-L load. The arrangement of the bidirectional switch matrix using IGBTs is the same as shown in Fig. 3.2 of Chapter III.

The modulation algorithm is developed in several sub units using Embedded MATLAB Function,



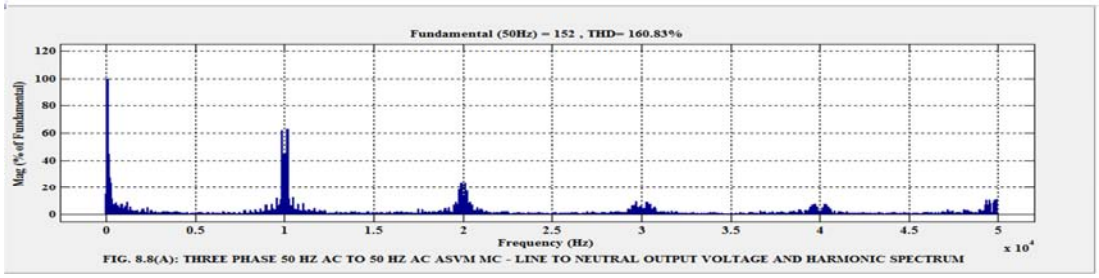
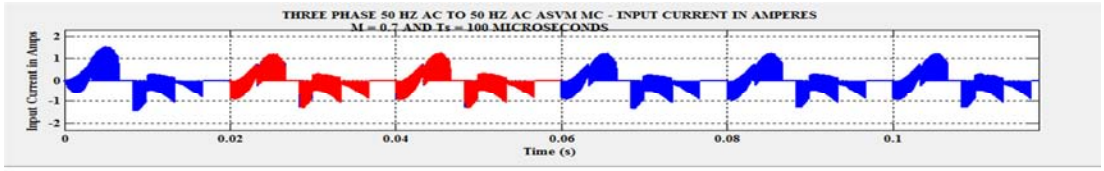


FIG. 8.8(A): THREE PHASE 50 HZ AC TO 50 HZ AC ASVM MC - LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM



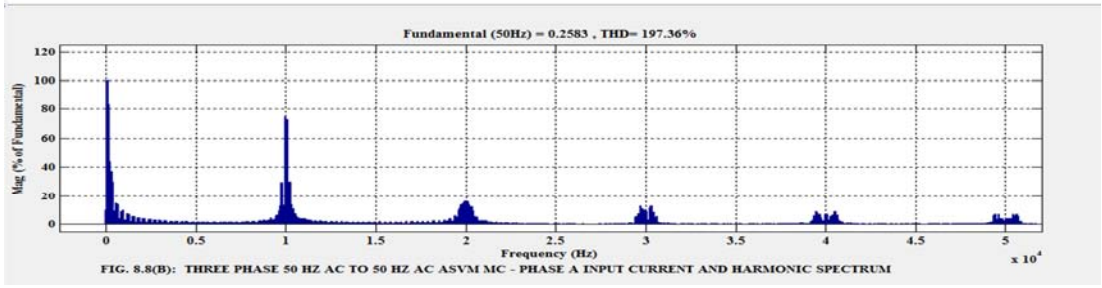
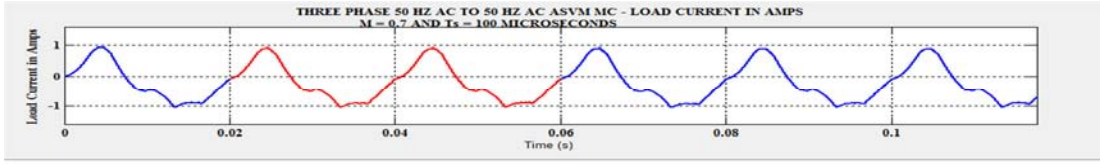


FIG. 8.8(B): THREE PHASE 50 HZ AC TO 50 HZ AC ASVM MC - PHASE A INPUT CURRENT AND HARMONIC SPECTRUM



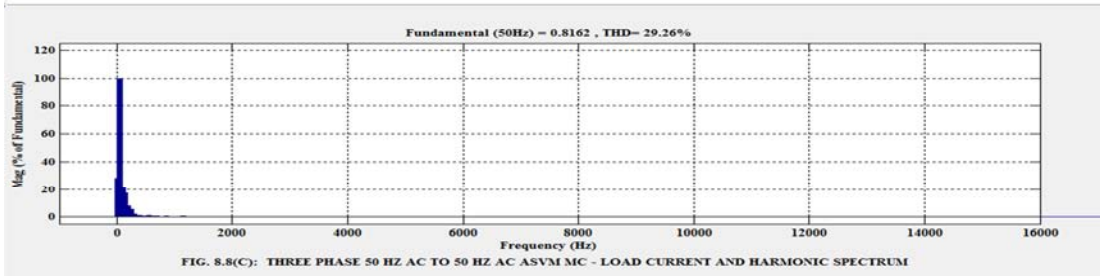
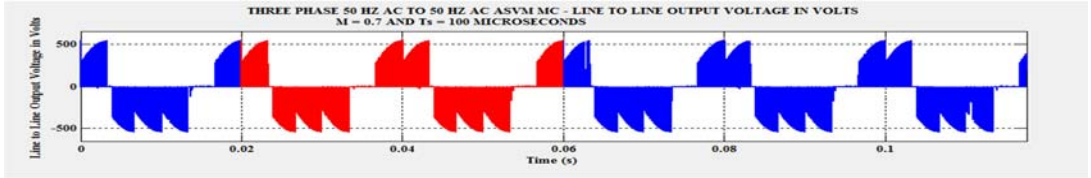


FIG. 8.8(C): THREE PHASE 50 HZ AC TO 50 HZ AC ASVM MC - LOAD CURRENT AND HARMONIC SPECTRUM



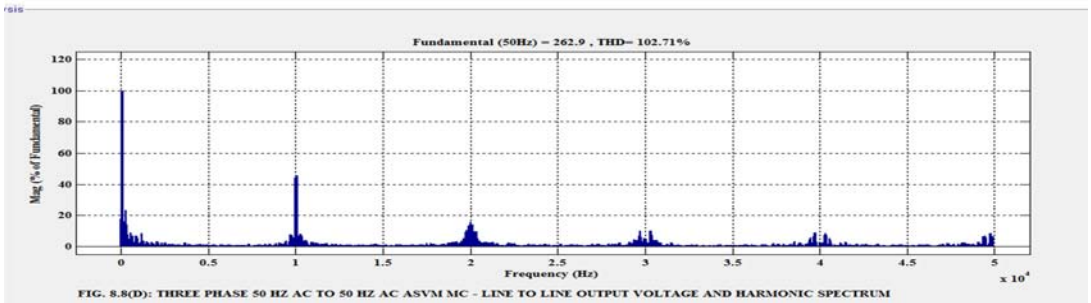


FIG. 8.8(D): THREE PHASE 50 HZ AC TO 50 HZ AC ASVM MC - LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM

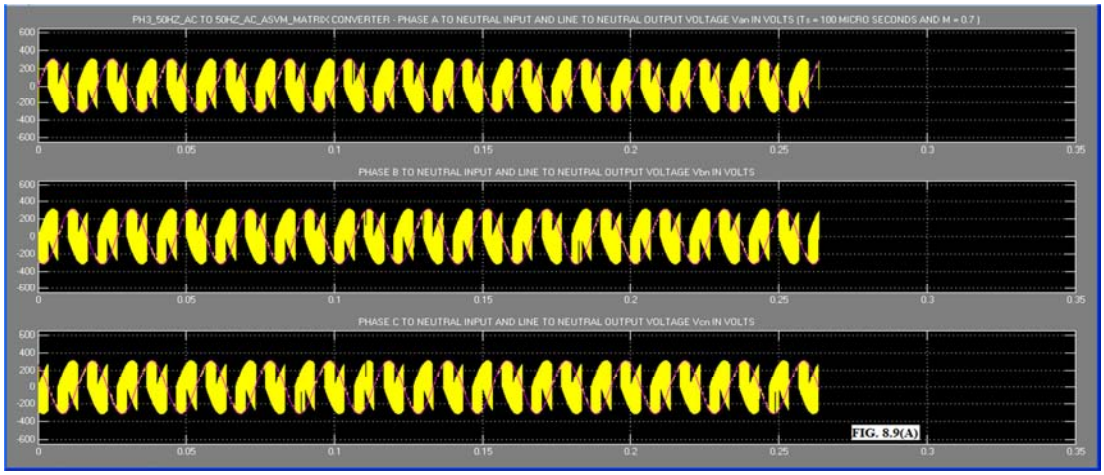


FIG. 8.9(A)

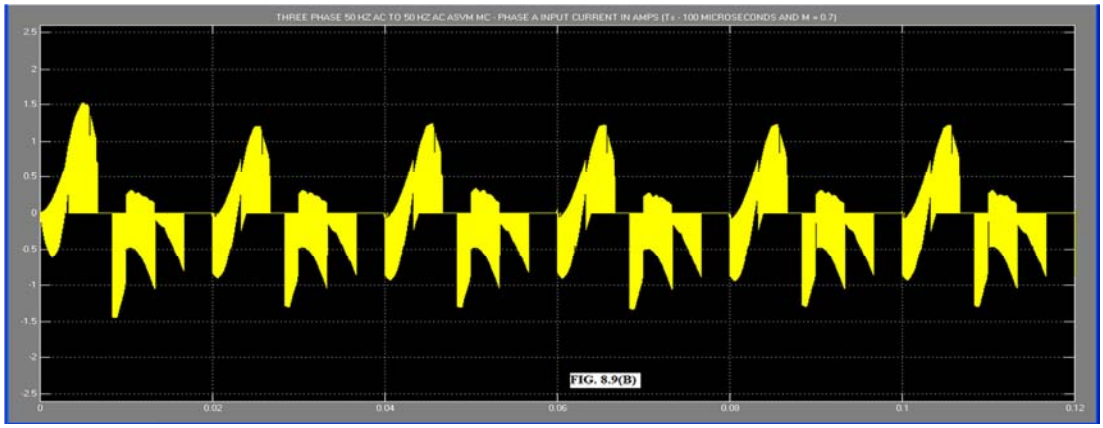


FIG. 8.9(B)

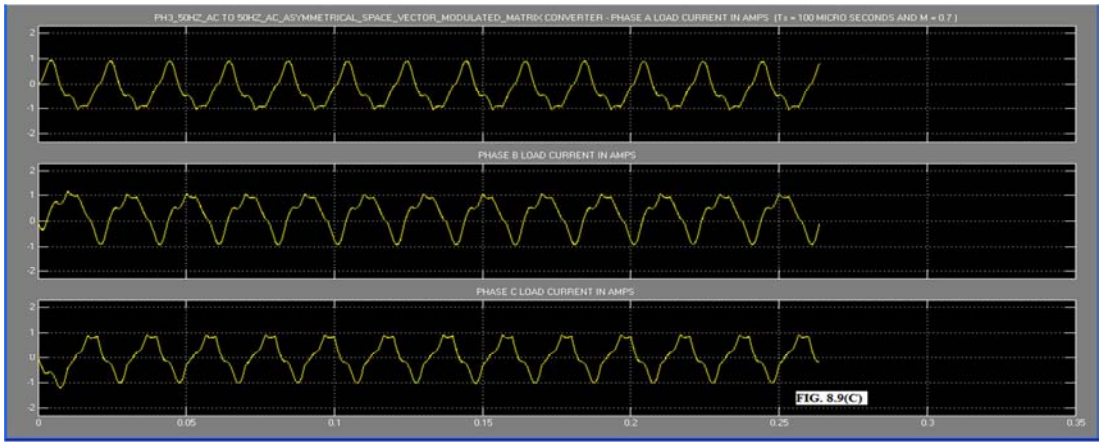


FIG. 8.9(C)

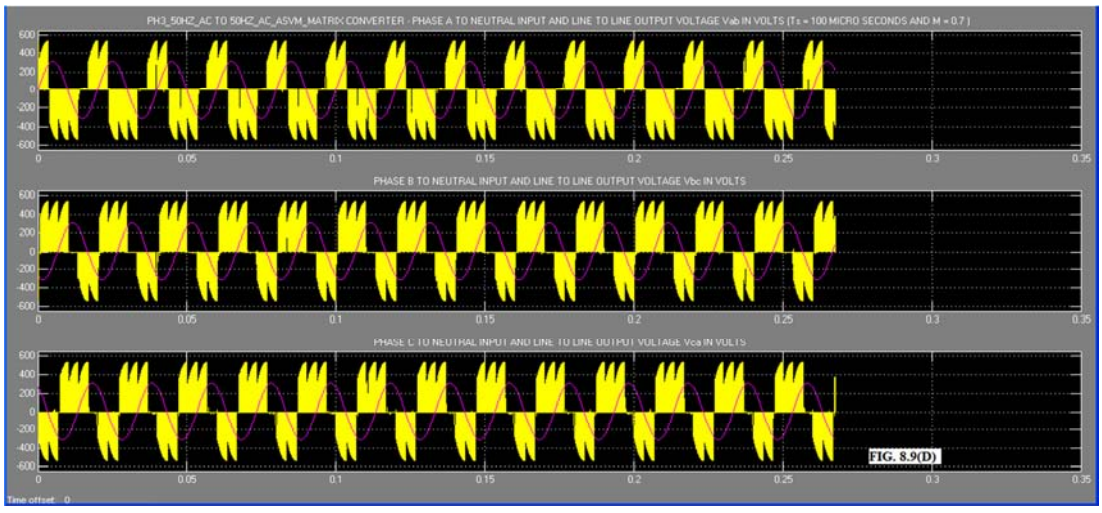
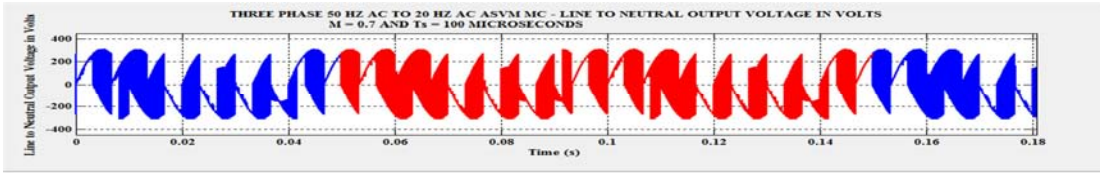


FIG. 8.9(D)



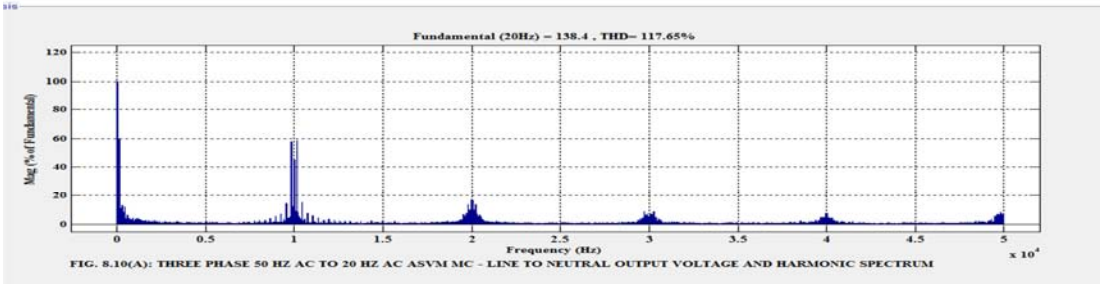
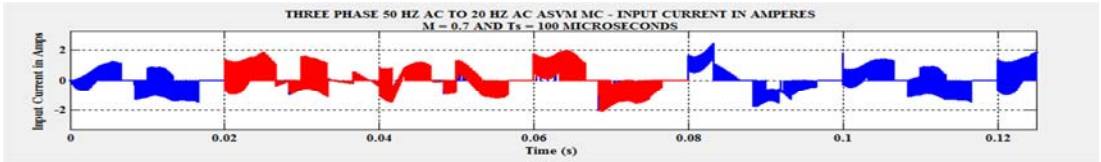


FIG. 8.10(A): THREE PHASE 50 HZ AC TO 20 HZ AC ASVM MC - LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM



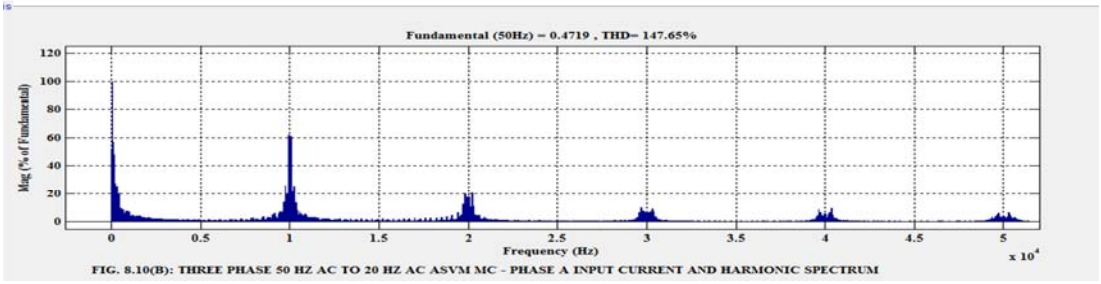
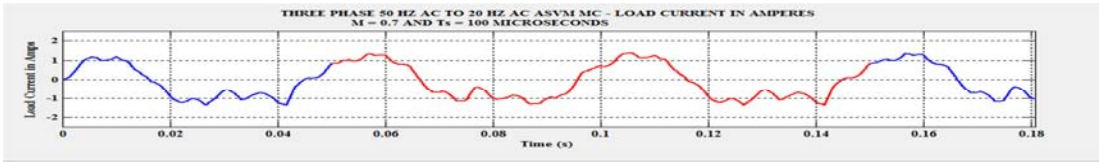


FIG. 8.10(B): THREE PHASE 50 HZ AC TO 20 HZ AC ASVM MC - PHASE A INPUT CURRENT AND HARMONIC SPECTRUM



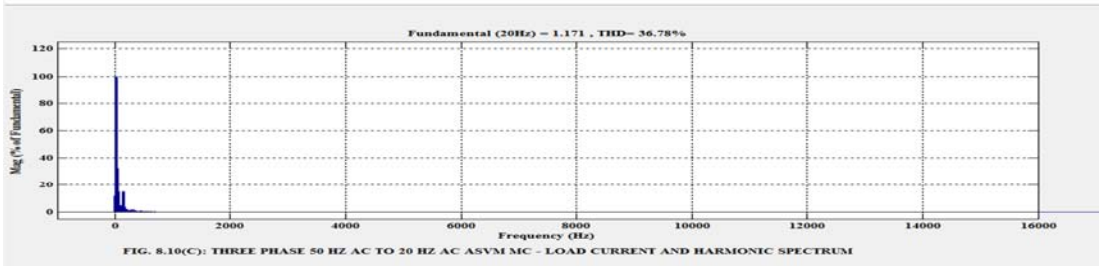
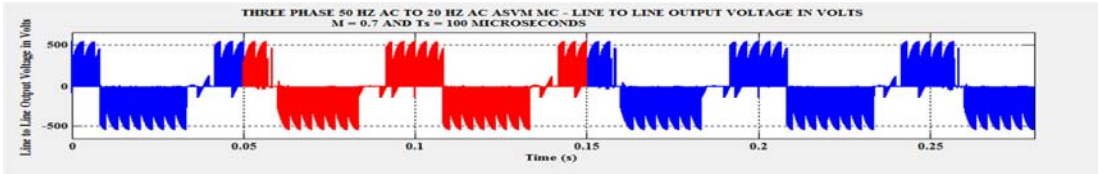


FIG. 8.10(C): THREE PHASE 50 HZ AC TO 20 HZ AC ASVM MC - LOAD CURRENT AND HARMONIC SPECTRUM



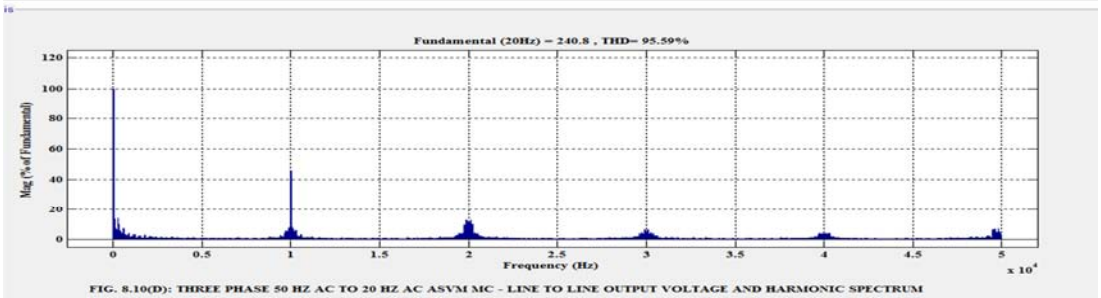
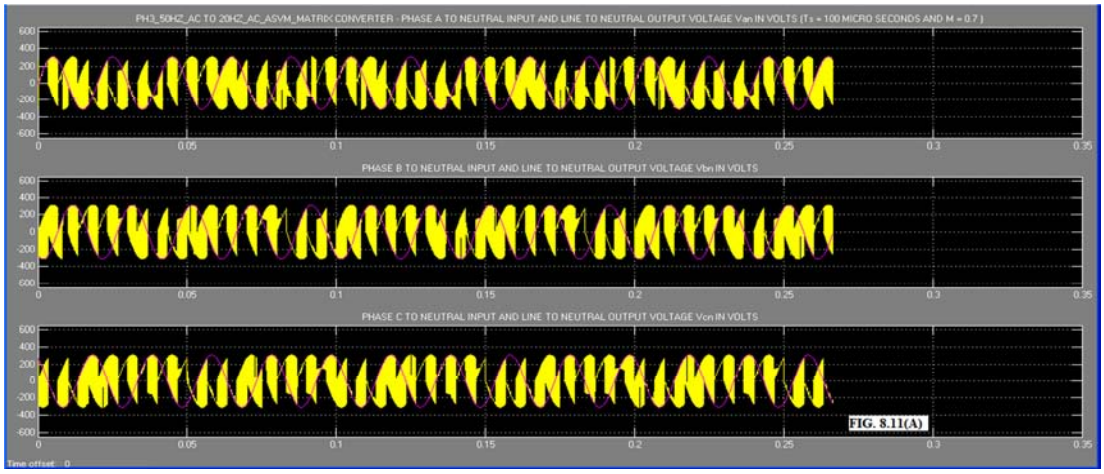
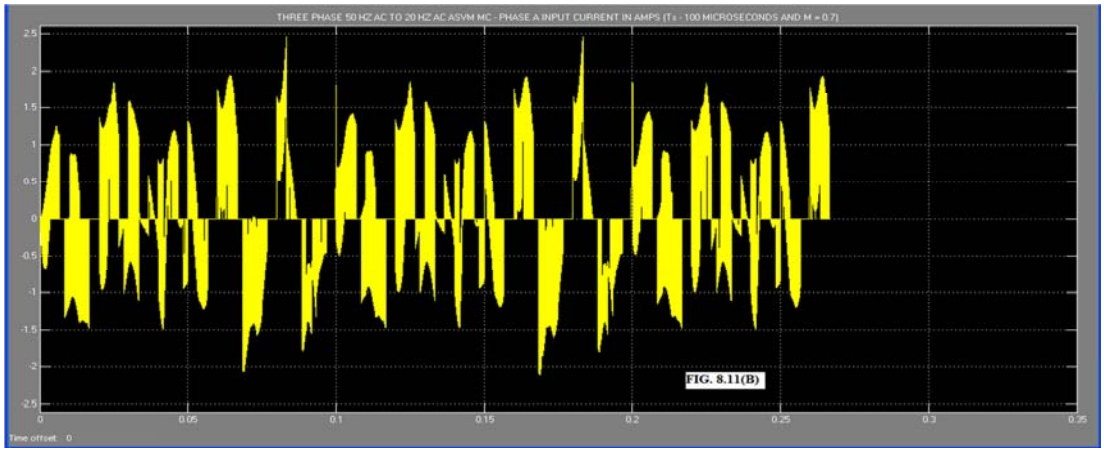
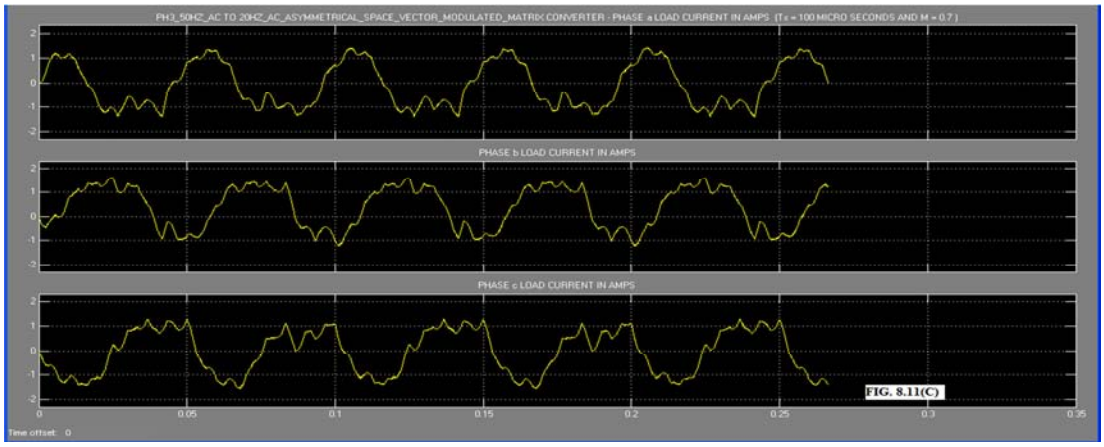


FIG. 8.10(D): THREE PHASE 50 HZ AC TO 20 HZ AC ASVM MC - LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM


PH3_50HZ_AC TO 20HZ_AC_ASVM_MATRIX CONVERTER - PHASE A TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Van IN VOLTS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vbn IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vcn IN VOLTS
FIG. 8.11(A)


THREE PHASE 50 HZ AC TO 20 HZ AC ASVM MC - PHASE A INPUT CURRENT IN AMPS (Ts = 100 MICROSECONDS AND M = 0.7)
FIG. 8.11(B)


PH3_50HZ_AC TO 20HZ_AC_ASYMMETRICAL_SPACE_VECTOR_MODULATED_MATRIX CONVERTER - PHASE a LOAD CURRENT IN AMPS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE b LOAD CURRENT IN AMPS
PHASE c LOAD CURRENT IN AMPS
FIG. 8.11(C)


PH3_50HZ_AC TO 20HZ_AC_ASVM_MATRIX CONVERTER - PHASE A TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vab IN VOLTS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vbc IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vca IN VOLTS
FIG. 8.11(D)

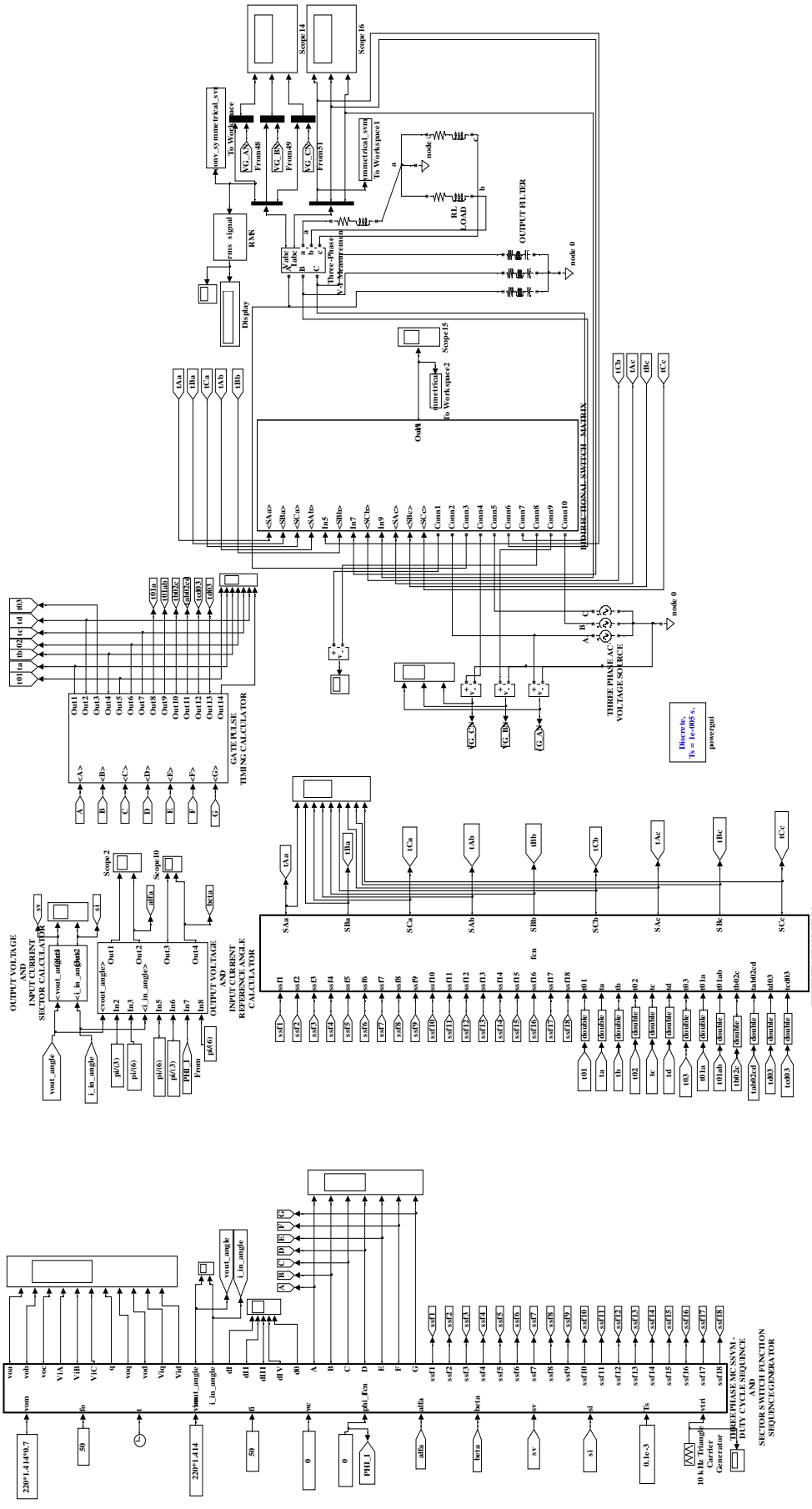


FIG. 8.12: SIMULINK MODEL OF THREE PHASE AC TO THREE PHASE AC SSVM MATRIX CONVERTER

MATLAB Function, Math Function, Logical and Bit Operator and using Sources block set in SIMULINK [51]. The various sub units are explained below:

8.5.1 DUTY-CYCLE SEQUENCE AND SECTOR SWITCH FUNCTION GENERATOR: This is developed using Embedded MATLAB Function block in SIMULINK, as shown in Fig. 8.12. With peak line to neutral input voltage, desired peak output phase voltage, input frequency, output frequency, time, angular frequency of reference frame ωc as input parameters, the three phase output voltage can be resolved into dq-axis component voltages [42] and the absolute value of the angle of the output phase voltage, vout_angle can be calculated using the function atan2(voq,vod). Using input voltage and input phase displacement angle, a similar procedure is used to calculate the absolute value of the input current angle, i_in_angle. The value of reference frame frequency ωc is zero. This is illustrated in Program segment I in Section 8.3.1 above. These two values of the angles are used to calculate the output voltage sector sv, input current sector si, α and β values for output voltage and input current using MATLAB function, REM functions and SUBTRACT modules. Program segment V illustrates the MATLAB code for duty cycle sequencing and sector switch function generation. Duty-cycle dI, dII, dIII, dIV and d0 are calculated using equations 8.5 to 8.8 and 8.10 , assuming unity input power factor. With (sv+si) even and odd, rule 1 and 2 for duty cycle are followed with zero vector duty cycle (d0/3) introduced at the start, middle and at the end of the four duty cycles, dI, dII, dIII, dIV. This is used to calculate the timing A, B, C, D, E, F and G, by comparison of the cumulative sector timing with a triangle carrier. This triangle carrier has a period Ts, peak value Ts/2 Volts and minimum value zero, as shown in Fig. 8.4. Cumulative sector timing is obtained by appropriately adding the value of duty-ratio and multiplying by Ts/2, as per rules 1 and 2 given above. Sector switch functions ssf1 to ssf18 are determined using if-then-else statement. For example sector switch function ssf1 is HIGH only when sv = si =1 or sv = si = 4 and is LOW otherwise.

8.5.2 OUTPUT VOLTAGE AND INPUT CURRENT SECTOR CALCULATOR: This is developed using MATLAB Function, a mux and a demux as shown in Fig. 8.5 above. The input to the mux are vout_angle and i_in_angle. The output from the demux are SV and SI. The source code to determine SV and SI is shown in Program Segment III above.

8.5.3 OUTPUT VOLTAGE AND INPUT CURRENT REFERENCE ANGLE CALCULATOR: This is shown in Fig. 8.6 above. This uses two REM function blocks and SUBTRACT modules. The first REM block has the inputs v_out_angle and pi/(3). The second REM block has the inputs i_in_angle and pi/(3). The output of the first REM block is subtracted from pi/(6) to obtain angle alfa defined in Fig. 8.2(A). The output of the second REM block is subtracted from pi/(6), input p.f. angle phi_i and once again from pi/(6) to obtain beta as per the configuration defined in Fig. 8.2(B).

8.5.4 GATE PULSE TIMING CALCULATOR: This is shown in Fig. 8.13. The inputs in1 to in7 are A, B, C, D, E, F and G respectively. The individual gate pulse timing, t01, ta, tb, t02, tc, td and

```
%%PROGRAM SEGMENT  V
%%NARAYANASWAMY. P.R. IYER
function(q,dI,dII,dIII,dIV,d0,A,B,C,D,E,ssf1,ssf2,ssf3,…ssf18)= fcn(Vom,fo,t,Vim,fi,wc,ph_i,alfa,beta,sv,si,Ts,vtri)
q = Vom/Vim  %%Duty cycle calculations
dI = (2*q*cos(alfa - pi/(3))*cos(beta - pi/(3))/(sqrt(3)*cos(phi_i)));
dII = (2*q*cos(alfa - pi/(3))*cos(beta + pi/(3))/(sqrt(3)*cos(phi_i)));
dIII = (2*q*cos(alfa + pi/(3))*cos(beta - pi/(3))/(sqrt(3)*cos(phi_i)));
dIV = (2*q*cos(alfa + pi/(3))*cos(beta + pi/(3))/(sqrt(3)*cos(phi_i)));
d0 = (1 - dI - dII - dIII - dIV);
if (rem((sv+si),2) == 0)
   %%even sequence
if ( vtri <= (d0/(3))*Ts/(2))
A = 1;    else
A = 0;
end
if ( vtri <= (dIII + d0/(3))*Ts/(2))
B = 1;    else
B = 0;
end
if ( vtri <= (dIII + dI + d0/(3))*Ts/(2))
C = 1;    else
C = 0;
end
if ( vtri <= (dIII + dI + d0/(3) + d0/(3))*Ts/(2))
D = 1;    else
D = 0;
end
if ( vtri <= (dIII + dI + d0/(3) + d0/(3) + dII)*Ts/(2))
E = 1;     else
E = 0;
end
if ( vtri <= (dIII + dI + d0/(3) + d0/(3) + dII + dIV)*Ts/(2))
F = 1;     else
F = 0;
end
if ( vtri <= (dIII + dI + d0/(3) + d0/(3) + d0/(3) + dII + dIV)*Ts/(2))
G = 1;    else
G = 0;
end
else
%%odd sequence
if ( vtri <= (d0/(3))*Ts/(2))
A = 1;    else
A = 0;
end
if ( vtri <= (dI + d0/(3))*Ts/(2))
B = 1;    else
B = 0;
end
if ( vtri <= (dIII + dI + d0/(3))*Ts/(2))
C = 1;     else
C = 0;
end
if ( vtri <= (dIII + dI + d0/(3) + d0/(3))*Ts/(2))
D = 1;     else
D = 0;
end
if ( vtri <= (dIII + dI + d0/(3) + d0/(3) + dIV)*Ts/(2))
E = 1;      else
E = 0;
end
if ( vtri <= (dIII + dI + d0/(3) + d0/(3) + dII + dIV)*Ts/(2))
F = 1;   else
F = 0;
end
if ( vtri <= (dIII + dI + d0/(3) + d0/(3) + d0/(3) + dII + dIV)*Ts/(2))
G = 1;   else
G = 0;
end
end
```

```
PROGRAM SEGEMNT V (CONTINUED)
%%NARAYANASWAMY. P.R. IYER
if (sv == 1 && si == 1 || sv == 4 && si == 4)
ssf1 = 1;   else
ssf1 = 0;
end
if ( sv == 4 && si == 1  ||  sv == 1 && si == 4 )
ssf2 = 1;   else
ssf2 = 0;
end
%%similar statements for ssf3 to ssf18.
.

.

if ( sv == 3 && si == 6  ||  sv == 6 && si == 3 )
ssf18 = 1; else
ssf18 = 0;
end
```

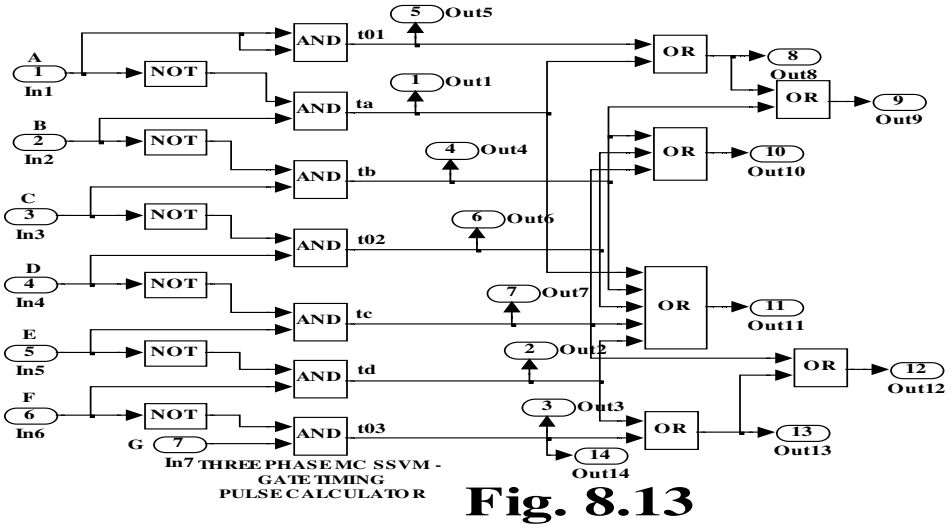


Fig. 8.13

t03 are respectively (d0/3)*Ts/2, dIII*Ts/(2), dI*Ts/(2), (d0/3)*Ts/(2), dII*Ts/(2), dIV*Ts/(2) and (d0/3)*Ts/2 when (SV+SI) is even and (d0/3)*Ts/2, dI*Ts/(2), dIII*Ts/(2), (d0/3)*Ts/2, dIV*Ts/(2), dII*Ts/(2) and (d0/3)*Ts/2 when (SV+SI) is odd. This individual gate pulse duration is obtained as shown in equation 8.14 below:

$$t_{01} = (A \,\&\, A)$$
$$t_a = (\sim A \,\&\, B)$$
$$t_b = (\sim B \,\&\, C)$$
$$t_{02} = (\sim C \,\&\, D)$$
$$t_c = (\sim D \,\&\, E)$$
$$t_d = (\sim E \,\&\, F)$$
$$t_{03} = (\sim F \,\&\, G) \ldots \qquad (8.14)$$

In equation 8.14, symbols (&) represents logical AND and (~) represents NOT operation respectively. To easily generate the MC gate pulse, the timing pulse in equation 8.14 are given to OR gates to obtain the following additional timing pulse:

$$t_{01a} = (t_a || t_{01})$$

$$t_{01ab} = (t_b||t_{01}||t_a)$$
$$t_{b02c} = (t_c||t_{02}||t_b)$$
$$t_{ab02cd} = (t_a||t_b||t_{02}||t_c||t_d)$$
$$t_{d03} = (t_d||t_{03})$$
$$t_{cd03} = (t_c||t_d||t_{03}) \ldots \quad (8.15)$$

In equation 8.15, symbol (||) represents logical OR operation.

The complete gate timing for the nine bidirectional switches using Direct SSVM algorithm is given in Table 8.8 below:

TABLE 8.8: SSVM Gate Pulse Timing

Sl.No.	SV,SI	SSF_X HIGH	SAa	SBa	SCa	SAb	SBb	SCb	SAc	SBc	SCc
1	1, 1 or 4, 4	ssf1	tab02cd	t03	t01	tb02c	td03	t01a	t02	tcd03	t01ab
2	1, 4 or 4, 1	ssf2	t02	tcd03	t01ab	tb02c	td03	t01a	tab02cd	t03	t01
3	1, 5 or 4, 2	ssf3	t03	t01	tab02cd	td03	t01a	tb02c	tcd03	t01ab	t02
4	1, 2 or 4, 5	ssf4	tcd03	t01ab	t02	td03	t01a	tb02c	t03	t01	tab02cd
5	1, 3 or 4, 6	ssf5	t01	tab02cd	t03	t01a	tb02c	td03	t01ab	t02	tcd03
6	1, 6 or 4, 3	ssf6	t01ab	t02	tcd03	t01a	tb02c	td03	t01	tab02cd	t03
7	2, 4 or 5, 1	ssf7	tb02c	td03	t01a	t02	tcd03	t01ab	tab02cd	t03	t01
8	2, 1 or 5, 4	ssf8	tb02c	td03	t01a	tab02cd	t03	t01	t02	tcd03	t01ab
9	2, 2 or 5, 5	ssf9	td03	t01a	tb02c	tcd03	t01ab	t02	t03	t01	tab02cd
10	2, 5 or 5, 2	ssf10	td03	t01a	tb02c	t03	t01	tab02cd	tcd03	t01ab	t02
11	2, 6 or 5, 3	ssf11	t01a	tb02c	td03	t01ab	t02	tcd03	t01	tab02cd	t03
12	2, 3 or 5, 6	ssf12	t01a	tb02c	td03	t01	tab02cd	t03	t01ab	t02	tcd03
13	3, 1 or 6, 4	ssf13	t02	tcd03	t01ab	tab02cd	t03	t01	tb02c	td03	t01a
14	3, 4 or 6, 1	ssf14	tab02cd	t03	t01	t02	tcd03	t01ab	tb02c	td03	t01a
15	3, 5 or 6, 2	ssf15	tcd03	t01ab	t02	t03	t01	tab02cd	td03	t01a	tb02c
16	3, 2 or 6, 5	ssf16	t03	t01	tab02cd	tcd03	t01ab	t02	td03	t01a	tb02c
17	3, 3 or 6, 6	ssf17	t01ab	t02	tcd03	t01	tab02cd	t03	t01a	tb02c	td03
18	3, 6 or 6, 3	ssf18	t01	tab02cd	t03	t01ab	t02	tcd03	t01a	tb02c	td03

8.5.5 GATE PULSE GENERATOR: The gate pulse generator for the MC is developed using Embedded MATLAB as shown in Fig. 8.12. The sector switch functions ssf1 to ssf18, gate pulse timing calculator outputs defined in equations 8.14 and 8.15 form the input modules and the outputs are the gate pulses for the nine bidirectional switches of the MC. In Table 8.8, the gate timing for the nine bidirectional switches are shown. The gate timing for switch SAa can be combined by logically ANDing the respective value with sector switch function ssf_x and ORing the value for each sector. Thus the gate timing pulse for switch SAa can be expressed as in equation 8.16 below:

$$\text{SAa} = \text{ssf1\&(tab02cd)}||\text{ssf2\&(t02)}||\text{ssf3\&(t03)}|| \ldots \ldots \ldots ||\text{ssf18\&(t01)}.. \quad (8.16)$$

Program segment VI gives the method of generating the gate timing pulses for the nine bidirectional switches using the calculated sector timings given in Table 8.8.

8.6 SIMULATION RESULTS: The simulation of the Three Phase SSVM Matrix Converter was carried out in SIMULINK [51]. The parameters used for simulation are shown in Table 8.6. The

```
PROGRAM SEGMENT  VI---
function [SAa,SBa,SCa,SAb,SBb,SCb,SAc,SBc,SCc]  =
fcn(ssf1,ssf2,ssf3,ssf4,ssf5,ssf6,ssf7,ssf8,ssf9,ssf10,ssf11,ssf12,ssf13,ssf14,ssf15,ssf16,ssf17,ssf18,t01,ta,tb,t02,tc,td,t03,t01a,
t01ab,tb02c,tab02cd,td03,tcd03)
 %%Narayanaswamy. P.R.Iyer
 SAa =
ssf1&(tab02cd)||ssf2&(t02)||ssf3&(t03)||ssf4&(tcd03)||ssf5&(t01)||ssf6&(t01ab)||ssf7&(tb02c)||ssf8&(tb02c)||ssf9&(td03)||
 ssf10&(td03)||ssf11&(t01a)||ssf12&(t01a)||ssf13&(t02)||ssf14&(tab02cd)||ssf15&(tcd03)||ssf16&(t03)||ssf17&(t01ab)||
ssf18& (t01);
 SBa =
ssf1&(t03)||ssf2&(tcd03)||ssf3&(t01)||ssf4&(t01ab)||ssf5&(tab02cd)||ssf6&(t02)||ssf7&(td03)||ssf8&(td03)||ssf9&(t01a)||
ssf10& (t01a)||ssf11&(tb02c)||ssf12&(tb02c)||ssf13&(tcd03)||ssf14&(t03)||ssf15&(t01ab)||ssf16&(t01)||ssf17&(t02)||
ssf18& (tab02cd);
 SCa =
ssf1&(t01)||ssf2&(t01ab)||ssf3&(tab02cd)||ssf4&(t02)||ssf5&(t03)||ssf6&(tcd03)||ssf7&(t01a)||ssf8&(t01a)||ssf9&(tb02c)||
ssf10&(tb02c)||ssf11&(td03)||ssf12&(td03)||ssf13&(t01ab)||ssf14&(t01)||ssf15&(t02)||ssf16&(tab02cd)||ssf17&(tcd03)||
ssf18& (t03);
 SAb =
ssf1&(tb02c)||ssf2&(tb02c)||ssf3&(td03)||ssf4&(td03)||ssf5&(t01a)||ssf6&(t01a)||ssf7&(t02)||ssf8&(tab02cd)||ssf9&(tcd03)||
 ssf10&(t03)||ssf11&(t01ab)||ssf12&(t01)||ssf13&(tab02cd)||ssf14&(t02)||ssf15&(t03)||ssf16&(tcd03)||ssf17&(t01)||
ssf18& (t01ab);
 SBb =
ssf1&(td03)||ssf2&(td03)||ssf3&(t01a)||ssf4&(t01a)||ssf5&(tb02c)||ssf6&(tb02c)||ssf7&(tcd03)||ssf8&(t03)||ssf9&(t01ab)||
ssf10&(t01)||ssf11&(t02)||ssf12&(tab02cd)||ssf13&(t03)||ssf14&(tcd03)||ssf15&(t01)||ssf16&(t01ab)||ssf17&(tab02cd)||
ssf18& (t02);
 SCb = ssf1&(t01a)||ssf2&(t01a)||ssf3&(tb02c)||ssf4&(tb02c)||ssf5&(td03)||ssf6&(td03)||ssf7&(t01ab)||ssf8&(t01)||ssf9&
(t02)||ssf10&(tab02cd)||ssf11&(tcd03)||ssf12&(t03)||ssf13&(t01)||ssf14&(t01ab)||ssf15&(tab02cd)||ssf16&(t02)||ssf17&(t03)||
ssf18&(tcd03);
 SAc =
ssf1&(t02)||ssf2&(tab02cd)||ssf3&(tcd03)||ssf4&(t03)||ssf5&(t01ab)||ssf6&(t01)||ssf7&(tab02cd)||ssf8&(t02)||ssf9&(t03)||
ssf10&(tcd03)||ssf11&(t01)||ssf12&(t01ab)||ssf13&(tb02c)||ssf14&(tb02c)||ssf15&(td03)||ssf16&(td03)||ssf17&(t01a)||
ssf18&(t01a);
 SBc = ssf1&(tcd03)||ssf2&(t03)||ssf3&(t01ab)||ssf4&(t01)||ssf5&(t02)||ssf6&(tab02cd)||ssf7&(t03)||ssf8&(tcd03)||ssf9&
(t01)|| ssf10&(t01ab)||ssf11&(tab02cd)||ssf12&(t02)||ssf13&(td03)||ssf14&(td03)||ssf15&(t01a)||ssf16&(t01a)||ssf17&(tb02c)||
ssf18&(tb02c);
 SCc =
ssf1&(t01ab)||ssf2&(t01)||ssf3&(t02)||ssf4&(tab02cd)||ssf5&(tcd03)||ssf6&(t03)||ssf7&(t01)||ssf8&(t01ab)||ssf9&(tab02cd)||
 ssf10&(t02)||ssf11&(t03)||ssf12&(tcd03)||ssf13&(t01a)||ssf14&(t01a)||ssf15&(tb02c)||ssf16&(tb02c)||ssf17&(td03)||ssf18&
(td03);
```

ode15S(Stiff/NDF) solver was used. Simulation of the above three phase AC to three phase AC direct SSVM of MC was carried out for two different output frequencies with all other parameters constant. The simulation results of the harmonic spectrum of line to neutral output voltage, input current, load current and line to line output voltage for a 50 Hz AC output voltage are shown in Fig. 8.14(A) to (D) and the oscilloscope waveform of the above in order are shown in Fig. 8.15(A) to (D). Similarly the harmonic spectrum of the above in order for a 20 Hz AC output voltage are shown in Fig. 8.16(A) to (D) and the oscilloscope waveform of the above in order are shown in Fig. 8.17(A) to (D). The simulation results are tabulated in Table 8.9.

TABLE 8.9: SSVM Simulation Results 2

Sl.No.	Three Phase SSVM MC Input – Output Frequency Hz	THD of Line to Line Output Voltage p.u.	THD Of Line to Neutral Output Voltage p.u.	THD of Input Current p.u.	THD of Load Current p.u.
1)	50 – 50	0.9913	1.85	2.5136	0.4541
2)	50 - 20	0.8925	1.3041	1.5777	0.3867

8.7 MODEL OF CENTRE ZERO ASYMMETRICAL SPACE VECTOR MODULATED THREE PHASE MATRIX CONVERTER: This method is newly proposed here. This is a modification of the direct ASVM technique discussed in section 8.2 above. The Table 8.1, 8.2 and 8.3 and the rules 1 and 2 discussed in section 8.2 above are used here to develop the model of the new Centre Zero ASVM (CZASVM) three phase MC. The equations 8.5 to 8.10 are used to calculate the duty-ratios d0, dI, dII, dIII, dIV and d0. With regard to zero configuration for CZASVM, Table 8.3

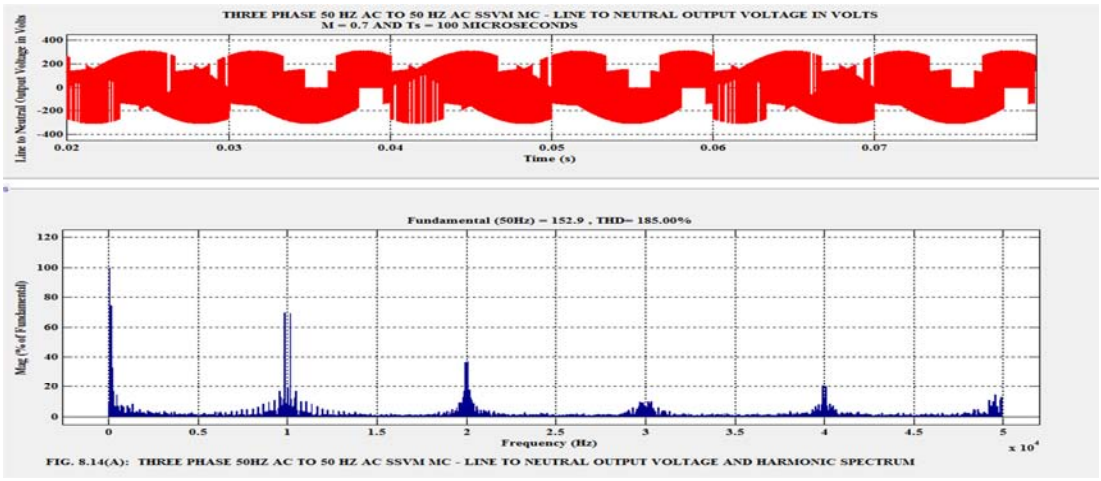


FIG. 8.14(A): THREE PHASE 50HZ AC TO 50 HZ AC SSVM MC - LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM

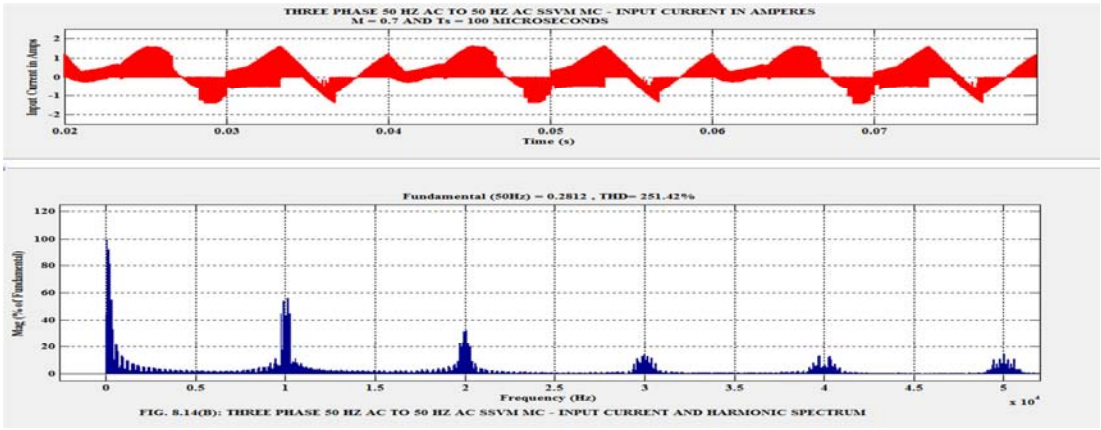


FIG. 8.14(B): THREE PHASE 50 HZ AC TO 50 HZ AC SSVM MC - INPUT CURRENT AND HARMONIC SPECTRUM

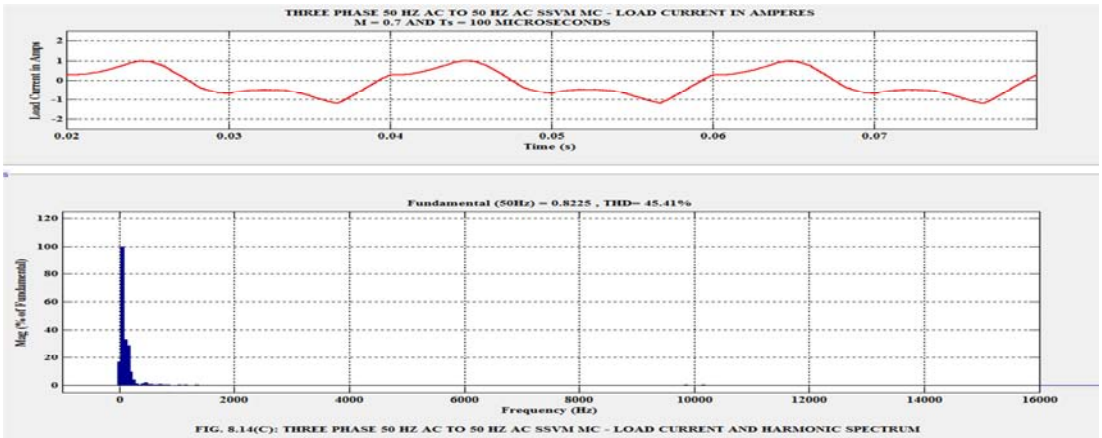


FIG. 8.14(C): THREE PHASE 50 HZ AC TO 50 HZ AC SSVM MC - LOAD CURRENT AND HARMONIC SPECTRUM

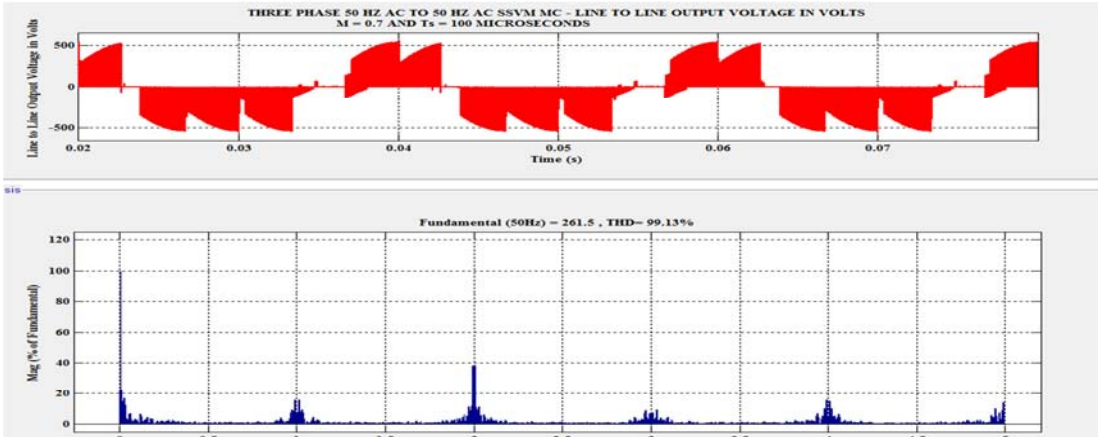
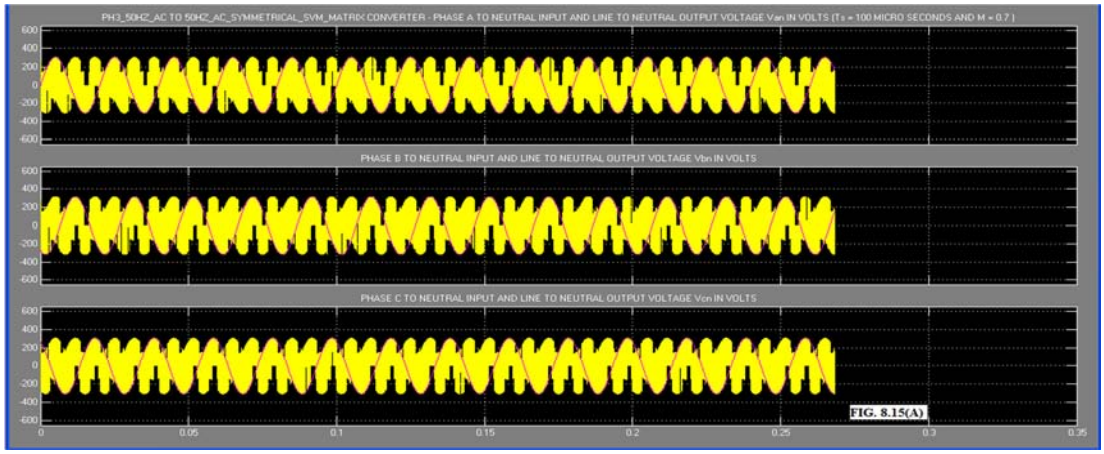
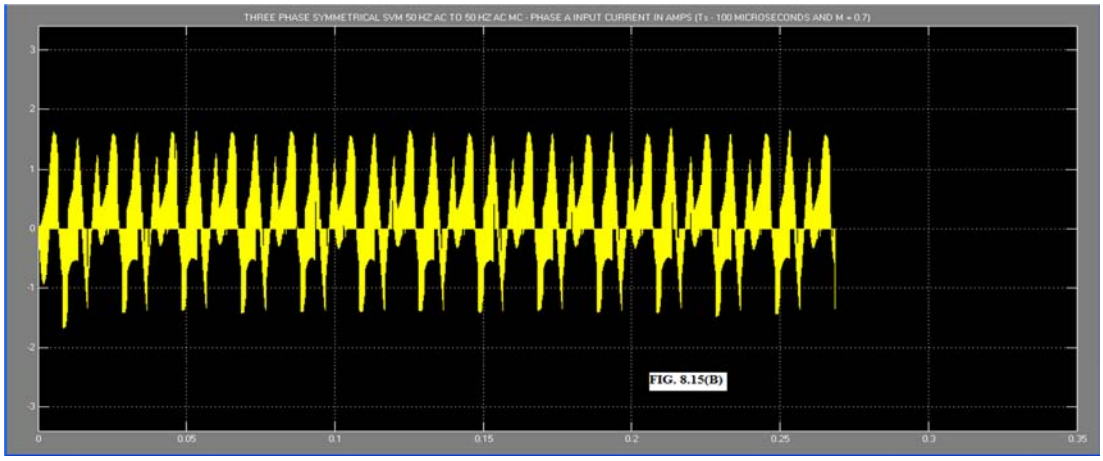
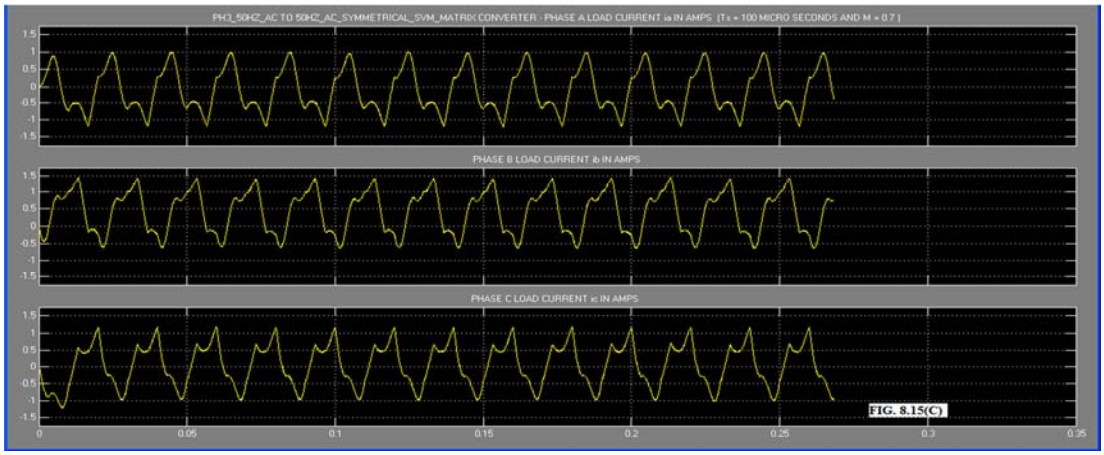
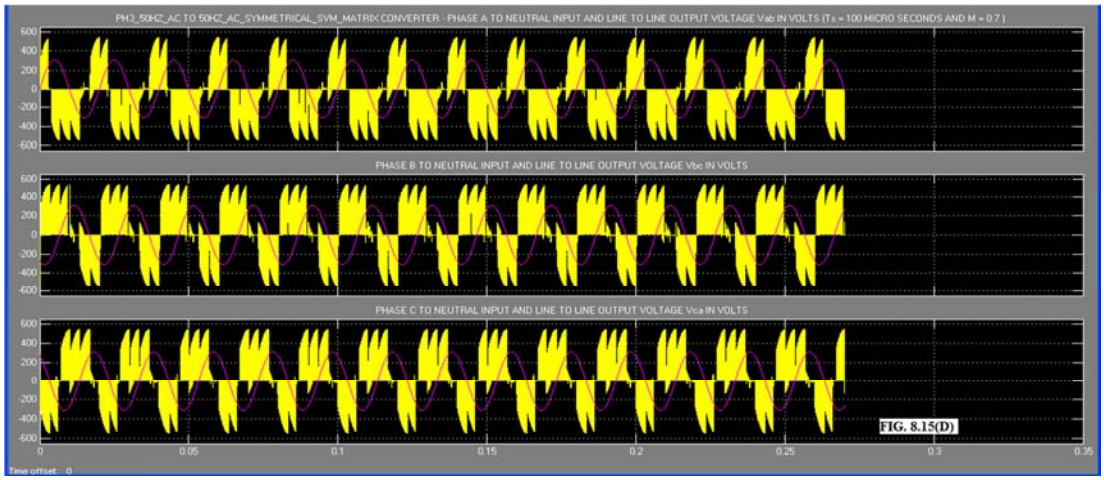


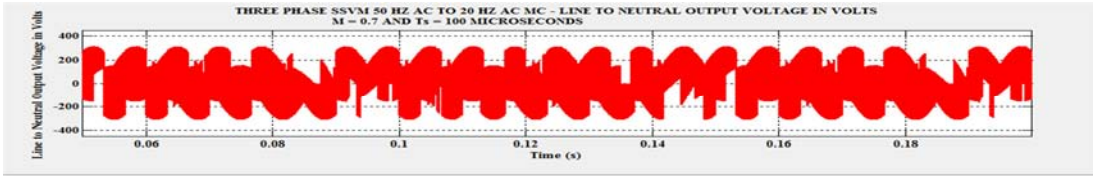
FIG. 8.14(D): THREE PHASE 50 HZ AC TO 50 HZ AC SSVM MC - LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM


PH3_50HZ_AC TO 50HZ_AC_SYMMETRICAL_SVM_MATRIX CONVERTER - PHASE A TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Van IN VOLTS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vbn IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vcn IN VOLTS
FIG. 8.15(A)


THREE PHASE SYMMETRICAL SVM 50 HZ AC TO 50 HZ AC MC - PHASE A INPUT CURRENT IN AMPS (Ts - 100 MICROSECONDS AND M = 0.7)
FIG. 8.15(B)


PH3_50HZ_AC TO 50HZ_AC_SYMMETRICAL_SVM_MATRIX CONVERTER - PHASE A LOAD CURRENT ia IN AMPS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B LOAD CURRENT ib IN AMPS
PHASE C LOAD CURRENT ic IN AMPS
FIG. 8.15(C)


PH3_50HZ_AC TO 50HZ_AC_SYMMETRICAL_SVM_MATRIX CONVERTER - PHASE A TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vab IN VOLTS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vbc IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vca IN VOLTS
FIG. 8.15(D)



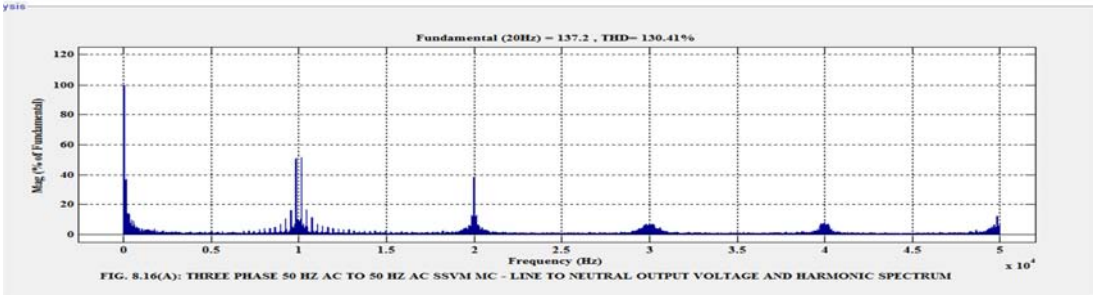
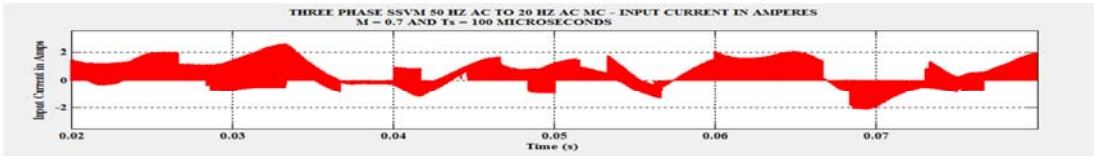


FIG. 8.16(A): THREE PHASE 50 HZ AC TO 50 HZ AC SSVM MC - LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM



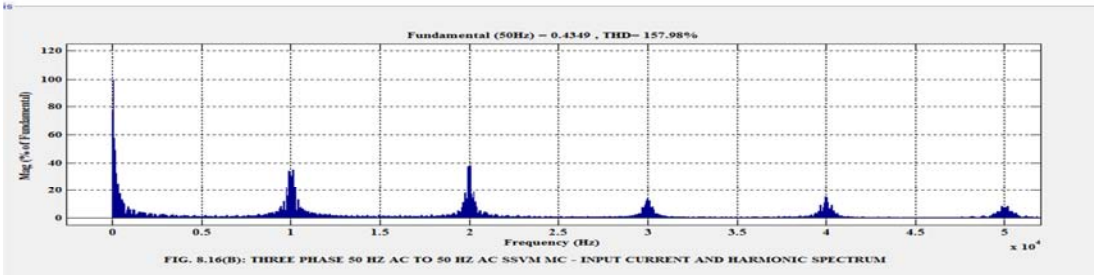
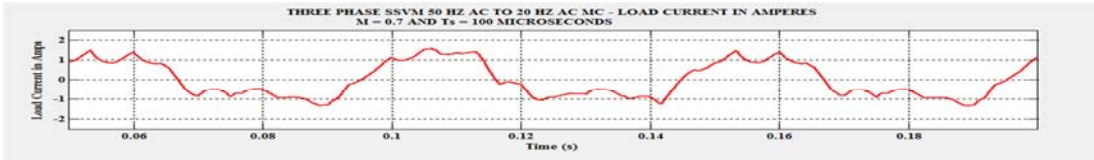


FIG. 8.16(B): THREE PHASE 50 HZ AC TO 50 HZ AC SSVM MC - INPUT CURRENT AND HARMONIC SPECTRUM



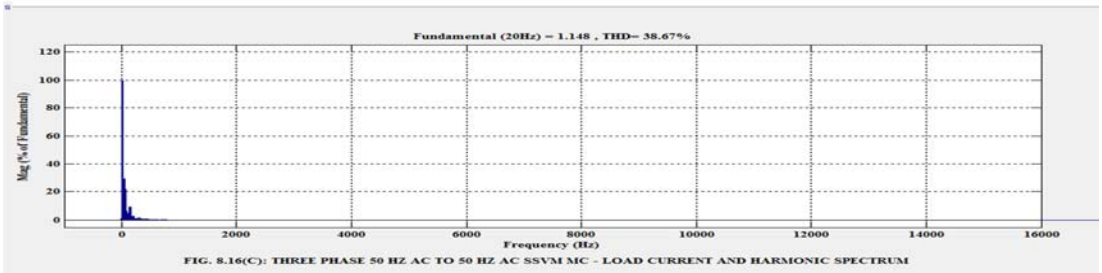
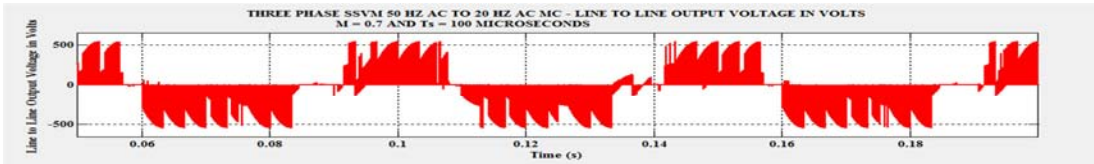


FIG. 8.16(C): THREE PHASE 50 HZ AC TO 50 HZ AC SSVM MC - LOAD CURRENT AND HARMONIC SPECTRUM



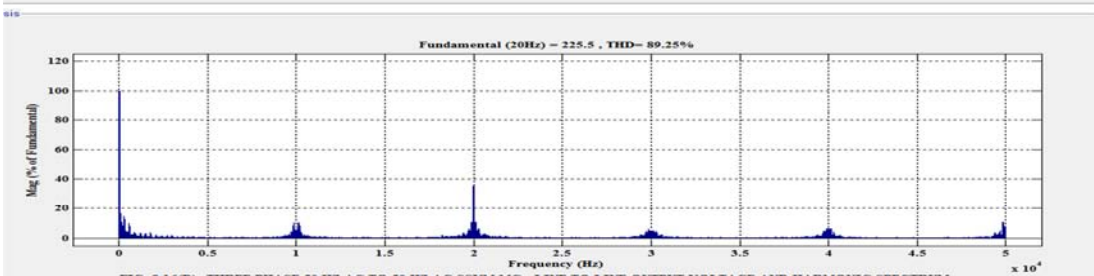
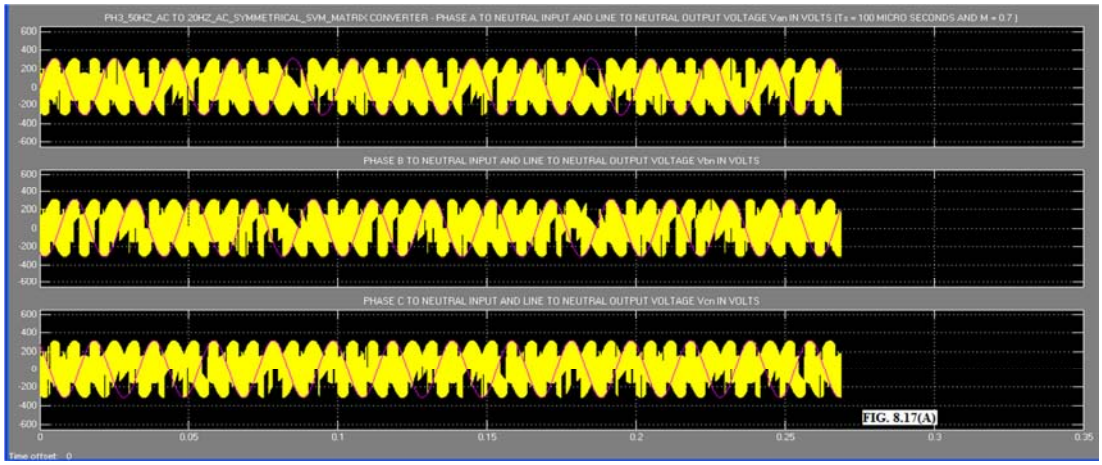
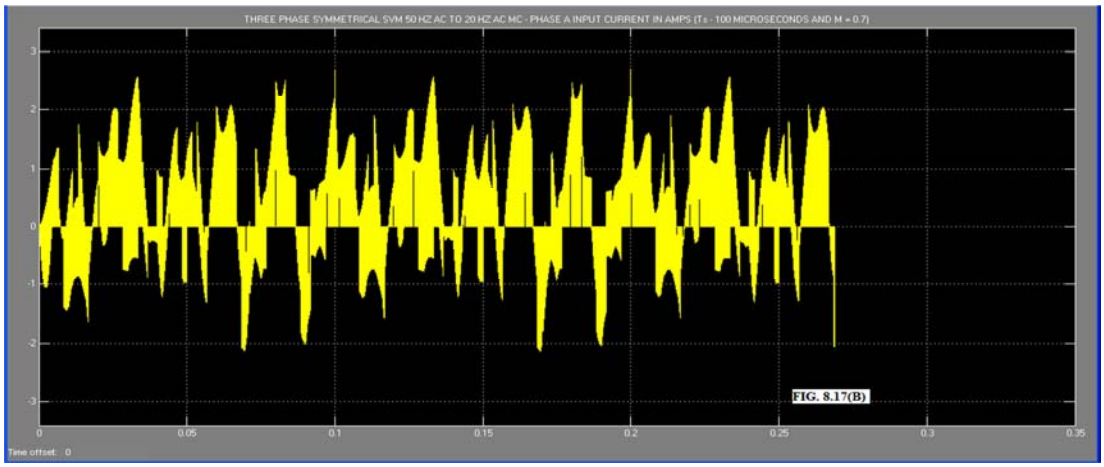
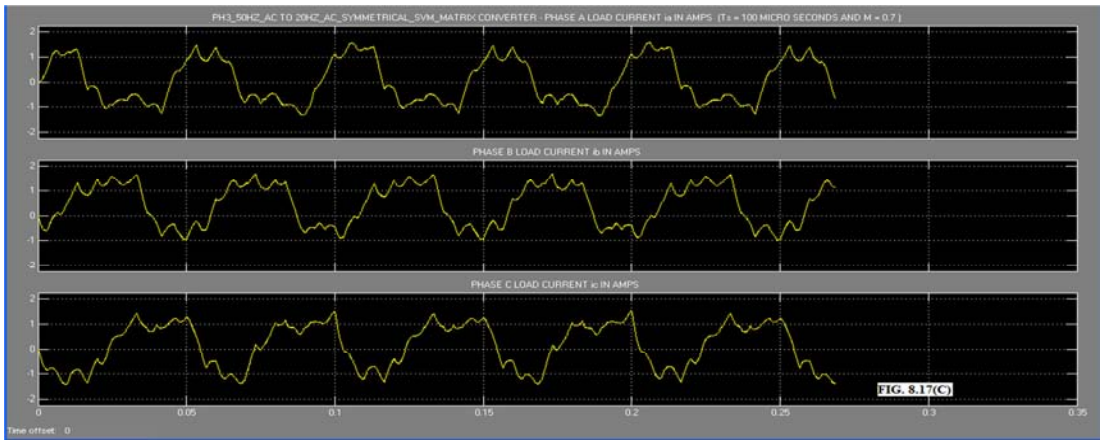


FIG. 8.16(D): THREE PHASE 50 HZ AC TO 50 HZ AC SSVM MC - LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM


PH3_50HZ_AC TO 20HZ_AC_SYMMETRICAL_SVM_MATRIX CONVERTER - PHASE A TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Van IN VOLTS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vbn IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vcn IN VOLTS
FIG. 8.17(A)


THREE PHASE SYMMETRICAL SVM 50 HZ AC TO 20 HZ AC MC - PHASE A INPUT CURRENT IN AMPS (Ts - 100 MICROSECONDS AND M = 0.7)
FIG. 8.17(B)


PH3_50HZ_AC TO 20HZ_AC_SYMMETRICAL_SVM_MATRIX CONVERTER - PHASE A LOAD CURRENT ia IN AMPS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B LOAD CURRENT ib IN AMPS
PHASE C LOAD CURRENT ic IN AMPS
FIG. 8.17(C)


PH3_50HZ_AC TO 20HZ_AC_SYMMETRICAL_SVM_MATRIX CONVERTER - PHASE A TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vab IN VOLTS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vbc IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vca IN VOLTS
FIG. 8.17(D)

shown above can be used. For example, considering output voltage vector in sector 1 and input current vector in sector 4 (i.e., SV = 1; SI = 4) within their respective hexagons, it can be seen that (SV + SI) is odd, rule 2 applies with δ^I *and* δ^{IV} having negative sign. Also using Table 8.3, the following is the only possible sequence that can be generated for CZASVM technique:

-9, +3, -1, +7 which from table 8.1 is given below:

CCA – CAA – BAA – BBA - AAA ׀ AAA - BBA – BAA – CAA – CCA

׀←----------Ts/2---------- →׀←----------Ts/2----------→׀

where Ts is the sampling period.

The gate pulse pattern for CZASVM using Tables 8.1 to 8.3, rules 1 and 2 is shown in Table 8.10.

		TABLE 8.10		CZASVM Switching Pattern				
Sl.No.	SV, SI	(SV+SI)	SSF_X HIGH	BIDIRECTIONAL SWITCH GATE PULSE PATTERN				
				ta	tb	tc	td	t0
1	1, 1 or 4, 4	Even	ssf1	ACC	AAC	AAB	ABB	AAA
2	1, 4 or 4, 1	Odd	ssf2	CCA	CAA	BAA	BBA	AAA
3	1, 5 or 4, 2	Even	ssf3	CBB	CCB	CCA	CAA	CCC
4	1, 2 or 4, 5	Odd	ssf4	BBC	BCC	ACC	AAC	CCC
5	1, 3 or 4, 6	Even	ssf5	BAA	BBA	BBC	BCC	BBB
6	1, 6 or 4, 3	Odd	ssf6	AAB	ABB	CBB	CCB	BBB
7	2, 4 or 5, 1	Even	ssf7	CCA	ACA	ABA	BBA	AAA
8	2, 1 or 5, 4	Odd	ssf8	CAC	AAC	AAB	BAB	AAA
9	2, 2 or 5, 5	Even	ssf9	BBC	CBC	CAC	AAC	CCC
10	2, 5 or 5, 2	Odd	ssf10	BCB	CCB	CCA	ACA	CCC
11	2, 6 or 5, 3	Even	ssf11	AAB	BAB	BCB	CCB	BBB
12	2, 3 or 5, 6	Odd	ssf12	ABA	BBA	BBC	CBC	BBB
13	3, 1 or 6, 4	Even	ssf13	CAC	CAA	BAA	BAB	AAA
14	3, 4 or 6, 1	Odd	ssf14	ACC	ACA	ABA	ABB	AAA
15	3, 5 or 6, 2	Even	ssf15	BCB	BCC	ACC	ACA	CCC
16	3, 2 or 6, 5	Odd	ssf16	CBB	CBC	CAC	CAA	CCC
17	3, 3 or 6, 6	Even	ssf17	ABA	ABB	CBB	CBC	BBB
18	3, 6 or 6, 3	Odd	ssf18	BAA	BAB	BCB	BCC	BBB

The SIMULINK model of the direct Centre Zero Asymmetrical Space Vector Modulated (CZASVM) three phase AC to three phase AC MC is shown in Fig. 8.18. The power circuit of the model is developed using the SimPowerSystems blockset in SIMULINK [51]. This mainly consists of three phase AC voltage source, bidirectional switch matrix, output filter and R-L load. The arrangement of the bidirectional switch matrix using IGBTs is the same as shown in Fig. 3.2 of Chapter III.

The modulation algorithm is developed in several sub units using Embedded MATLAB Function, MATLAB Function, Math Function, Logical and Bit Operator and using Sources block set in SIMULINK [51]. The various sub units are explained below:

8.7.1 DUTY-CYCLE SEQUENCE AND SECTOR SWITCH FUNCTION GENERATOR: This is developed using Embedded MATLAB Function block in SIMULINK, as shown in Fig. 8.18. With peak line to neutral input voltage, desired peak output phase voltage, input frequency, output frequency, time, angular frequency of reference frame ωc as input parameters, the three phase output voltage can be resolved into dq-axis component voltages [42] and the absolute value of the angle of the output phase voltage, vout_angle can be calculated using the function atan2(voq,vod). Using input voltage and input phase displacement angle, a similar procedure is used to calculate the absolute value of the input current angle, i_in_angle. The value of reference frame frequency ωc is zero. This

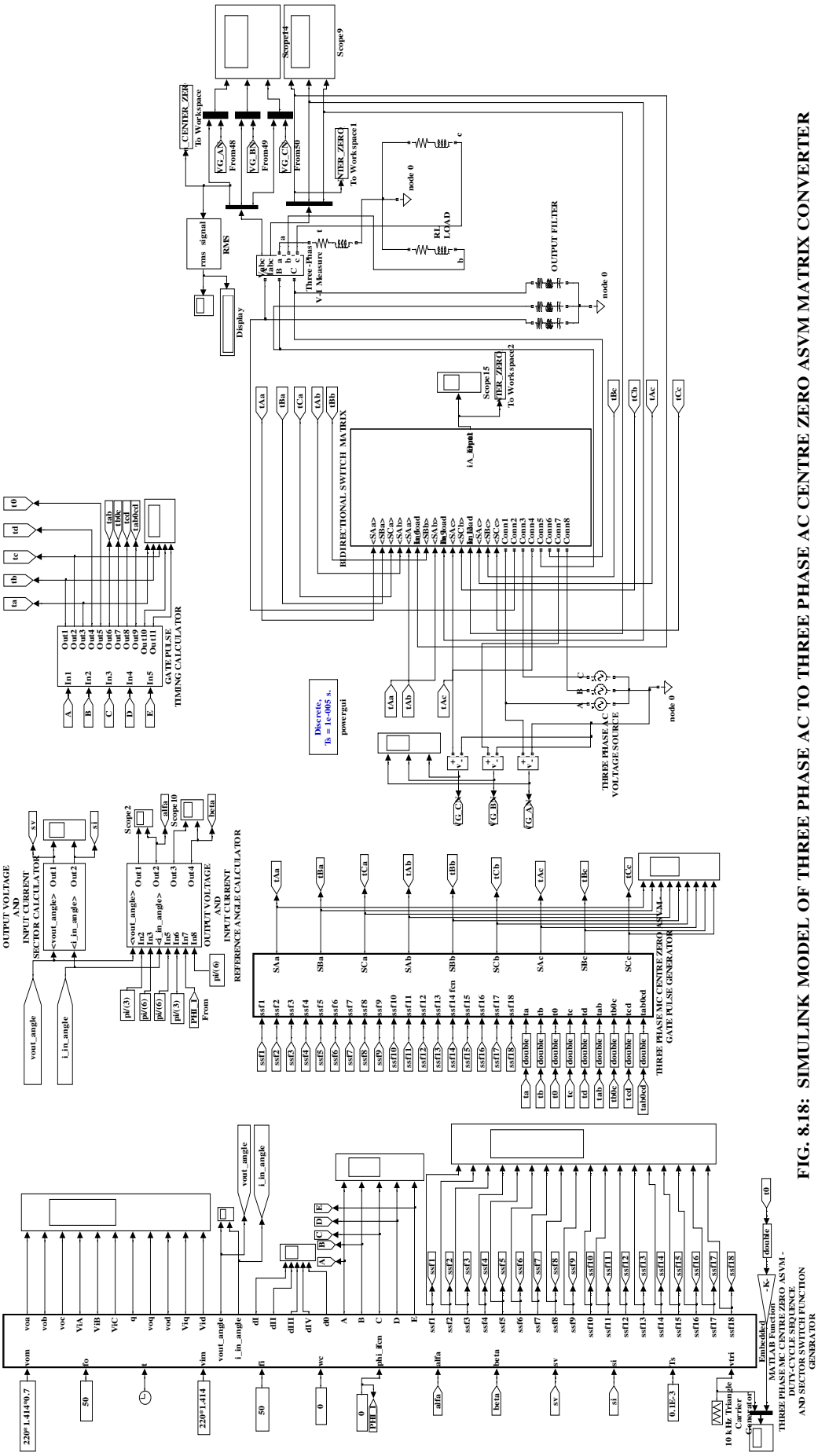


FIG. 8.18: SIMULINK MODEL OF THREE PHASE AC TO THREE PHASE AC CENTRE ZERO ASVM MATRIX CONVERTER

is illustrated in Program segment I above. These two values of vout_angle and i_in_angle are used to calculate the output voltage sector sv, input current sector si, α and β values for output voltage and input current using MATLAB function, REM functions and SUBTRACT modules.

Program segment VII illustrates the MATLAB code for duty cycle sequencing and sector switch function generation. Duty-cycle dI, dII, dIII, dIV and d0 are calculated using equations 8.5 to 8.8 and 8.10 assuming unity input power factor. With (sv+si) even and odd, rule 1 and 2 for duty cycle are followed with zero vector duty cycle d0 introduced at the end of the four duty cycles, dI, dII, dIII, dIV. This is used to calculate the timing A, B, C, D and E, by comparison of the cumulative sector timing with a triangle carrier Vtri as shown in Program Segment VII. This triangle carrier Vtri has a period Ts, peak value Ts/2 Volts and minimum value zero, as shown in Fig. 8.4. Cumulative sector timing is obtained by appropriately adding the value of duty-ratio and multiplying by Ts/2, as per rules 1 and 2 given above. Sector switch functions ssf1 to ssf18 are determined using if-then-else statement. For example sector switch function ssf1 is HIGH only when sv = si =1 or sv = si = 4 and is LOW otherwise.

8.7.2 OUTPUT VOLTAGE AND INPUT CURRENT SECTOR CALCULATOR: This is developed using MATLAB Function, a mux and a demux as shown in Fig. 8.5 above. The input to the mux are vout_angle and i_in_angle. The output from the demux are SV and SI. The source code to determine SV and SI is shown in Program Segment III above.

8.7.3 OUTPUT VOLTAGE AND INPUT CURRENT REFERENCE ANGLE CALCULATOR: This is shown in Fig. 8.6 above. This uses two REM function blocks and SUBTRACT modules. The first REM block has the inputs v_out_angle and pi/(3). The second REM block has the inputs i_in_angle and pi/(3). The output of the first REM block is subtracted from pi/(6) to obtain angle alfa defined in Fig. 8.2(A). The output of the second REM block is subtracted from pi/(6), input p.f. angle phi_i and once again from pi/(6) to obtain beta as per the configuration defined in Fig. 8.2(B).

8.7.4 GATE PULSE TIMING CALCULATOR: This is shown in Fig. 8.19. The inputs in1 to in5 are A, B, C, D and E respectively. The individual gate pulse timing, ta, tb, tc, td and t0 are respectively dIII*Ts/(2), dI*Ts/(2), dII*Ts/(2), dIV*Ts/(2) and d0*Ts/(2), when (SV+SI) is even and dI*Ts/(2), dIII*Ts/(2), dIV*Ts/(2), dII*Ts/(2) and d0*Ts/(2), when (SV+SI) is odd. This individual gate pulse duration is obtained as shown in equation 8.17 below:

$$t_a = (A \,\&\, A)$$
$$t_b = (\sim A \,\&\, B)$$
$$t_c = (\sim B \,\&\, C)$$
$$t_d = (\sim C \,\&\, D)$$
$$t_0 = (\sim D \,\&\, E) \ldots \qquad (8.17)$$

```
PROGRAM SEGMENT  VII
%%Narayanaswamy. P.R. Iyer
function(q,dI,dII,dIII,dIV,d0,A,B,C,D,E,ssf1,ssf2,ssf3,…ssf18) =
fcn(Vom,fo,t,Vim,fi,wc,ph_i,alfa,beta,sv,si,Ts,vtri)
%%Duty cycle calculations
dI = (2*q*cos(alfa - pi/(3))*cos(beta - pi/(3))/(sqrt(3)*cos(phi_i)));
dII = (2*q*cos(alfa - pi/(3))*cos(beta + pi/(3))/(sqrt(3)*cos(phi_i)));
dIII = (2*q*cos(alfa + pi/(3))*cos(beta - pi/(3))/(sqrt(3)*cos(phi_i)));
dIV = (2*q*cos(alfa + pi/(3))*cos(beta + pi/(3))/(sqrt(3)*cos(phi_i)));
d0 = (1 - dI - dII - dIII - dIV);
if (rem((sv+si),2) == 0)
%%even sequence
if ( vtri <= dIII*Ts/(2))
A = 1; else
A = 0;
end
if ( vtri <= (dIII + dI)*Ts/(2))
B = 1; else
B = 0;
end
if ( vtri <= (dIII + dI + dII)*Ts/(2))
C = 1; else
C = 0;
end
if ( vtri <= (dIII + dI + dIV + dII)*Ts/(2))
D = 1; else
D = 0;
end
if ( vtri <= (dIII + dI + d0 + dII + dIV)*Ts/(2))
E = 1; else
E = 0;
end
else
%%odd sequence
if ( vtri <= dI*Ts/(2))
A = 1; else
A = 0;
end
if ( vtri <= (dIII + dI)*Ts/(2))
B = 1; else
B = 0;
end
if ( vtri <= (dIII + dI + dIV)*Ts/(2))
C = 1; else
C = 0;
end
if ( vtri <= (dIII + dI + dII + dIV)*Ts/(2))
D = 1; else
D = 0;
end
if ( vtri <= (dIII + dI + d0 + dII + dIV)*Ts/(2))
E = 1; else
E = 0;
end
end
if (sv == 1 && si == 1 || sv == 4 && si == 4)
%%sector 1. sector switch function ssf1.
ssf1 = 1; else
ssf1 = 0;
end
if ( sv == 4 && si == 1  ||  sv == 1 && si == 4 )
%%sector 2. sector switch function ssf2.
ssf2 = 1; else
ssf2 = 0;
end
.
.
.
if ( sv == 3 && si == 6  ||  sv == 6 && si == 3 )
%%sector 18. sector switch function ssf18.
ssf18 = 1; else
ssf18 = 0;
end
```

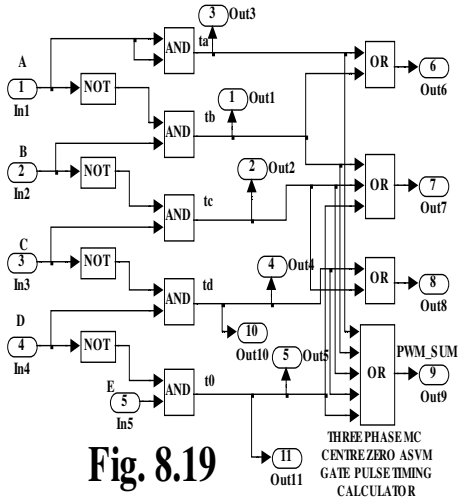


Fig. 8.19

In equation 8.17, symbols (&) represents logical AND and (~) represents NOT operation respectively. To easily generate the MC gate pulse, the timing pulse in equation 8.17 are given to OR gates to obtain the following additional timing pulse:

$$t_{ab} = (t_a||t_b)$$

$$t_{b0c} = (t_b||t_0||t_c)$$

$$t_{cd} = (t_c||t_d)$$

$$t_{ab0cd} = (t_a||t_b||t_0||t_c||t_d) \ldots\ldots (8.18)$$

In equation 8.18, symbol (||) represents logical OR operation.

The complete gate timing for the nine bidirectional switches using CZASVM algorithm is given in Table 8.11 below:

TABLE 8.11: CZASVM Gate Pulse Timing

Sl.No.	SV,SI	SSF_X HIGH	SAa	SBa	SCa	Sab	SBb	SCb	SAc	SBc	SCc
1	1, 1 or 4, 4	ssf1	tab0cd	0	0	tb0c	td	ta	t0	tcd	tab
2	1, 4 or 4, 1	ssf2	t0	tcd	tab	tb0c	td	ta	tab0cd	0	0
3	1, 5 or 4, 2	ssf3	0	0	tabocd	td	ta	tb0c	tcd	tab	t0
4	1, 2 or 4, 5	ssf4	tcd	tab	t0	td	ta	tb0c	0	0	tab0cd
5	1, 3 or 4, 6	ssf5	0	tab0cd	0	ta	tb0c	td	tab	t0	tcd
6	1, 6 or 4, 3	ssf6	tab	t0	tcd	ta	tb0c	td	0	tab0cd	0
7	2, 4 or 5, 1	ssf7	tb0c	td	ta	t0	tcd	tab	tab0cd	0	0
8	2, 1 or 5, 4	ssf8	tb0c	td	ta	tab0cd	0	0	t0	tcd	tab
9	2, 2 or 5, 5	ssf9	td	ta	tb0c	tcd	tab	t0	0	0	tab0cd
10	2, 5 or 5, 2	ssf10	td	ta	tb0c	0	0	tab0cd	tcd	tab	t0
11	2, 6 or 5, 3	ssf11	ta	tb0c	td	tab	t0	tcd	0	tab0cd	0
12	2, 3 or 5, 6	ssf12	ta	tb0c	td	0	tab0cd	0	tab	t0	tcd
13	3, 1 or 6, 4	ssf13	t0	tcd	tab	tab0cd	0	0	tb0c	td	ta
14	3, 4 or 6, 1	ssf14	tab0cd	0	0	t0	tcd	tab	tb0c	td	ta
15	3, 5 or 6, 2	ssf15	tcd	tab	t0	0	0	tab0cd	td	ta	tb0c
16	3, 2 or 6, 5	ssf16	0	0	tab0cd	tcd	tab	t0	td	ta	tb0c
17	3, 3 or 6, 6	ssf17	tab	t0	tcd	0	tab0cd	0	ta	tb0c	td
18	3, 6 or 6, 3	ssf18	0	tab0cd	0	tab	t0	tcd	ta	tb0c	td

8.7.5 GATE PULSE GENERATOR: The gate pulse generator for the MC is developed using Embedded MATLAB as shown in Fig. 8.18. The sector switch functions ssf1 to ssf18, gate pulse timing calculator outputs defined in equations 8.17 and 8.18 form the input modules and the outputs are the gate pulses for the nine bidirectional switches of the MC. In Table 8.11, the gate timing for the nine bidirectional switches are shown. The gate timing for switch SAa can be combined by logically ANDing the respective value with sector switch function ssf_x and ORing the value for each sector. Thus the gate timing pulse for switch SAa can be expressed as in equation 8.19 below:

$$SAa = ssf1\&(tab0cd)||ssf2\&(t0)||ssf3\&(0)|| \ldots\ldots\ldots ||ssf18\&(0)..(8.19)$$

Program segment VIII gives the method of generating the gate timing pulses for the nine bidirectional switches using the calculated sector timings given in Table 8.11.

```
PROGRAM SEGMENT  VIII
function [SAa,SBa,SCa,SAb,SBb,SCb,SAc,SBc,SCc]  =
fcn(ssf1,ssf2,ssf3,ssf4,ssf5,ssf6,ssf7,ssf8,ssf9,ssf10,ssf11,ssf12,ssf13,ssf14,ssf15,ssf16,ssf17,ssf18,ta,tb,t0,tc,td,tab,tb0c,tcd,
tab0cd)
%%Narayanaswamy. P.R.Iyer.
SAa =
ssf1&(tab0cd)||ssf2&(t0)||ssf3&(0)||ssf4&(tcd)||ssf5&(0)||ssf6&(tab)||ssf7&(tb0c)||ssf8&(tb0c)||ssf9&(td)||ssf10&(td)||ssf11
&(ta)||ssf12&(ta)||ssf13&(t0)||ssf14&(tab0cd)||ssf15&(tcd)||ssf16&(0)||ssf17&(tab)||ssf18&(0);
SBa =
ssf1&(0)||ssf2&(tcd)||ssf3&(0)||ssf4&(tab)||ssf5&(tab0cd)||ssf6&(t0)||ssf7&(td)||ssf8&(td)||ssf9&(ta)||ssf10&(ta)||ssf11&
(tb0c)|| ssf12&(tb0c)||ssf13&(tcd)||ssf14&(0)||ssf15&(tab)||ssf16&(0)||ssf17&(t0)||ssf18&(tab0cd);
SCa =
ssf1&(0)||ssf2&(tab)||ssf3&(tab0cd)||ssf4&(t0)||ssf5&(0)||ssf6&(tcd)||ssf7&(ta)||ssf8&(ta)||ssf9&(tb0c)||ssf10&(tb0c)||ssf11
&(td) ||ssf12&(td)||ssf13&(tab)||ssf14&(0)||ssf15&(t0)||ssf16&(tab0cd)||ssf17&(tcd)||ssf18&(0);
SAb =
ssf1&(tb0c)||ssf2&(tb0c)||ssf3&(td)||ssf4&(td)||ssf5&(ta)||ssf6&(ta)||ssf7&(t0)||ssf8&(tab0cd)||ssf9&(tcd)||ssf10&(0)||ssf11
& (tab)||ssf12&(0)||ssf13&(tab0cd)||ssf14&(t0)||ssf15&(0)||ssf16&(tcd)||ssf17&(0)||ssf18&(tab);
SBb =
ssf1&(td)||ssf2&(td)||ssf3&(ta)||ssf4&(ta)||ssf5&(tb0c)||ssf6&(tb0c)||ssf7&(tcd)||ssf8&(0)||ssf9&(tab)||ssf10&(0)||ssf11
&(t0)||ssf12&(tab0cd)||ssf13&(0)||ssf14&(tcd)||ssf15&(0)||ssf16&(tab)||ssf17&(tab0cd)||ssf18&(t0);
SCb =
ssf1&(ta)||ssf2&(ta)||ssf3&(tb0c)||ssf4&(tb0c)||ssf5&(td)||ssf6&(td)||ssf7&(tab)||ssf8&(0)||ssf9&(t0)||ssf10&(tab0cd)||ssf11
&(tcd)||ssf12&(0)||ssf13&(0)||ssf14&(tab)||ssf15&(tab0cd)||ssf16&(t0)||ssf17&(0)||ssf18&(tcd);
SAc =
ssf1&(t0)||ssf2&(tab0cd)||ssf3&(tcd)||ssf4&(0)||ssf5&(tab)||ssf6&(0)||ssf7&(tab0cd)||ssf8&(t0)||ssf9&(0)||ssf10&(tcd)||ssf11
&(0) ||ssf12&(tab)||ssf13&(tb0c)||ssf14&(tb0c)||ssf15&(td)||ssf16&(td)||ssf17&(ta)||ssf18&(ta);
SBc =
ssf1&(tcd)||ssf2&(0)||ssf3&(tab)||ssf4&(0)||ssf5&(t0)||ssf6&(tab0cd)||ssf7&(0)||ssf8&(tcd)||ssf9&(0)||ssf10&(tab)||ssf11
&(tab0cd)||ssf12&(t0)||ssf13&(td)||ssf14&(td)||ssf15&(ta)||ssf16&(ta)||ssf17&(tb0c)||ssf18&(tb0c);
SCc =
ssf1&(tab)||ssf2&(0)||ssf3&(t0)||ssf4&(tab0cd)||ssf5&(tcd)||ssf6&(0)||ssf7&(0)||ssf8&(tab)||ssf9&(tab0cd)||ssf10&(t0)||ssf11
&(0) ||ssf12&(tcd)||ssf13&(ta)||ssf14&(ta)||ssf15&(tb0c)||ssf16&(tb0c)||ssf17&(td)||ssf18&(td);
```

8.8 SIMULATION RESULTS: The simulation of the Three Phase CZASVM Matrix Converter was carried out in SIMULINK [51]. The parameters used for simulation are shown in Table 8.6. The ode15S(Stiff/NDF) solver was used. Simulation of the above three phase AC to three phase AC direct CZASVM of MC was carried out for two different output frequencies with all other parameters constant. The simulation results of the harmonic spectrum of line to neutral output voltage, input current, load current and line to line output voltage for a 50 Hz AC output voltage are shown in Fig. 8.20(A) to (D) and the oscilloscope waveform of the above in order are shown in Fig. 8.21(A) to (D). Similarly the harmonic spectrum of the above in order for a 20 Hz AC output voltage are shown in Fig. 8.22(A) to (D) and the oscilloscope waveform of the above in order are shown in Fig. 8.23(A) to (D). The simulation results are tabulated in Table 8.12.

TABLE 8.12: CZASVM Simulation Results 3

Sl.No.	Three Phase CZASVM MC Input – Output Frequency Hz	THD of Line to Line Output Voltage p.u.	THD Of Line to Neutral Output Voltage p.u.	THD of Input Current p.u.	THD of Load Current p.u.
1)	50 – 50	1.5989	2.8457	3.9484	0.8002
2)	50 – 20	1.2932	2.2127	3.8462	0.3569

8.9 DISCUSSION OF RESULTS: The Centre Zero ASVM (CZASVM) is a newly proposed Space Vector Modulation technique. The THD of line to neutral and line to line output voltage, input current and load current decreases as the output frequency is reduced. However for ASVM technique the THD of load current increases as the output frequency is reduced. Although CZASVM technique is presented here, from the point of harmonic performance of the MC, it is found to be inferior to

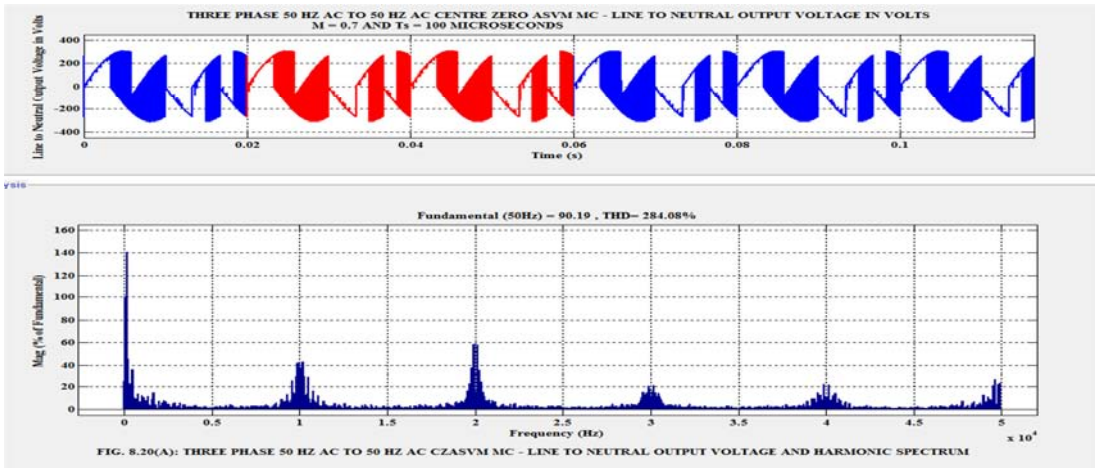


FIG. 8.20(A): THREE PHASE 50 HZ AC TO 50 HZ AC CZASVM MC - LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM

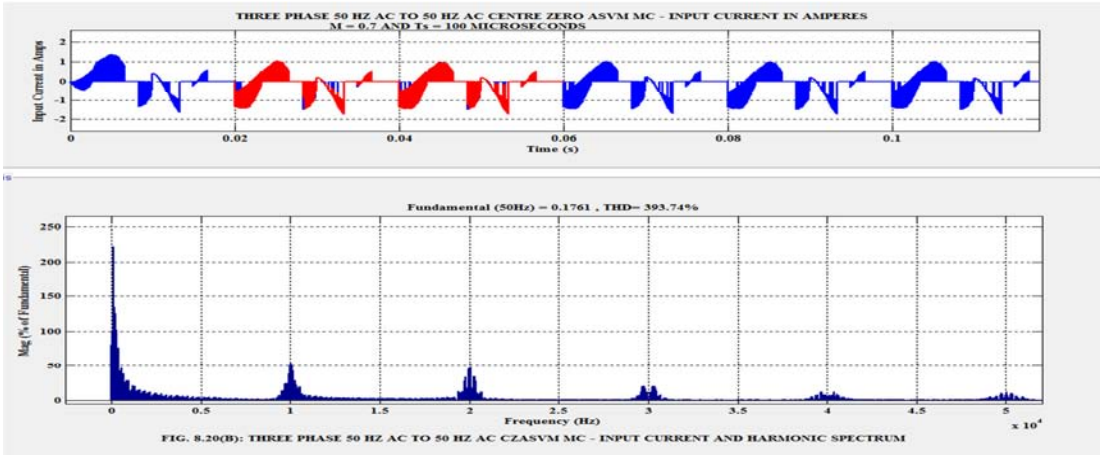


FIG. 8.20(B): THREE PHASE 50 HZ AC TO 50 HZ AC CZASVM MC - INPUT CURRENT AND HARMONIC SPECTRUM

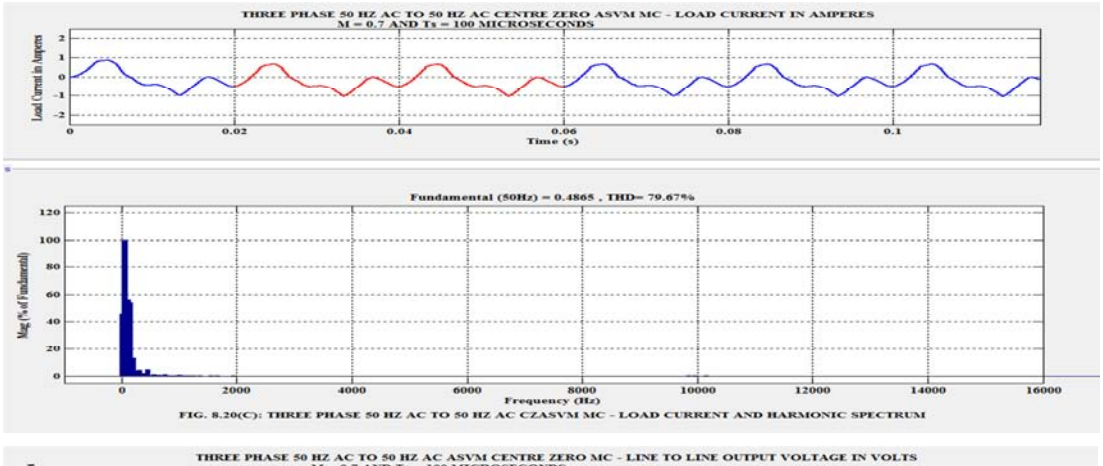


FIG. 8.20(C): THREE PHASE 50 HZ AC TO 50 HZ AC CZASVM MC - LOAD CURRENT AND HARMONIC SPECTRUM

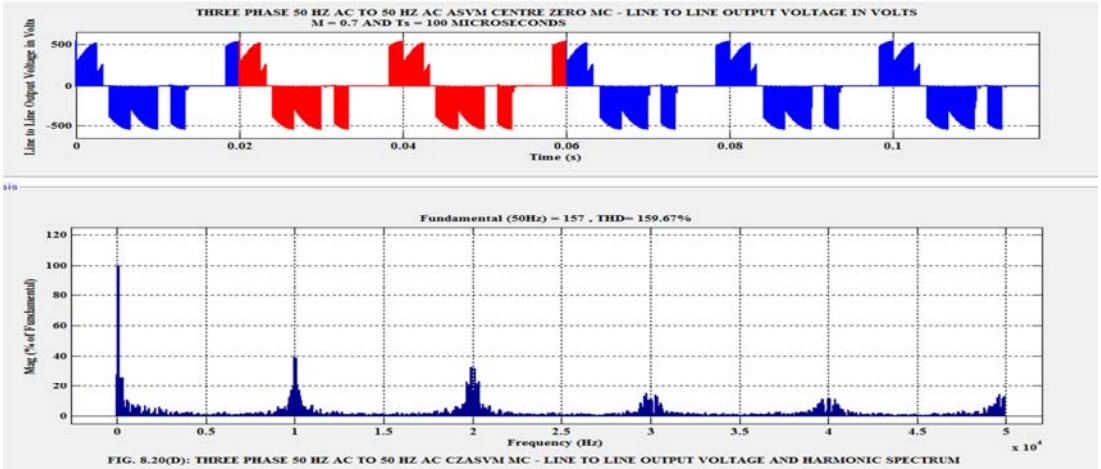
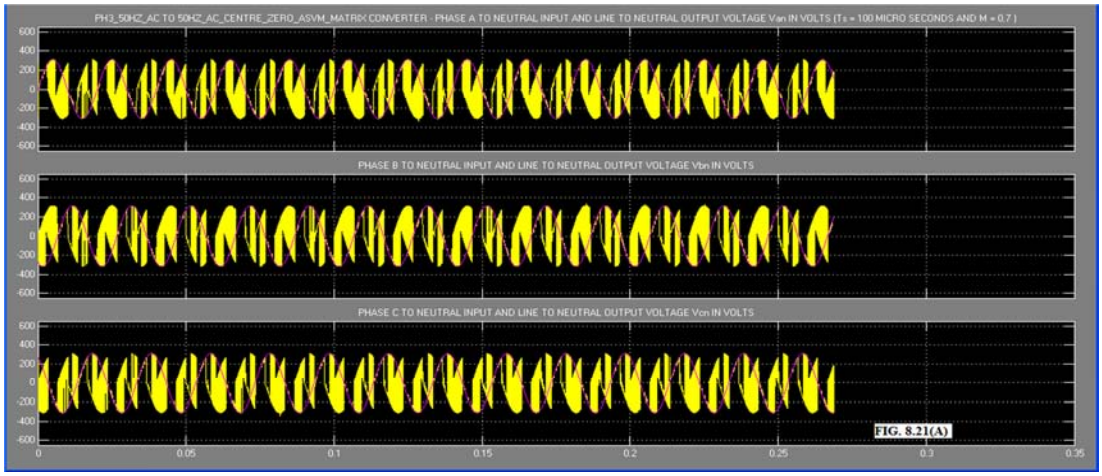
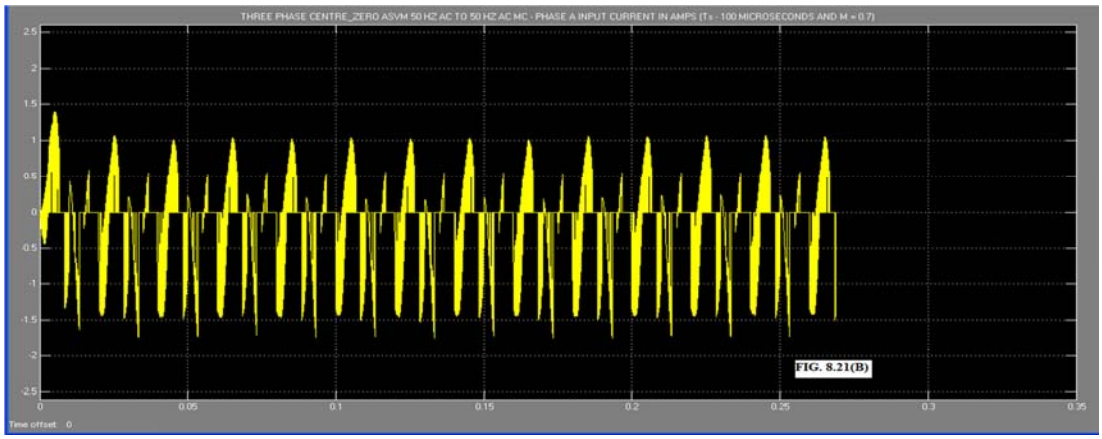
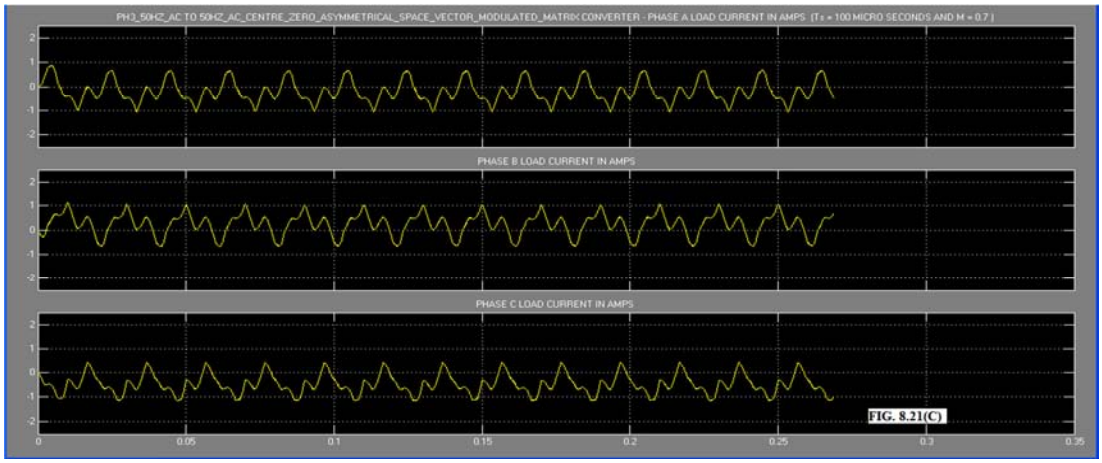
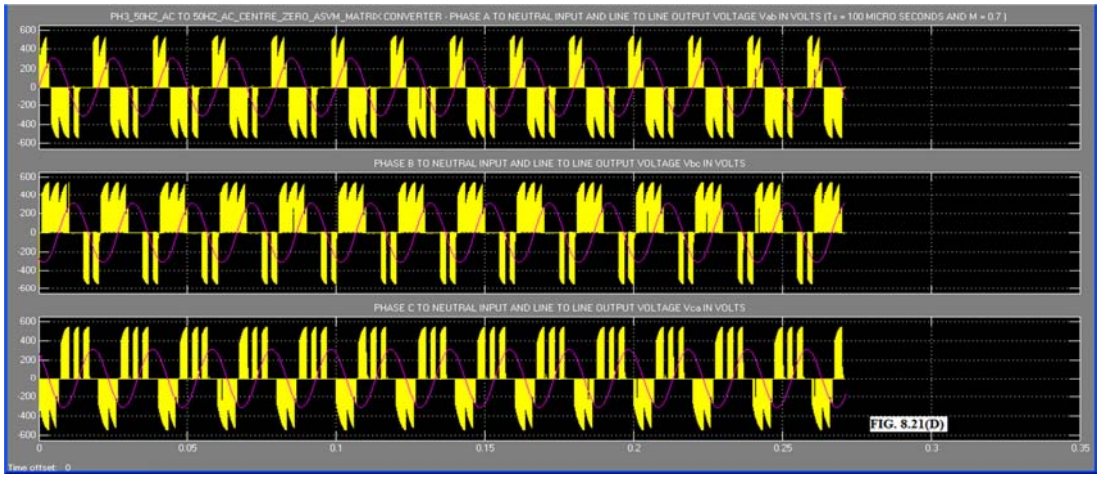


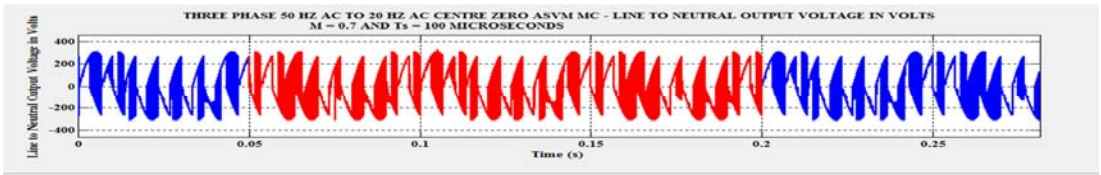
FIG. 8.20(D): THREE PHASE 50 HZ AC TO 50 HZ AC CZASVM MC - LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM


PH3_50HZ_AC TO 50HZ_AC_CENTRE_ZERO_ASVM_MATRIX CONVERTER - PHASE A TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Van IN VOLTS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vbn IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vcn IN VOLTS
FIG. 8.21(A)


THREE PHASE CENTRE_ZERO ASVM 50 HZ AC TO 50 HZ AC MC - PHASE A INPUT CURRENT IN AMPS (Ts - 100 MICROSECONDS AND M = 0.7)
FIG. 8.21(B)


PH3_50HZ_AC TO 50HZ_AC_CENTRE_ZERO_ASYMMETRICAL_SPACE_VECTOR_MODULATED_MATRIX CONVERTER - PHASE A LOAD CURRENT IN AMPS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B LOAD CURRENT IN AMPS
PHASE C LOAD CURRENT IN AMPS
FIG. 8.21(C)


PH3_50HZ_AC TO 50HZ_AC_CENTRE_ZERO_ASVM_MATRIX CONVERTER - PHASE A TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vab IN VOLTS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vbc IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vca IN VOLTS
FIG. 8.21(D)



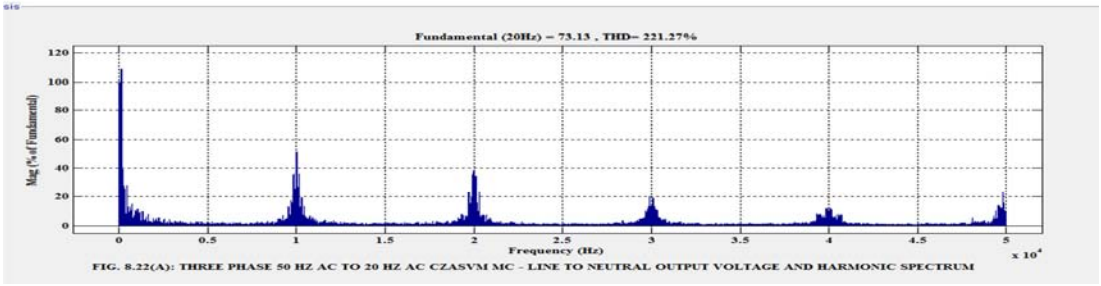
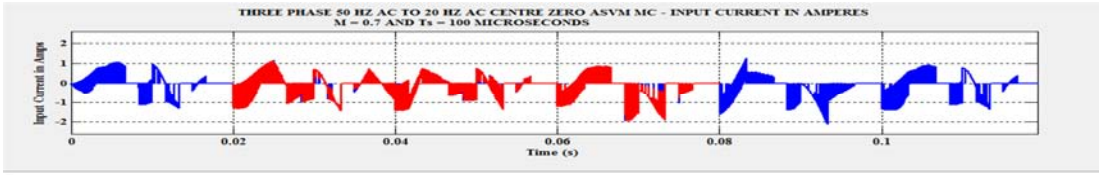


FIG. 8.22(A): THREE PHASE 50 HZ AC TO 20 HZ AC CZASVM MC - LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM



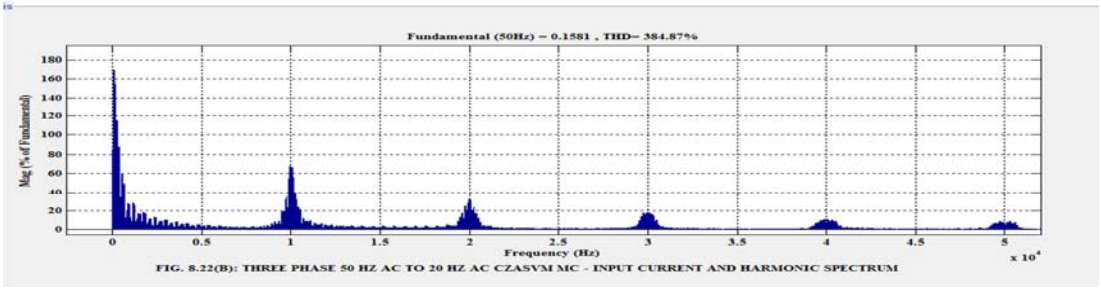
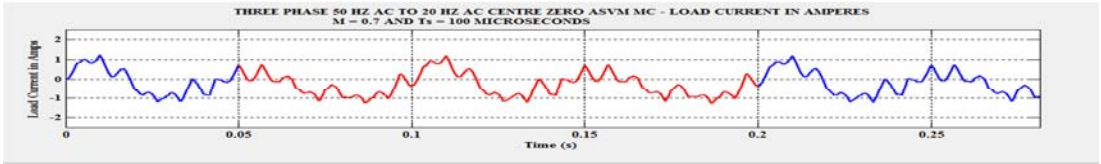


FIG. 8.22(B): THREE PHASE 50 HZ AC TO 20 HZ AC CZASVM MC - INPUT CURRENT AND HARMONIC SPECTRUM



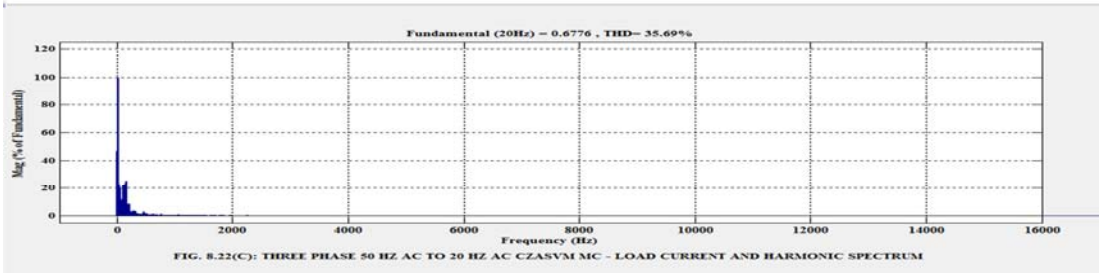
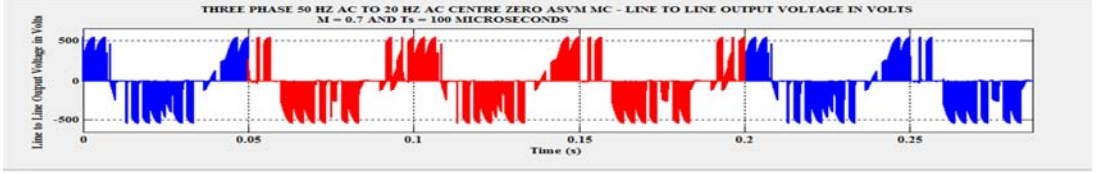


FIG. 8.22(C): THREE PHASE 50 HZ AC TO 20 HZ AC CZASVM MC - LOAD CURRENT AND HARMONIC SPECTRUM



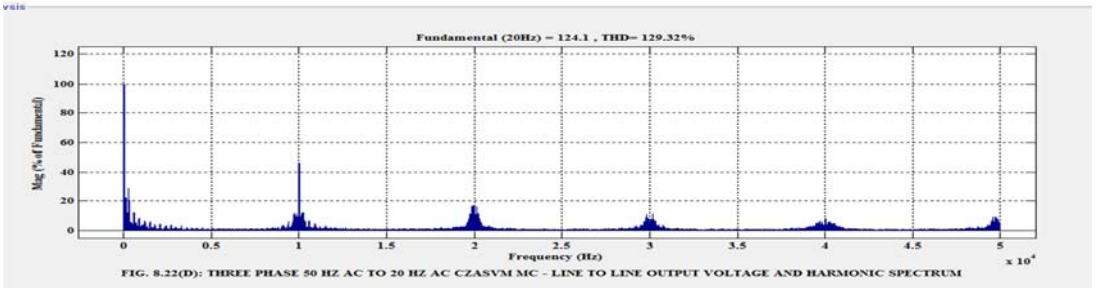
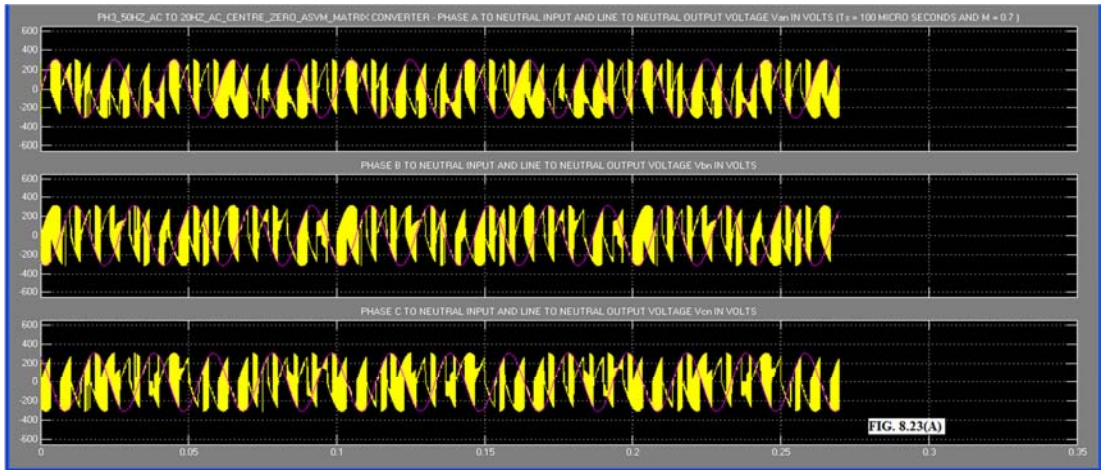
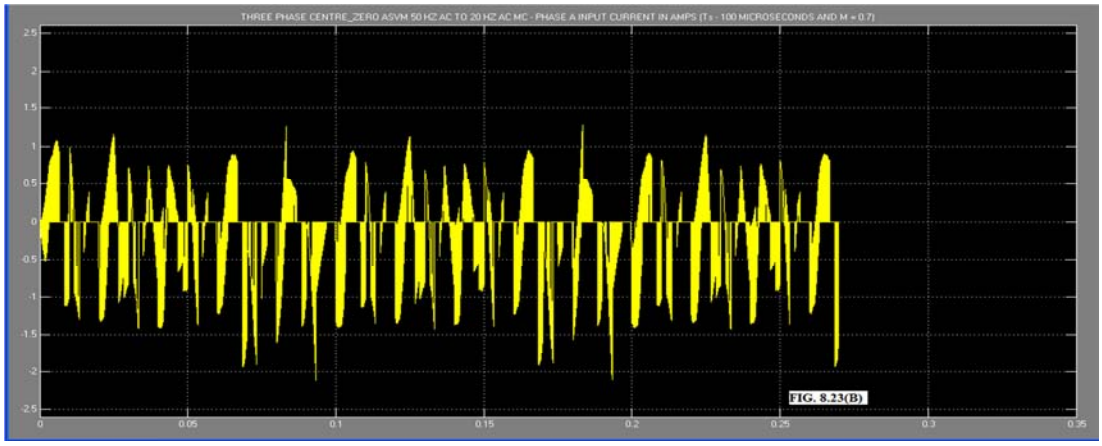
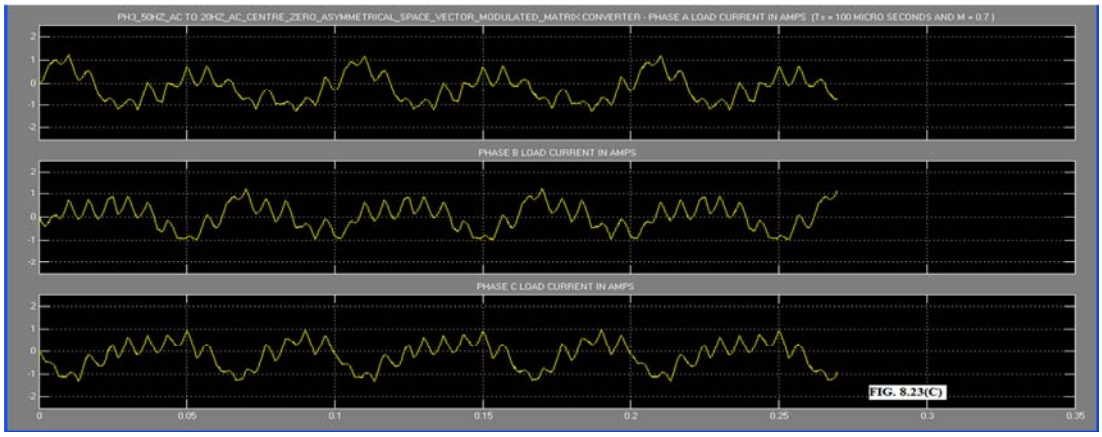
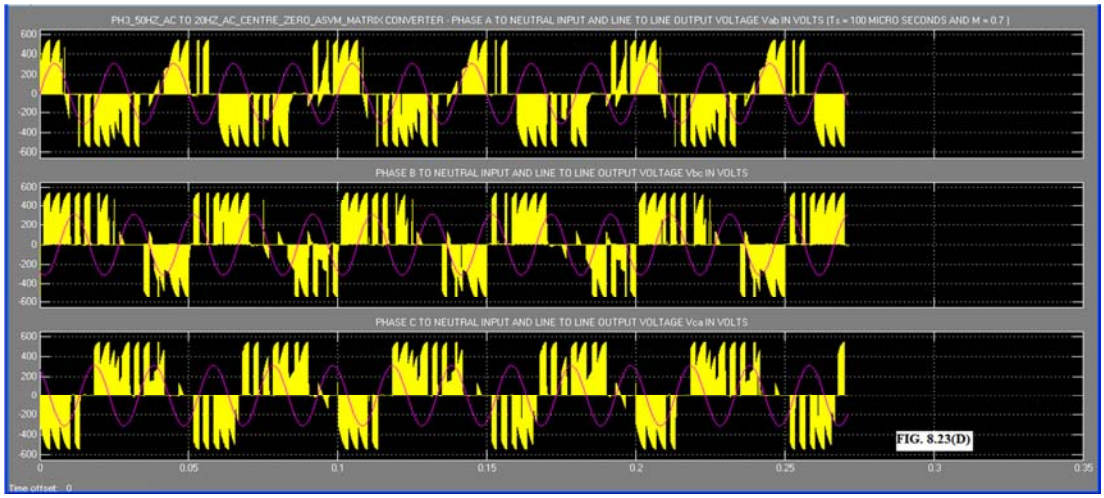


FIG. 8.22(D): THREE PHASE 50 HZ AC TO 20 HZ AC CZASVM MC - LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM


PH3_50HZ_AC TO 20HZ_AC_CENTRE_ZERO_ASVM_MATRIX CONVERTER - PHASE A TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Van IN VOLTS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vbn IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vcn IN VOLTS
FIG. 8.23(A)


THREE PHASE CENTRE_ZERO ASVM 50 HZ AC TO 20 HZ AC MC - PHASE A INPUT CURRENT IN AMPS (Ts - 100 MICROSECONDS AND M = 0.7)
FIG. 8.23(B)


PH3_50HZ_AC TO 20HZ_AC_CENTRE_ZERO_ASYMMETRICAL_SPACE_VECTOR_MODULATED_MATRIX CONVERTER - PHASE A LOAD CURRENT IN AMPS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B LOAD CURRENT IN AMPS
PHASE C LOAD CURRENT IN AMPS
FIG. 8.23(C)


PH3_50HZ_AC TO 20HZ_AC_CENTRE_ZERO_ASVM_MATRIX CONVERTER - PHASE A TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vab IN VOLTS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vbc IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vca IN VOLTS
FIG. 8.23(D)

three phase ASVM and SSVM techniques. The input power factor is assumed to be unity in this analysis. In all the three SVM techniques, it is seen from the simulation results that all the harmonic components are centred around the integral multiples of carrier switching frequency. The ASVM and CZASVM have eight commutations, whereas SSVM has twelve commutations per carrier switching period.

8.10 CONCLUSIONS: The model of the three phase AC to three phase AC MC has been developed in SIMULINK using the Duty-Cycle Space Vector approach. All possible switching combinations are represented by space vectors. The SVM technique for three phase MC is considered an optimal solution. Owing to its intrinsic two degrees of freedom, SVM technique represents the general solution of the matrix converter modulation problem and can be considered the best solution for achieving the highest voltage transfer ratio and optimizing the switching pattern through a suitable use of the zero configurations. Placing of the zero vector at the centre of the sampling interval which is named here as CZASVM technique is inferior to the ASVM and SSVM techniques from the point of view of harmonic performance of line to neutral, line to line output voltages, input current and load currents. With SVM technique modulation ratio as high as 0.866 can be achieved. The SSVM technique is found to be better from the point of view of harmonic performance of the MC as compared to ASVM and CZASVM techniques.

A8.1 APPENDIX: Using the line to line to line to neutral voltage transformation, we have the following transformation matrix:

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} * \begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} \cdots (A8.1.1)$$

From serial number 1 of Table 8.1, from the output states column, we have

$$\left.\begin{matrix} V_{ab} = V_{AB} \\ V_{bc} = 0 \\ V_{ca} = -V_{AB} \end{matrix}\right] \cdots (A8.1.2)$$

Using equation A8.1.2 in A8.1.1 and simplifying, we have

$$\left.\begin{matrix} V_{an} = \dfrac{2 * V_{AB}/\_0}{3} \\ V_{bn} = \dfrac{-V_{AB}/\_\dfrac{2\pi}{3}}{3} \\ V_{cn} = \dfrac{-V_{AB}/\_\dfrac{4\pi}{3}}{3} \end{matrix}\right] \cdots (A8.1.3)$$

The output phase voltage reference is V_{an} in equation A8.1.3, which corresponds to column 4 of Table 8.1.

Similarly corresponding to serial number 12 of Table 8.1, we have

$$\left.\begin{matrix} V_{ab} = V_{CA} \\ V_{bc} = -V_{CA} \\ V_{ca} = 0 \end{matrix}\right] \cdots (A8.1.4)$$

Using equation A8.1.4 in A.1 and simplifying, we have

$$\left.\begin{aligned} V_{an} &= \frac{V_{CA}/\_0}{3} \\ V_{bn} &= \frac{-2 * V_{CA}/\_\frac{2\pi}{3}}{3} \\ V_{cn} &= \frac{-V_{CA}/\_\frac{4\pi}{3}}{3} \end{aligned}\right] \cdots (A8.1.5)$$

The output phase voltage reference is V_{bn} in equation A8.1.5, which corresponds to column 4 of Table 8.1.

For serial number 17 of Table 8.1, we have

$$\left.\begin{aligned} V_{ab} &= 0 \\ V_{bc} &= -V_{CA} \\ V_{ca} &= V_{CA} \end{aligned}\right] \cdots (A8.1.6)$$

Using equation A8.1.6 in A8.1.1 and simplifying, we have

$$\left.\begin{aligned} V_{an} &= \frac{-V_{CA}/\_0}{3} \\ V_{bn} &= \frac{-V_{CA}/\_\frac{2\pi}{3}}{3} \\ V_{cn} &= \frac{2 * V_{CA}/\_\frac{4\pi}{3}}{3} \end{aligned}\right] \cdots (A8.1.7)$$

The output phase voltage reference is V_{cn} in equation A8.1.7, which corresponds to column 4 of Table 8.1. Similar transformation applies to input current vector, as shown below:

For phase current to line current transformation assume that the three phase load connected to the MC are in DELTA and the three phase load currents are i_{ab}, i_{bc} and i_{ca} and the input line currents are i_A, i_B and i_C respectively. Then the following transformation apply:

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = (-) * \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} * \begin{bmatrix} i_{ab} \\ i_{bc} \\ i_{ca} \end{bmatrix} \cdots (A8.1.8)$$

For serial number 1 of Table 8.1, we have iab = ia/√3; ibc = -ia/√3; ica = 0. Using this values of phase currents in equation A8.1.8, we have the following:

$$i_A = -i_a/\sqrt{3}/\_\pi/2\ ; i_B = 2 * i_a/\sqrt{3}/\_-\pi/6; i_C = -i_a/\sqrt{3}/\_-5\pi/6 \ldots \quad (A8.1.9)$$

Similarly for serial number 12 of Table 8.1, we have iab = ib/√3; ibc = 0; ica = ;-ia/√3. Using this values of phase currents in equation A8.1.8, we have the following:

$$i_A = -2 * i_b/\sqrt{3}/\_7\pi/6\ ; i_B = -i_b/\sqrt{3}/\_\pi/2; i_C = -i_b/\sqrt{3}/\_-\pi/6 \ldots \quad (A8.1.10)$$

Similarly for serial number 17 of Table 8.1, we have iab = -ic/√3; ibc = 0; ica = ;ic/√3. Using this values of phase currents in equation A8.1.8, we have the following:

$$i_A = 2 * i_c/\sqrt{3}/\_7\pi/6\ ; i_B = -i_c/\sqrt{3}/\_\pi/2; i_C = -i_c/\sqrt{3}/\_-\pi/6 \ldots \quad (A8.1.11)$$

Equations A8.1.9, A8.1.10, A8.1.11 confirms with Table 8.1 column 4.

A8.2 APPENDIX: Proof of equations 8.1 and 8.2 are given below. Referring to Fig. A8.2.1, the line voltage Vv from origin can be expressed as follows:

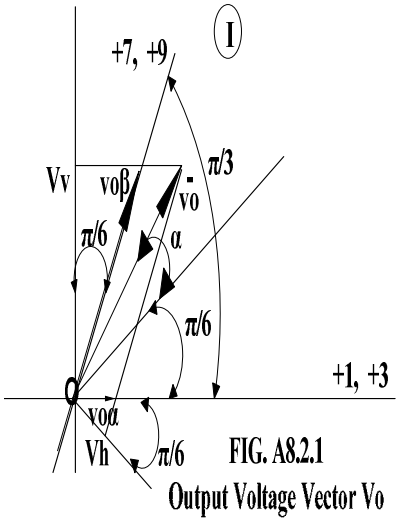


FIG. A8.2.1
Output Voltage Vector Vo

$$V_v = V_o * cos\left(\frac{\pi}{3} - \alpha\right) \ldots (A8.2.1)$$

Thus $v_{o\beta}$ from the origin can be expressed as follows:

$$v_{o\beta} = \frac{V_v}{cos\left(\frac{\pi}{6}\right)} = \frac{2}{\sqrt{3}} * V_o * cos\left(\frac{\pi}{3} - \alpha\right) \ldots (A8.2.2)$$

The expression $e^{j\left[(S_v-1).\frac{\pi}{3}+\frac{\pi}{3}\right]}$ in equation 8.1 gives the location of $v_{o\beta}$ as the output voltage sector number changes from 1 to 6. Thus in sector 1, $v_{o\beta}$ is having π/3 radians and in sector 6, this value is 2π radians.

Similarly resolving vo in a direction perpendicular to $v_{o\beta}$, we have the following equation for Vh from the origin:

$$V_h = V_o * cos\left(\frac{\pi}{3} + \alpha\right) \ldots (A8.2.3)$$

Thus $v_{o\alpha}$ from the origin can be expressed as follows:

$$v_{o\alpha} = \frac{V_h}{cos\left(\frac{\pi}{6}\right)} = \frac{2}{\sqrt{3}} * V_o * cos\left(\frac{\pi}{3} + \alpha\right) \ldots (A8.2.4)$$

The expression $e^{j\left[(S_v-1).\frac{\pi}{3}\right]}$ in equation 8.2 gives the location of $v_{o\alpha}$ as the output voltage sector number changes from 1 to 6. Thus in sector 1, $v_{o\alpha}$ is having zero radians and in sector 6, this value is 5π/3 radians.

The solution of equations 8.1 and 8.3, to find the duty cycle δ^I and δ^{II} for the first two switching configurations are given below:

$$\delta^I = \frac{\begin{bmatrix} \frac{2}{\sqrt{3}} * v_o * cos\left(\alpha - \frac{\pi}{3}\right) * e^{j\left[(S_v-1).\frac{\pi}{3}+\frac{\pi}{3}\right]} & \overrightarrow{v_o^{II}} \\ 0 & \overrightarrow{i_i^{II}} * je^{j\beta} * e^{j(S_i-1).\frac{\pi}{3}} \end{bmatrix}}{\begin{bmatrix} \overrightarrow{v_o^I} & \overrightarrow{v_o^{II}} \\ \overrightarrow{i_i^I} * je^{j\beta} * e^{j(S_i-1).\frac{\pi}{3}} & \overrightarrow{i_i^{II}} * je^{j\beta} * e^{j(S_i-1).\frac{\pi}{3}} \end{bmatrix}} \ldots (A8.2.5)$$

Simplifying and rewriting equation A8.2.5, we have the following:

$$\delta^I = \left[\frac{\frac{2}{\sqrt{3}} * v_o * \overrightarrow{i_i^{II}} * cos\left(\alpha - \frac{\pi}{3}\right) * e^{j\left[(S_v+S_i-2).\frac{\pi}{3}+\frac{\pi}{3}+\beta\right]}}{\overrightarrow{v_o^I} * \overrightarrow{i_i^{II}} * e^{j\left[(S_i-1).\frac{\pi}{3}+\beta\right]} - \overrightarrow{v_o^{II}} * \overrightarrow{i_i^I} * e^{j\left[(S_i-1).\frac{\pi}{3}+\beta\right]}}\right] \ldots (A8.2.6)$$

Considering the real part, the denominator of equation A8.2.6 gives the output power delivered. This is also the input power neglecting switching losses. Thus the denominator of equation A8.2.6 can be replaced by the following:

$$\overrightarrow{v_o^I} * \overrightarrow{i_i^{II}} * e^{j\left[(S_i-1).\frac{\pi}{3}+\beta\right]} - \overrightarrow{v_o^{II}} * \overrightarrow{i_i^{I}} * e^{j\left[(S_i-1).\frac{\pi}{3}+\beta\right]} = V_i * I_i * cos(\varphi_i) \ldots (A8.2.7)$$

In equation A8.2.6, $\overrightarrow{i_i^I}$, $\overrightarrow{i_i^{II}}$ are the value of I_i for the first and second switching configuration. Thus using equation A8.2.6 and A8.2.7, duty-cycle δ^I can be expressed as follows:

$$\delta^I = \frac{\frac{2}{\sqrt{3}} * q * cos\left(\alpha - \frac{\pi}{3}\right) * cos\left[(S_v + S_i - 2).\frac{\pi}{3} + \frac{\pi}{3} + \beta\right]}{cos(\varphi_i)} \ldots (A8.2.8)$$

Similarly solving for duty-cycle δ^{II} we have the following equation:

$$\delta^{II} = \left[\frac{\frac{2}{\sqrt{3}} * v_o * \overrightarrow{i_i^I} * cos\left(\alpha - \frac{\pi}{3}\right) * e^{j\left[(S_v+S_i-2).\frac{\pi}{3}+\frac{\pi}{3}+\beta\right]}}{\overrightarrow{v_o^I} * \overrightarrow{i_i^{II}} * e^{j\left[(S_i-1).\frac{\pi}{3}+\beta\right]} - \overrightarrow{v_o^{II}} * \overrightarrow{i_i^{I}} * e^{j\left[(S_i-1).\frac{\pi}{3}+\beta\right]}}\right] \ldots (A8.2.9)$$

$$i.e., \quad \delta^{II} = \frac{\frac{2}{\sqrt{3}} * q * cos\left(\alpha - \frac{\pi}{3}\right) * cos\left[(S_v + S_i - 2).\frac{\pi}{3} + \frac{\pi}{3} + \beta\right]}{cos(\varphi_i)} \ldots (A8.2.10)$$

Duty-cycle δ^I corresponds to the case when (Sv+Si) is odd. Thus when (Sv+Si) is 3, using equation A8.2.8, cos (β+2π/3) can be expressed as cos[π + (β - π/3)] which is (-1)*cos(β - π/3). Thus equation A8.2.8 can be expressed as follows:

$$\delta^I = \frac{(-1)^{(S_v+S_i)} * \frac{2}{\sqrt{3}} * q * cos\left(\alpha - \frac{\pi}{3}\right) * cos(\beta - \pi/3)}{cos(\varphi_i)} \ldots (A8.2.11)$$

Duty-cycle δ^{II} corresponds to the case when (Sv+Si) is even. Thus when (Sv+Si) is 2, using equation A8.2.9, we have the following:

$$\delta^{II} = \frac{(-1)^{(S_v+S_i+1)} * \frac{2}{\sqrt{3}} * q * cos\left(\alpha - \frac{\pi}{3}\right) * cos(\beta + \pi/3)}{cos(\varphi_i)} \ldots (A8.2.12)$$

In equations A8.2.11 and A8.2.12, q is the voltage transfer ratio vo/vi. Similar derivations hold good for δ^{III} and δ^{IV}, as given below:

The solution of equations 8.2 and 8.4, to find the duty cycle δ^{III} and δ^{IV} for the third and fourth switching configurations are given below:

$$\delta^{III} = \frac{\begin{bmatrix} \frac{2}{\sqrt{3}} * v_o * cos\left(\alpha + \frac{\pi}{3}\right) * e^{j\left[(S_v-1).\frac{\pi}{3}\right]} & \overrightarrow{v_o^{IV}} \\ 0 & \overrightarrow{i_i^{IV}} * je^{j\beta} * e^{j(S_i-1).\frac{\pi}{3}} \end{bmatrix}}{\begin{bmatrix} \overrightarrow{v_o^{III}} & \overrightarrow{v_o^{IV}} \\ \overrightarrow{i_i^{III}} * je^{j\beta} * e^{j(S_i-1).\frac{\pi}{3}} & \overrightarrow{i_i^{IV}} * je^{j\beta} * e^{j(S_i-1).\frac{\pi}{3}} \end{bmatrix}} \ldots (A8.2.13)$$

Simplifying and rewriting equation A8.2.13, we have the following:

$$\delta^{III} = \left[\frac{\frac{2}{\sqrt{3}} * v_o * \overrightarrow{i_i^{IV}} * cos\left(\alpha + \frac{\pi}{3}\right) * e^{j\left[(S_v+S_i-2).\frac{\pi}{3}+\beta\right]}}{\overrightarrow{v_o^{III}} * \overrightarrow{i_i^{IV}} * e^{j\left[(S_i-1).\frac{\pi}{3}+\beta\right]} - \overrightarrow{v_o^{IV}} * \overrightarrow{i_i^{III}} * e^{j\left[(S_i-1).\frac{\pi}{3}+\beta\right]}}\right] \ldots (A8.2.14)$$

Considering the real part, the denominator of equation A8.2.14 gives the output power delivered. This is also the input power neglecting switching losses. Thus the denominator of equation A8.2.14 can be replaced by the following:

$$\overrightarrow{v_o^{III}} * \overrightarrow{i_i^{IV}} * e^{j\left[(S_i-1).\frac{\pi}{3}+\beta\right]} - \overrightarrow{v_o^{IV}} * \overrightarrow{i_i^{III}} * e^{j\left[(S_i-1).\frac{\pi}{3}+\beta\right]} = V_i * I_i * cos(\varphi_i) \ldots (A8.2.15)$$

In equation A8.2.14, $\overrightarrow{i_i^{III}}, \overrightarrow{i_i^{IV}}$ are the value of I_i for the third and fourth switching configuration. Thus using equation A8.2.14 and A8.2.15, duty-cycle δ^{III} can be expressed as follows:

$$\delta^{III} = \frac{\frac{2}{\sqrt{3}} * q * cos\left(\alpha + \frac{\pi}{3}\right) * cos\left[(S_v + S_i - 2).\frac{\pi}{3} + \beta\right]}{cos(\varphi_i)} \ldots (A8.2.16)$$

Similarly solving for duty-cycle δ^{IV} we have the following equation:

$$\delta^{IV} = \left[\frac{\frac{2}{\sqrt{3}} * v_o * \overrightarrow{i_i^{III}} * cos\left(\alpha + \frac{\pi}{3}\right) * e^{j\left[(S_v+S_i-2).\frac{\pi}{3}+\beta\right]}}{\overrightarrow{v_o^{III}} * \overrightarrow{i_i^{IV}} * e^{j\left[(S_i-1).\frac{\pi}{3}+\beta\right]} - \overrightarrow{v_o^{IV}} * \overrightarrow{i_i^{III}} * e^{j\left[(S_i-1).\frac{\pi}{3}+\beta\right]}}\right] \ldots (A8.2.17)$$

$$i.e., \quad \delta^{IV} = \frac{\frac{2}{\sqrt{3}} * q * cos\left(\alpha - \frac{\pi}{3}\right) * cos\left[(S_v + S_i - 2).\frac{\pi}{3} + \frac{\pi}{3} + \beta\right]}{cos(\varphi_i)} \ldots (A8.2.18)$$

Duty-cycle δ^{III} corresponds to the case when (Sv+Si) is even. Thus when (Sv+Si) is 4, using equation A8.2.14, cos (β+2π/3) can be expressed as cos[π + (β - π/3)] which is (-1)*cos(β - π/3). Thus equation A8.2.16 can be expressed as follows:

$$\delta^{III} = \frac{(-1)^{(S_v+S_i+1)} * \frac{2}{\sqrt{3}} * q * cos\left(\alpha + \frac{\pi}{3}\right) * cos(\beta - \pi/3)}{cos(\varphi_i)} \ldots (A8.2.19)$$

Duty-cycle δ^{IV} corresponds to the case when (Sv+Si) is odd. Thus when (Sv+Si) is 3, using equation A8.2.17, we have the following:

$$\delta^{IV} = \frac{(-1)^{(S_v+S_i)} * \frac{2}{\sqrt{3}} * q * cos\left(\alpha + \frac{\pi}{3}\right) * cos(\beta + \pi/3)}{cos(\varphi_i)} \ldots (A8.2.20)$$

Equations A8.2.19 and A8.2.20 well agree with equations 8.7 and 8.8 respectively.

Chapter IX
Indirect Space Vector Modulation of Three Phase AC to Three Phase AC Matrix Converter

9.1 INTRODUCTION: Three Phase AC to Three Phase AC Matrix Converter has advantages over the conventional three phase rectifier-inverter frequency converters in the sense that the former directly converts AC voltage at any given frequency to AC output voltage of any other magnitude and frequency without the need for a DC link capacitor storage element and with a regeneration capability [25-30]. In the proposed voltage Space Vector PWM control of MCs, the Indirect Transfer Function (ITF) approach is used where the input AC voltage is first rectified to create a fictitious DC voltage which is then inverted at the required output frequency [25-30]. For low harmonic distortion, the inverter operation is achieved by Space Vector Modulation (SVM) simultaneously with input current SVM for rectification [25-30]. The simultaneous output voltage-input current SVM algorithm is reviewed here and the model of the 3 X 3 MC is derived based on this algorithm using SIMULINK. The simulation results are presented.

9.2 PRINCIPLE OF INDIRECT SPACE VECTOR MODULATION: The three phase AC to three phase AC Conventional Matrix Converter (CMC) is shown in Fig. 9.1 with the load represented

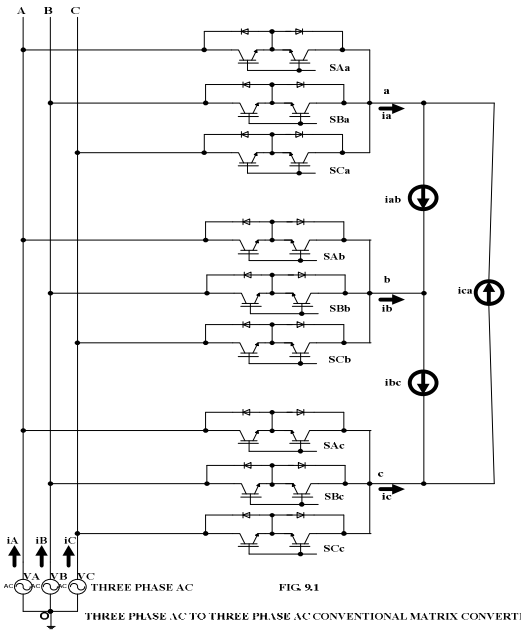


FIG. 9.1

THREE PHASE AC TO THREE PHASE AC CONVENTIONAL MATRIX CONVERTER

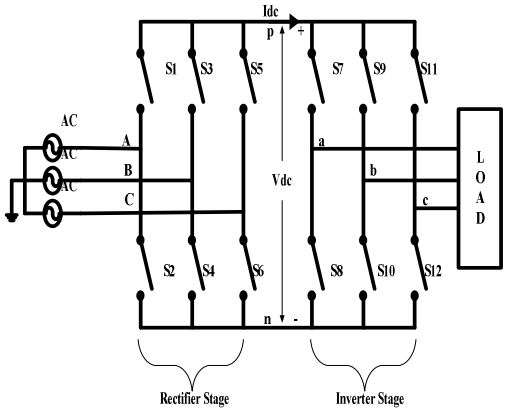


FIG. 9.2

MATRIX CONVERTER EQUIVALENT CIRCUIT

as a current source connected in delta. The equivalent circuit of this CMC is shown in Fig. 9.2. The CMC can be considered equivalent to a three phase rectifier forming a virtual DC link output voltage which is then inverted using a three phase inverter to get the required AC output voltage and frequency [25-30]. The model equivalence of Fig. 9.1 and Fig. 9.2 can be expressed as follows:

$$\begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} = \begin{bmatrix} S_7 & S_8 \\ S_9 & S_{10} \\ S_{11} & S_{12} \end{bmatrix} \cap \begin{bmatrix} S_1 & S_3 & S_5 \\ S_2 & S_4 & S_6 \end{bmatrix}$$

$$= \left[\begin{array}{cc|c} (S_7 \cap S_1) \cup (S_8 \cap S_2) & (S_7 \cap S_3) \cup (S_8 \cap S_4) & (S_7 \cap S_5) \cup (S_8 \cap S_6) \\ (S_9 \cap S_1) \cup (S_{10} \cap S_2) & (S_9 \cap S_3) \cup (S_{10} \cap S_4) & (S_9 \cap S_5) \cup (S_{10} \cap S_6) \\ \hline (S_{11} \cap S_1) \cup (S_{12} \cap S_2) & (S_{11} \cap S_3) \cup (S_{12} \cap S_4) & (S_{11} \cap S_5) \cup (S_{12} \cap S_6) \end{array}\right] \quad (9.1)$$

where $\cap$ *= Logical AND;* $\cup$ *= Logical OR.*

The basic idea of the indirect SVM (ISVM) technique is to decouple the control of the input current and the control of the output voltage. Modeling the matrix converter in this way enables the well-known space vector PWM to be applied for a rectifier as well as an inverter stage independently [25-30, 41].

9.3 INDIRECT SPACE VECTOR MODULATION ALGORITHM: The 3 X 3 matrix converter shown in Fig.9.1 connects the three phase ac source to the three phase load. The switching Function for a 3 X 3 matrix converter can be defined as in equations 3.1 and 3.2 under section 3.2 in Chapter III. Also the twenty seven switching states of the 3 X 3 MC is presented in Table 3.1 in Chapter III. Using this Table 3.1 and Fig. 9.1, the following expressions for the output line voltage and input phase currents are obtained:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} (S_{Aa} - S_{Ab}) & (S_{Ba} - S_{Bb}) & (S_{Ca} - S_{Cb}) \\ (S_{Ab} - S_{Ac}) & (S_{Bb} - S_{Bc}) & (S_{Cb} - S_{Cc}) \\ (S_{Ac} - S_{Aa}) & (S_{Bc} - S_{Ba}) & (S_{Cc} - S_{Ca}) \end{bmatrix} * \begin{bmatrix} v_{AO} \\ v_{BO} \\ v_{CO} \end{bmatrix} \quad (9.2)$$

$$\text{i.e. } v_{oL} = \lceil T_{phL} \rceil * v_{iph} \quad (9.3)$$

$$\text{and } i_{iph} = \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \lceil T_{phL} \rceil^T * \begin{bmatrix} i_{ab} \\ i_{bc} \\ i_{ca} \end{bmatrix} = \lceil T_{phL} \rceil^T * i_{OL} \quad (9.4)$$

T_{phL} is the instantaneous input phase to output line Transfer Function matrix of the three phase MC.

$$v_{oph} = \begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} * \begin{bmatrix} v_{AO} \\ v_{BO} \\ v_{CO} \end{bmatrix} = \lceil T_{phph} \rceil * \lceil v_{iph} \rceil \quad (9.5)$$

$$\text{and } i_{iph} = \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \lceil T_{phph} \rceil^T * \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \lceil T_{phph} \rceil^T * i_{oph} \quad (9.6)$$

T_{phph} is the instantaneous input phase to output phase matrix. To use the HF synthesis, the switching frequency must be higher than the frequency of the input voltages and output currents. The switching function s_{Kj} is the duty-cycle of the switch S_{Kj} and is denoted by M_{Kj}. The LF equivalents are given below:

$$0 \leq M_{Kj} \leq 1 \text{ where } K \in A, B, C \text{ and } j \in a, b, c. \quad (9.7)$$

$$M_{Aj} + M_{Bj} + M_{Cj} = 1 \text{ for } j \in a, b, c \quad (9.8)$$

The remaining LF equivalents are given in equations 9.4 to 9.7. Equations for T_{phL} and `T_{phph} can now be rewritten as follows:

$$\lceil T_{phL} \rceil = \begin{bmatrix} (M_{Aa} - M_{Ab}) & (M_{Ba} - M_{Bb}) & (M_{Ca} - M_{Cb}) \\ (M_{Ab} - M_{Ac}) & (M_{Bb} - M_{Bc}) & (M_{Cb} - M_{Cc}) \\ (M_{Ac} - M_{Aa}) & (M_{Bc} - M_{Ba}) & (M_{Cc} - M_{Ca}) \end{bmatrix} \quad (9.9)$$

$$\text{and } \left[T_{phph}\right] = \begin{bmatrix} M_{Aa} & M_{Ba} & M_{Ca} \\ M_{Ab} & M_{Bb} & M_{Cb} \\ M_{Ac} & M_{Bc} & M_{Cc} \end{bmatrix} \qquad (9.10)$$

Let the input phase voltage be expressed as follows:

$$v_{iph} = V_{im} * \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t - 120°) \\ \cos(\omega_i t + 120°) \end{bmatrix} \quad (9.11)$$

The averaged output line voltage is expressed as follows:

$$v_{oL} = \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \sqrt{3} * V_{om} * \begin{bmatrix} \cos(\omega_o t - \varphi_o + 30°) \\ \cos(\omega_o t - \varphi_o + 30° - 120°) \\ \cos(\omega_o t - \varphi_o + 30° + 120°) \end{bmatrix} \qquad (9.12)$$

where φ_O is the output phase displacement angle. The input phase to output line transfer matrix is chosen as follows:

$$\left[\mathrm{T_{phL}}\right] = \mathrm{m} * \begin{bmatrix} \cos(\omega_o t - \varphi_o + 30°) \\ \cos(\omega_o t - \varphi_o + 30° - 120°) \\ \cos(\omega_o t - \varphi_o + 30° + 120°) \end{bmatrix} * \begin{bmatrix} \cos(\omega_i t - \varphi_i) \\ \cos(\omega_i t - \varphi_i - 120°) \\ \cos(\omega_i t - \varphi_i + 120°) \end{bmatrix}^T \qquad (9.13)$$

where $0 \leq \mathrm{m} \leq 1$ is the modulation index and φ_i is the input phase displacement angle.

Equations 9.11 to 9.13 satisfy equation 9.3 for value of Vom given below:

$$V_{om} = \frac{\sqrt{3}}{2} * V_{im} * m * \cos(\varphi_i) \qquad (9.14)$$

The proof of equation 9.14 is given in A9.1Appendix. The output line current is assumed sinusoidal and is given below:

$$i_{OL} = \begin{bmatrix} i_{ab} \\ i_{bc} \\ i_{ca} \end{bmatrix} = \frac{I_{om}}{\sqrt{3}} * \begin{bmatrix} \cos(\omega_o t - \varphi_o - \varphi_L + 30°) \\ \cos(\omega_o t - \varphi_o - \varphi_L + 30° - 120°) \\ \cos(\omega_o t - \varphi_o - \varphi_L + 30° + 120°) \end{bmatrix} \qquad (9.15)$$

where φ_L is the load displacement angle. At the output frequency fo Hz. If equations 9.14 and 9.15 are substituted in equation 9.4, the local averaged input currents are obtained as given below:

$$i_{iph} = \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = I_{im} * \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t - 120°) \\ \cos(\omega_i t + 120°) \end{bmatrix} \qquad (9.16)$$

where

$$I_{im} = \frac{\sqrt{3}}{2} * I_{om} * m * \cos(\varphi_L) \qquad (9.17)$$

The proof of equation 9.17 is given in A9.2Appendix. Unity input displacement factor is obtained by letting φ_i equal to zero which from equation 9.14 results in a voltage gain of 0.866 for unity modulation index. The HF synthesis requires determination of the value of duty-cycle M_{Kj} and the position of the switching pulses such that the constraint given by equations 9.7 and 9.8 are satisfied and the required transfer matrix given by equation 9.13 is implemented. For the control of three phase AC to three phase MC, indirect and direct Transfer Function approaches are used. Here Indirect Transfer Function (ITF) approach is discussed below:

Equation 9.13 represents the ITF approach. The transfer matrix T_{phL} may be expressed as follows:

$$\left[T_{phL}\right] = \left[T_{VSI}(\omega_O)\right] * \left[T_{VSR}(\omega_i)\right]^T \qquad (9.18)$$

Multiplying $[T_{VSR}(\omega_i)]^T$ with input phase voltage vector given by equation 9.11, the following is obtained:

$$[T_{VSR}(\omega_i)]^T * v_{iph} = \frac{3}{2} * V_{im} * \cos(\varphi_i) \qquad (9.19)$$

This constant voltage given by equation 9.19 represents the operation of a Voltage Source Rectifier (VSR). Equation 9.19 is derived in A9.3Appendix. Multiplying equation 9.19 with $[T_{VSI}(\omega_O)]$, the operation of a Voltage Source Inverter (VSI) is obtained. Therefor ITF approach emulates a VSR-VSI combination as shown in Fig. 9.2. From Fig. 9.2, it is clear that the three phase to three phase matrix converter falls to one of the six possible subtopologies with Vdc $\in [V_{ab}, V_{bc}, V_{ca}, V_{ba}, V_{cb}, V_{ac}]$. It can be seen that for each allowed switching combination in Fig. 9.2, there is only one allowed switching combination in Table 3.1 of chapter III that results in the same output voltage and input current. The ITF approach enables application of well known VSR-VSI PWM technique for three phase AC to three phase AC MC control.

Here based on the ITF approach, Space Vector Modulation (SVM) is simultaneously employed for both VSR and VSI part of the MC. The procedure for VSI SVM and VSR SVM are reviewed and their LF transfer functions are derived. The steps for HF synthesis of the simultaneous output voltage and input current SVM are derived and the representation of the modulation process in the complex plane is given.

9.3.1 VOLTAGE SOURCE INVERTER OUTPUT VOLTAGE SVM: Consider the voltage source inverter part of Fig. 9.2, supplied by a DC

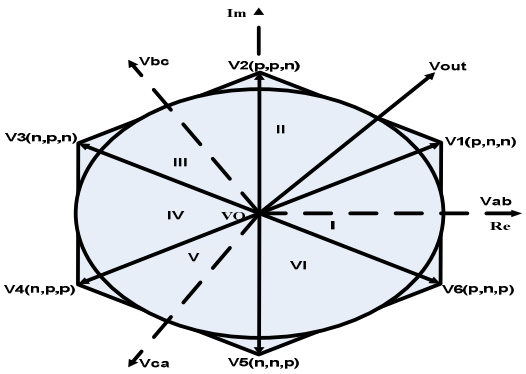
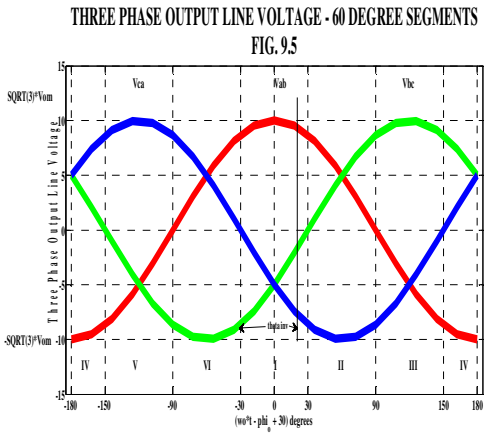


FIG. 9.3
OUTPUT VOLTAGE VECTOR HEXAGON



voltage source vpn = Vdc. The VSI can assume six non-zero and two zero output voltage values. The resulting output line voltage space vector is defined below:

$$v_{oL} = \frac{2}{3} * (v_{ab} + v_{bc}.e^{+j120} + v_{ca}.e^{-j120}) \qquad (9.20)$$

The output line voltage space vector can assume seven discrete Voltage Switching Space Vectors

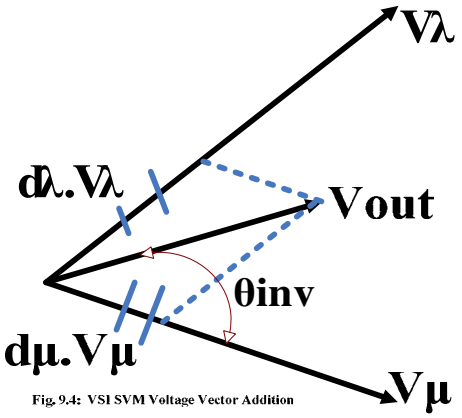


Fig. 9.4: VSI SVM Voltage Vector Addition

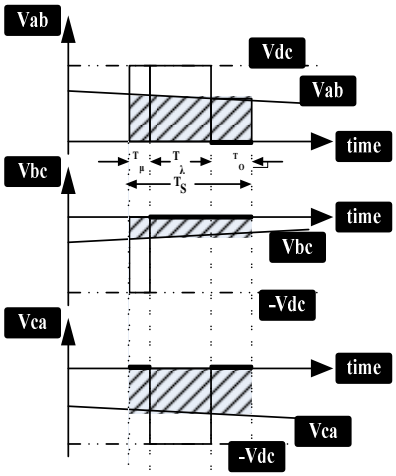


FIG. 9.6: SYNTHESIS OF VSI OUTPUT LINE VOLTAGE

(SSV's) Vo – V6 shown in Fig. 9.3. The desired output line voltage space vector is given below:

$$v_{oL} = \sqrt{3} * V_{om} * e^{j(\omega_O.t - \varphi_O + 30)} \qquad (9.21)$$

The line voltage space vector can be resolved into Vμ, Vλ, and Vo using PWM as shown in Fig. 9.4. In Fig. 9.4, Vout is the sampled value of v_{oL} at any instant within the switching period Ts. The duty-cycles of the two SSVs are given below:

$$d_\mu = \frac{T_\mu}{T_S} = m_V * \sin\left(\frac{\pi}{3} - \theta_{inv}\right) \qquad (9.22)$$

$$d_\lambda = \frac{T_\lambda}{T_S} = m_V * \sin(\theta_{inv}) \qquad (9.23)$$

$$d_{ov} = \frac{T_{ov}}{T_S} = \left(1 - d_\mu - d_\lambda\right) \qquad (9.24)$$

Where m_V is the voltage modulation index whose range is defined below:

$$0 \le m_V \le \frac{\left(\sqrt{3} * V_{Om}\right)}{V_{dc}} \le 1 \qquad (9.25)$$

The sectors of the VSI hexagon in Fig. 9.3 correspond to the six 60 degree segments within a period of the desired three phase output line voltages shown in Fig. 9.5. In Fig. 9.6, the line voltage during the period T_μ correspond V6(p,n,p), T_λ correspond to V1(p,n,n) and To correspond to zero voltage vector in Fig. 9.3. When the switching in Fig. 9.2 correspond to V6(p,n,p), the line to line output voltages Vab, Vbc and Vca are +Vdc, -Vdc and zero and when this switching is V1(p,n,n) the corresponding line to line output voltages are +Vdc, zero and –Vdc respectively. These values are shown in Fig. 9.6. The local averaged output line voltages are given below:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} d_\mu + d_\lambda \\ -d_\mu \\ -d_\lambda \end{bmatrix} * V_{dc} \qquad (9.26)$$

Using equation 9.22 to 9.23 in 9.26, the following:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = m_v * \begin{bmatrix} \cos(\theta_{inv} - 30°) \\ -\sin(60° - \theta_{inv}) \\ -\sin(\theta_{inv}) \end{bmatrix} * V_{dc} \qquad (9.27)$$

For the first sixty degree segment

$$-30° \le (\omega_o.t - \varphi_o + 30°) \le 30°$$

$$\theta_{inv} = \left(\omega_o.t - \varphi_o + 30°\right) + 30° \qquad (9.28)$$

Using equation 9.28 in equation 9.27, we have the following:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \mathrm{m_v} * \begin{bmatrix} \cos(\omega_o t - \varphi_o + 30°) \\ \cos(\omega_o t - \varphi_o + 30° - 120°) \\ \cos(\omega_o t - \varphi_o + 30° + 120°) \end{bmatrix} * V_{dc} = T_{VSI} * V_{dc} \qquad (9.29)$$

T_{VSI} in equation 9.29 is the LF transfer matrix of VSI. Using equation 9.25 in equation 9.29, equation 9.12 is obtained. The local averaged input current is defined as follows:

$$i_{dc} = [T_{VSI}]^T * i_{OL} = \frac{\sqrt{3}}{2} * I_{om} * m_v * \cos(\varphi_L) \qquad (9.30)$$

9.3.2 VOLTAGE SOURCE RECTIFIER INPUT CURRENT SVM: Consider the VSR part of Fig.9.2 as a standalone VSR loaded by a DC current generator I_{dc}. The VSR input current hexagon is similar to VSI output voltage hexagon except that the subscripts μ, λ and inv are replaced by α, β and rect respectively. The VSR hexagon is shown in Fig. 9.7. The input current space vector is shown in Fig. 9.8. The VSR duty-cycles are defined below:

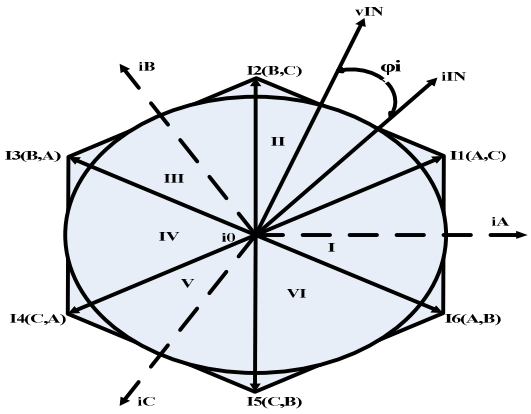


FIG. 9.7
INPUT CURRENT VECTOR HEXAGON

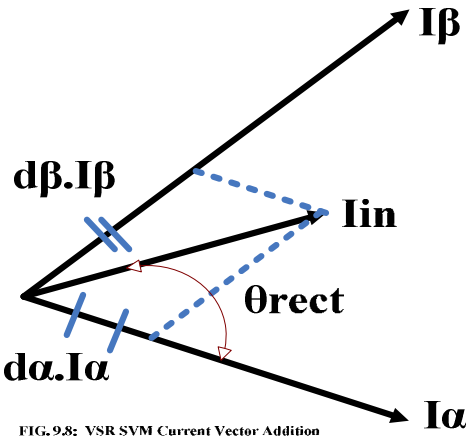


FIG. 9.8: VSR SVM Current Vector Addition

$$d_\alpha = \frac{T_\alpha}{T_S} = m_c * \sin\left(\frac{\pi}{3} - \theta_{rect}\right) \qquad (9.31)$$

$$d_\beta = \frac{T_\beta}{T_S} = m_c * \sin(\theta_{rect}) \qquad (9.32)$$

$$d_{ov} = \frac{T_{oc}}{T_S} = \left(1 - d_\alpha - d_\beta\right) \qquad (9.33)$$

Where m_c is the VSR modulation index whose range is defined below:

$$0 \leq m_c \leq \frac{I_{im}}{I_{dc}} \leq 1 \qquad (9.34)$$

The local averaged input phase currents in the first sector of VSR hexagon are given below:

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} d_\alpha + d_\beta \\ -d_\alpha \\ -d_\beta \end{bmatrix} * I_{dc} \qquad (9.35)$$

$$= m_c * \begin{bmatrix} \cos(\theta_{rect} - 30°) \\ -\sin(60° - \theta_{rect}) \\ -\sin(\theta_{rect}) \end{bmatrix} * I_{dc} \qquad (9.36)$$

But θ_{rect} in the first sector of input current hexagon can be expressed as follows:

$$\theta_{rect} = (\omega_i.t - \varphi_i + 30°) \qquad (9.37)$$

$$-30° \leq (\omega_i.t - \varphi_i) \leq +30°$$

Using equation 9.37 in equation 9.36, the LF transfer matrix T_{VSR} for the first sector of input current hexagon is defined as follows:

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = m_c * \begin{bmatrix} \cos(\omega_i.t - \varphi_i) \\ \cos(\omega_i.t - \varphi_i - 120°) \\ \cos(\omega_i.t - \varphi_i + 120°) \end{bmatrix} * I_{dc} = T_{VSR} * I_{dc} \qquad (9.38)$$

Using equation 9.34 in 9.38, equation 9.16 is obtained. The VSR local averaged output voltage v_{pn} = V_{dc} in Fig. 9.2 is obtained as follows:

$$v_{pn} = V_{dc} = [T_{VSR}]^T * v_{iph} = \frac{3}{2} * V_{im} * m_c * \cos(\varphi_i) \qquad (9.39)$$

9.3.3 MATRIX CONVERTER OUTPUT VOLTAGE AND INPUT CURRENT SVM: The local averaged output voltage of the SVM VSR given in equation 9.39 and that for the input current SVM VSI given in equation 9.30 are constants and hence can be directly interconnected. Also it is seen that the product $[T_{VSR}]*[T_{VSI}]^T$ from equation 9.38 and 9.29 correspond to T_{phL} in equation 9.13 where m corresponds to the product m_v*m_c. For simplicity m_c is chosen as one and mv is chosen to be the value of m.

There are six sectors each for the VSI and VSR hexagons and hence thirty six operating modes are possible. Consider the instant when the first 60 degree segment for both the output voltage and input current are active. Then using equation 9.27 and 9.36, the following expression for LF transfer matrix is obtained:

$$[TphL] = m * \begin{bmatrix} \cos(\theta_{inv} - 30°) \\ -\sin(60° - \theta_{inv}) \\ -\sin(\theta_{inv}) \end{bmatrix} * \begin{bmatrix} \cos(\theta_{rect} - 30°) \\ -\sin(60° - \theta_{rect}) \\ -\sin(\theta_{rect}) \end{bmatrix}^T \qquad (9.40)$$

where $m = m_v*m_c$. Using equations 9.26 and 9.35 in equation 9.3, we have the following:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} d_\mu + d_\lambda \\ -d_\mu \\ -d_\lambda \end{bmatrix} * \begin{bmatrix} d_\alpha + d_\beta \\ -d_\alpha \\ -d_\beta \end{bmatrix}^T * \begin{bmatrix} v_{AO} \\ v_{BO} \\ v_{CO} \end{bmatrix} \qquad (9.41)$$

Equation 9.41 simplifies to the following:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} (d_{\alpha\mu} + d_{\alpha\lambda}) & (d_{\beta\mu} + d_{\beta\lambda}) \\ -d_{\alpha\mu} & -d_{\beta\mu} \\ -d_{\alpha\lambda} & -d_{\beta\lambda} \end{bmatrix} * \begin{bmatrix} v_{AB} \\ v_{AC} \end{bmatrix} \qquad (9.42)$$

where

$$v_{AB} = v_{AO} - v_{BO} \qquad (9.43)$$

$$v_{AC} = v_{AO} - v_{CO} \qquad (9.44)$$

$$d_{\alpha\mu} = d_\alpha * d_\mu = m * \sin\left(\frac{\pi}{3} - \theta_{rect}\right) * \sin\left(\frac{\pi}{3} - \theta_{inv}\right) = \frac{T_{\alpha\mu}}{T_S} \qquad (9.45)$$

$$d_{\alpha\lambda} = d_\alpha * d_\lambda = m * \sin\left(\frac{\pi}{3} - \theta_{rect}\right) * \sin(\theta_{inv}) = \frac{T_{\alpha\lambda}}{T_S} \qquad (9.46)$$

$$d_{\beta\mu} = d_\beta * d_\mu = m * \sin(\theta_{rect}) * \sin\left(\frac{\pi}{3} - \theta_{inv}\right) = \frac{T_{\beta\mu}}{T_S} \qquad (9.47)$$

$$d_{\beta\lambda} = d_\beta * d_\lambda = m * \sin(\theta_{rect}) * \sin(\theta_{inv}) = \frac{T_{\beta\lambda}}{T_S} \qquad (9.48)$$

The derivation equation 9.42 is given in A9.4Appendix. From equation 9.42, it is clear that the standard output voltage and input current SVM can be implemented in two VSI sub topologies. When the VSI SVM sub topology corresponds to v_{pn} = V_{dc} = v_{AB}, then the two duty-cycles of the two adjacent voltage vectors are $d_{\alpha\mu}$ and $d_{\alpha\lambda}$. When the VSI SVM sub topology corresponds to vpn =

Vdc = vac, then the two duty-cycles of the adjacent output voltage vectors are $d_{\beta\mu}$ and $d_{\beta\lambda}$. During the remaining part of the switching period, the output line voltage is zero and the duty-cycle corresponds to the following:

$$d_0 = 1 - d_{\alpha\mu} - d_{\alpha\lambda} - d_{\beta\mu} - d_{\beta\lambda} = \frac{T_o}{T_S} \qquad (9.49)$$

Finally it is the selection of the zero switching state vector from Group III of Table 3.1 of Chapter III and the order of arrangement of the five switching state vectors (SSVs). The pattern followed for arrangement of the state switching vectors is : $d_{\alpha\mu} \rightarrow d_{\beta\mu} \rightarrow d_{\beta\lambda} \rightarrow d_{\alpha\lambda} \rightarrow d_0$. The optimum zero switching state vector is used for each of the thirty six switching combinations.

The thirty six switching combinations are tabulated as shown in Table 9.1 to Table 9.6, each with six sub tables. In Table 9.1 to 9.6, S_I and S_V corresponds to the input current and output voltage hexagon sector number. Also in Table 9.1 to 9.6, serial number 1 to 5 corresponds to the timing $T_{\alpha\mu} \rightarrow T_{\beta\mu} \rightarrow T_{\beta\lambda} \rightarrow T_{\alpha\lambda} \rightarrow T_0$. Also it is seen from Table 9.1 to 9.6 that with reference to VSI output voltage switching combination, there are eighteen pair of identical sub tables. If output voltage vol and input current iph are both in the first sector of respective hexagon, then referring Fig. 9.3, 9.4 , 9.7 and 9.8, the SSV pair using the above duty-cycle sequence will be I6-V6, I1-V6, I1-V1, I6-V1 and Io-Vo. Similar procedure is used to complete all the sector combinations of the output voltage and input current. Corresponding to I6-V6 SSV pair, from Fig. 9.7 and 9.8, p =A and n=B. From Fig. 9.3 and 9.4, p=a, n=b and p=c. As p and n correspond to input phase A and B, it follows that the output voltage VSI switching combination is A, B, A which has an ON duration ($d_{\alpha\mu} * Ts$). Table 9.1 to 9.6 shows the ON duration for all the thirty six switching combinations. The method of completing Table 9.1 to 9.6 is shown in A9.5 Appendix.

9.4 MODEL OF INDIRECT SPACE VECTOR MODULATED THREE PHASE MATRIX CONVERTER: The model of the three phase AC to three phase AC Indirect SVM MC was developed in SIMULINK [51]. This model is shown in Fig. 9.9. The individual subsystems are explained below:

The power circuit of the model is shown in in Fig. 9.9. This is developed using the SimPowerSystems blockset in SIMULINK [51]. This mainly consists of three phase AC source, bidirectional switch matrix, output filter and R-L load. The arrangement of the bidirectional switch matrix using IGBTs is shown in Fig. 3.2 of chapter III.

The modulation algorithm is developed in several sub units using Embedded MATLAB Function, MATLAB Function, Math Function, Logical and Bit Operator and using Sources block set in SIMULINK [51]. The various sub units are explained below:

9.4.1 DUTY-CYCLE SEQUENCE AND SECTOR SWITCH FUNCTION GENERATOR: This is developed using Embedded Matlab Function block in SIMULINK, as shown in Fig. 9.9. With peak

TABLE 9.1

SI=I & Sv=I (A)									SI=I & Sv=II (B)									SI=I & Sv=III (C)								
Sl.No	SSV Pair	Switching Combinations							Sl.No	SSV Pair	Switching Combinations							Sl.No	SSV Pair	Switching Combinations						
		p	n	a	b	c					p	n	a	b	c					p	n	a	b	c		
1	I6-V6	A	B	A	B	A			1	I6-V1	A	B	A	B	B			1	I6-V2	A	B	A	A	B		
2	I1-V6	A	C	A	C	A			2	I1-V1	A	C	A	C	C			2	I1-V2	A	C	A	A	C		
3	I1-V1	A	C	A	C	C			3	I1-V2	A	C	A	A	C			3	I1-V3	A	C	C	A	C		
4	I6-V1	A	B	A	B	B			4	I6-V2	A	B	A	A	B			4	I6-V3	A	B	B	A	B		
5	Io-Vo	A	A	A	A	A			5	Io-Vo	A	A	A	A	A			5	Io-Vo	A	A	A	A	A		

TABLE 9.1 (Continued)

SI=I & Sv=IV (D)									SI=I & Sv=V (E)									SI=I & Sv=VI (F)								
Sl.No	SSV Pair	Switching Combinations							Sl.No	SSV Pair	Switching Combinations							Sl.No	SSV Pair	Switching Combinations						
		p	n	a	b	c					p	n	a	b	c					p	n	a	b	c		
1	I6-V3	A	B	B	A	B			1	I6-V4	A	B	B	A	A			1	I6-V5	A	B	B	B	A		
2	I1-V3	A	C	C	A	C			2	I1-V4	A	C	C	A	A			2	I1-V5	A	C	C	C	A		
3	I1-V4	A	C	C	A	A			3	I1-V5	A	C	C	C	A			3	I1-V6	A	C	A	C	A		
4	I6-V4	A	B	B	A	A			4	I6-V5	A	B	B	B	A			4	I6-V6	A	B	A	B	A		
5	Io-Vo	A	A	A	A	A			5	Io-Vo	A	A	A	A	A			5	Io-Vo	A	A	A	A	A		

TABLE 9.2

SI=IV& Sv=I (A)									SI=IV & Sv=II (B)									SI=IV & Sv=III (C)								
Sl.No	SSV Pair	Switching Combinations							Sl.No	SSV Pair	Switching Combinations							Sl.No	SSV Pair	Switching Combinations						
		p	n	a	b	c					p	n	a	b	c					p	n	a	b	c		
1	I3-V6	B	A	B	A	B			1	I3-V1	B	A	B	A	A			1	I3-V2	B	A	B	B	A		
2	I4-V6	C	A	C	A	C			2	I4-V1	C	A	C	A	A			2	I4-V2	C	A	C	C	A		
3	I4-V1	C	A	C	A	A			3	I4-V2	C	A	C	C	A			3	I4-V3	C	A	A	C	A		
4	I3-V1	B	A	B	A	A			4	I3-V2	B	A	B	B	A			4	I3-V3	B	A	A	B	A		
5	Io-Vo	A	A	A	A	A			5	Io-Vo	A	A	A	A	A			5	Io-Vo	A	A	A	A	A		

TABLE 9.2 (Contiued)

SI=IV& Sv=IV (D)									SI=IV & Sv=V (E)									SI=IV & Sv=VI (F)								
Sl.No	SSV Pair	Switching Combinations							Sl.No	SSV Pair	Switching Combinations							Sl.No	SSV Pair	Switching Combinations						
		p	n	a	b	c					p	n	a	b	c					p	n	a	b	c		
1	I3-V3	B	A	A	B	A			1	I3-V4	B	A	A	B	B			1	I3-V5	B	A	A	A	B		
2	I4-V3	C	A	A	C	A			2	I4-V4	C	A	A	C	C			2	I4-V5	C	A	A	A	C		
3	I4-V4	C	A	A	C	C			3	I4-V5	C	A	A	A	C			3	I4-V6	C	A	C	A	C		
4	I3-V4	B	A	A	B	B			4	I3-V5	B	A	A	A	B			4	I3-V6	B	A	B	A	B		
5	Io-Vo	A	A	A	A	A			5	Io-Vo	A	A	A	A	A			5	Io-Vo	A	A	A	A	A		

TABLE 9.3

SI=II& Sv=I (A)									SI=II & Sv=II (B)									SI=II & Sv=III (C)								
Sl.No	SSV Pair	Switching Combinations							Sl.No	SSV Pair	Switching Combinations							Sl.No	SSV Pair	Switching Combinations						
		p	n	a	b	c					p	n	a	b	c					p	n	a	b	c		
1	I1-V6	A	C	A	C	A			1	I1-V1	A	C	A	C	C			1	I1-V2	A	C	A	A	C		
2	I2-V6	B	C	B	C	B			2	I2-V1	B	C	B	C	C			2	I2-V2	B	C	B	B	C		
3	I2-V1	B	C	B	C	C			3	I2-V2	B	C	B	B	C			3	I2-V3	B	C	C	B	C		
4	I1-V1	A	C	A	C	C			4	I1-V2	A	C	A	A	C			4	I1-V3	A	C	C	A	C		
5	Io-Vo	C	C	C	C	C			5	Io-Vo	C	C	C	C	C			5	Io-Vo	C	C	C	C	C		

TABLE 9.3 (Continued)

SI=II& Sv=IV (D)									SI=II & Sv=V (E)									SI=II & Sv=VI (F)								
Sl.No	SSV Pair	Switching Combinations							Sl.No	SSV Pair	Switching Combinations							Sl.No	SSV Pair	Switching Combinations						
		p	n	a	b	c					p	n	a	b	c					p	n	a	b	c		
1	I1-V3	A	C	C	A	C			1	I1-V4	A	C	C	A	A			1	I1-V5	A	C	C	C	A		
2	I2-V3	B	C	C	B	C			2	I2-V4	B	C	C	B	B			2	I2-V5	B	C	C	C	B		
3	I2-V4	B	C	C	B	B			3	I2-V5	B	C	C	C	B			3	I2-V6	B	C	B	C	B		
4	I1-V4	A	C	C	A	A			4	I1-V5	A	C	C	C	A			4	I1-V6	A	C	A	C	A		
5	Io-Vo	C	C	C	C	C			5	Io-Vo	C	C	C	C	C			5	Io-Vo	C	C	C	C	C		

TABLE 9.4

SI=V& Sv=I (A)									SI=V & Sv=II (B)									SI=V & Sv=III (C)								
Sl.No	SSV Pair	Switching Combinations							Sl.No	SSV Pair	Switching Combinations							Sl.No	SSV Pair	Switching Combinations						
		p	n	a	b	c					p	n	a	b	c					p	n	a	b	c		
1	I4-V6	C	A	C	A	C			1	I4-V1	C	A	C	A	A			1	I4-V2	C	A	C	C	A		
2	I5-V6	C	B	C	B	C			2	I5-V1	C	B	C	B	B			2	I5-V2	C	B	C	C	B		
3	I5-V1	C	B	C	B	B			3	I5-V2	C	B	C	C	B			3	I5-V3	C	B	B	C	B		

4	I4-V1	C A C A A	4	I4-V2	C A C C A	4	I4-V3	C A A C A
5	Io-Vo	C C C C C	5	Io-Vo	C C C C C	5	Io-Vo	C C C C C

TABLE 9.4 (Continued)

SI=V& Sv=IV (D)			SI=V & Sv=V (E)			SI=V & Sv=VI (F)		
Sl.No	SSV Pair	Switching Combinations p n a b c	Sl.No	SSV Pair	Switching Combinations p n a b c	Sl.No	SSV Pair	Switching Combinations p n a b c
1	I4-V3	C A A C A	1	I4-V4	C A A C C	1	I4-V5	C A A A C
2	I5-V3	C B B C B	2	I5-V4	C B B C C	2	I5-V5	C B B B C
3	I5-V4	C B B C C	3	I5-V5	C B B B C	3	I5-V6	C B C B C
4	I4-V4	C A A C C	4	I4-V5	C A A A C	4	I4-V6	C A C A C
5	Io-Vo	C C C C C	5	Io-Vo	C C C C C	5	Io-Vo	C C C C C

TABLE 9.5

SI=III& Sv=I (A)			SI=III & Sv=II (B)			SI=III & Sv=III (C)		
Sl.No	SSV Pair	Switching Combinations p n a b c	Sl.No	SSV Pair	Switching Combinations p n a b c	Sl.No	SSV Pair	Switching Combinations p n a b c
1	I2-V6	B C B C B	1	I2-V1	B C B C C	1	I2-V2	B C B B C
2	I3-V6	B A B A B	2	I3-V1	B A B A A	2	I3-V2	B A B B A
3	I3-V1	B A B A A	3	I3-V2	B A B B A	3	I3-V3	B A A B A
4	I2-V1	B C B C C	4	I2-V2	B C B B C	4	I2-V3	B C C B C
5	Io-Vo	B B B B B	5	Io-Vo	B B B B B	5	Io-Vo	B B B B B

TABLE V9.5(Continued)

SI=III& Sv=IV (D)			SI=III & Sv=V (E)			SI=III & Sv=VI (F)		
Sl.No	SSV Pair	Switching Combinations p n a b c	Sl.No	SSV Pair	Switching Combinations p n a b c	Sl.No	SSV Pair	Switching Combinations p n a b c
1	I2-V3	B C C B C	1	I2-V4	B C C B B	1	I2-V5	B C C C B
2	I3-V3	B A A B A	2	I3-V4	B A A B B	2	I3-V5	B A A A B
3	I3-V4	B A A B B	3	I3-V5	B A A A B	3	I3-V6	B A B A B
4	I2-V4	B C C B B	4	I2-V5	B C C C B	4	I2-V6	B C B C B
5	Io-Vo	B B B B B	5	Io-Vo	B B B B B	5	Io-Vo	B B B B B

TABLE 9.6

SI=VI& Sv=I (A)			SI=VI & Sv=II (B)			SI=VI & Sv=III (C)		
Sl.No	SSV Pair	Switching Combinations p n a b c	Sl.No	SSV Pair	Switching Combinations p n a b c	Sl.No	SSV Pair	Switching Combinations p n a b c
1	I5-V6	C B C B C	1	I5-V1	C B C B B	1	I5-V2	C B C C B
2	I6-V6	A B A B A	2	I6-V1	A B A B B	2	I6-V2	A B A A B
3	I6-V1	A B A B B	3	I6-V2	A B A A B	3	I6-V3	A B B A B
4	I5-V1	C B C B B	4	I5-V2	C B C C B	4	I5-V3	C B B C B
5	Io-Vo	B B B B B	5	Io-Vo	B B B B B	5	Io-Vo	B B B B B

TABLE 9.6 (Continued)

SI=VI& Sv=IV (D)			SI=VI & Sv=V (E)			SI=VI & Sv=VI (F)		
Sl.No	SSV Pair	Switching Combinations p n a b c	Sl.No	SSV Pair	Switching Combinations p n a b c	Sl.No	SSV Pair	Switching Combinations p n a b c
1	I5-V3	C B B C B	1	I5-V4	C B B C C	1	I5-V5	C B B B C
2	I6-V3	A B B A B	2	I6-V4	A B B A A	2	I6-V5	A B B B A
3	I6-V4	A B B A A	3	I6-V5	A B B B A	3	I6-V6	A B A B A
4	I5-V4	C B B C C	4	I5-V5	C B B B C	4	I5-V6	C B C B C
5	Io-Vo	B B B B B	5	Io-Vo	B B B B B	5	Io-Vo	B B B B B

Table 9.1 to 9.6: PH3 AC to PH3 AC ISVM MC – Switching Sequence Table

line to neutral input voltage, desired peak output phase voltage, input frequency, output frequency, time, angular frequency of reference frame ωc as input parameters, the three phase output voltage can be resolved into dq-axis component voltages [42] and the absolute value of the angle of the output phase voltage, vout_angle can be calculated using the function atan2(voq,vod). Using input voltage and input phase displacement angle, a similar procedure is used to calculate the absolute value of the input current angle, i_in_angle. The value of reference frame frequency ωc is zero. This is illustrated in Program segment I in section 8.3.1 of chapter VIII. These two values of the angles are used to calculate the output voltage sector SV, input current sector SI using MATLAB function and theta_inv

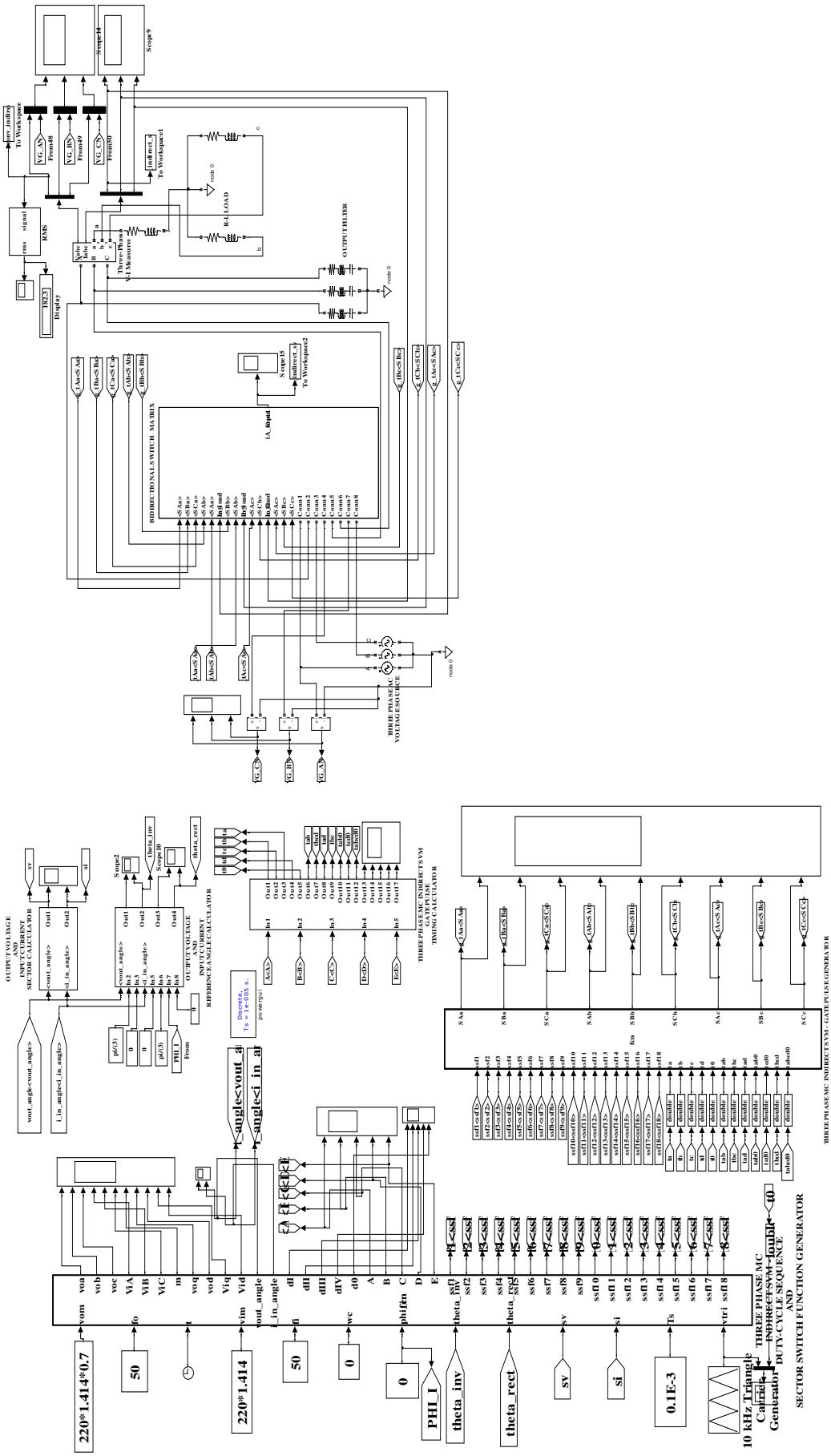
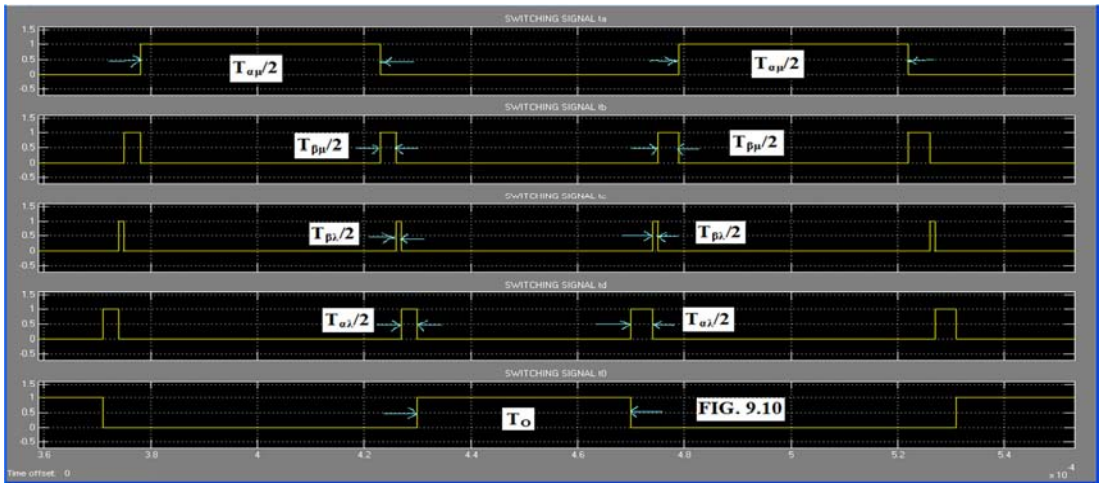


FIG. 9.9: THREE PHASE AC TO THREE PHASE AC INDIRECT SPACE VECTOR MODULATED MATRIX CONVERTER

and theta_rect using the REM and SUBTRACT modules. Program Segment II illustrates part of the MATLAB code for duty cycle sequencing and sector switch function generation. Duty-cycle dI, dII, dIII, dIV and d0 are calculated using equations 9.45, 9.47, 9.48, 9.46 and 9.49 respectively, assuming unity input power factor. This is used to calculate the timing A, B, C, D and E by comparison of the cumulative sector timing with a triangle carrier as shown in Program Segment II. This triangle carrier has a period Ts, peak value Ts/2 Volts and minimum value zero, as shown in Fig.8.4 of chapter VIII. The PWM signal timing is shown in Fig. 9.10. Cumulative sector timing is obtained by appropriately adding the value of duty-ratios and multiplying by $T_S/2$, as shown in Program Segment II. Sector switch functions ssf1 to ssf18 are determined using if-then-else statement. For example sector switch function ssf1 is HIGH only when sv = si =1 or sv = si = 4 and is LOW otherwise.

```
%%PROGRAM SEGMENT  II
%%Narayanaswamy. P.R. Iyer
Function [m,dI,dII,dIII,dIV,d0,A,B,C,D,E,ssf1,ssf2,ssf3,ssf4,ssf5,ssf6,ssf7,ssf8,ssf9,ssf10,ssf11,ssf12,ssf13,ssf14,ssf15,
ssf16,ssf17, ssf18] = fcn(vom,fo,t,vim,fi,wc,phi_i,theta_inv,theta_rect,sv,si,Ts,vtri)
m = vo/vim;
dI = (m*sin(pi/(3)-theta_rect)*sin(pi/(3)-theta_inv));%%d_alfa_meu
dII = (m*sin(theta_rect)*sin(pi/(3)-theta_inv));%%d_beta_meu
dIII = (m*sin(theta_rect)*sin(theta_inv));%%d_beta_lamda
dIV = (m*sin(pi/(3)-theta_rect)*sin(theta_inv));%%d_alfa_lamda
d0 = (1 - dI - dII - dIII - dIV);
if ( vtri <= dI*Ts/(2))
A = 1;    else
 A = 0;
 end
if ( vtri <= (dII + dI)*Ts/(2))
B = 1;    else
B = 0;
end
if ( vtri <= (dIII + dII + dI)*Ts/(2))
C = 1;   else
C = 0;
end
if ( vtri <= (dIV + dIII + dII + dI)*Ts/(2))
D = 1;  else
D = 0;
end
if ( vtri <= (dIV + dIII + dII + dI + d0)*Ts/(2))
E = 1;  else
E = 0;
end
if (sv == 1 && si == 1 || sv == 4 && si == 4)
    %%sector 1. sector switch function ssf1.
    ssf1 = 1;
else
    ssf1 = 0;
end
if ( sv == 2 && si == 1  ||  sv == 5 && si == 4 )
    %%sector 2. sector switch function ssf2.
    ssf2 = 1;
else
    ssf2 = 0;
end
%%Similar statement for ssf3 to ssf18.
.
.
.
if ( sv == 6 && si == 3  ||  sv == 3 && si == 6 )
   %%sector 18. sector switch function ssf18.
    ssf18 = 1;
else
    ssf18 = 0;
end
```

9.4.2 OUTPUT VOLTAGE AND INPUT CURRENT SECTOR CALCULATOR: This is developed using MATLAB Function, a mux and a demux as shown in Fig. 8.5 of chapter VIII. The



input to the mux are vout_angle and i_in_angle. The output from the demux are SV and SI. The source code to determine SV and SI is shown in Program Segment III in section 8.3.1 of chapter VIII.

9.4.3 OUTPUT VOLTAGE AND INPUT CURRENT REFERENCE ANGLE CALCULATOR: This is shown in Fig. 9.11. This uses two REM function blocks and SUBTRACT modules. The first REM block has the inputs v_out_angle and pi/(3). The output of the first REM block gives θinv defined in Fig. 9.4. The second REM block has the inputs i_in_angle and pi/(3). The output of the second REM block is subtracted from input p.f. angle φi to obtain θrect defined in Fig. 9.8.

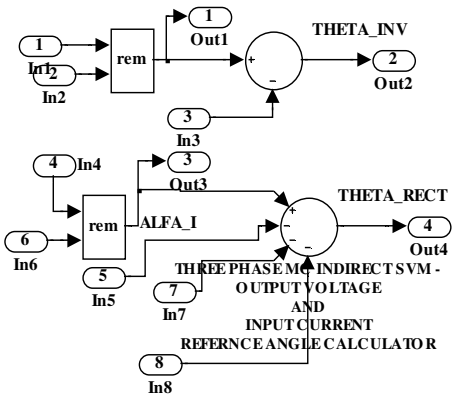


Fig. 9.11

9.4.4 GATE PULSE TIMING CALCULATOR: This is shown in Fig. 9.12. The inputs in1 to in5 are A, B, C, D and E respectively. The individual gate pulse timing, ta, tb, tc, td and t0 are respectively dI*Ts/(2), dII*Ts/(2), dIII*Ts/(2), dIV*Ts/(2) and d0*Ts/(2) where each duty-cycle dI, dII, dIII, dIV and d0 respectively correspond to dαμ, $d_{\beta\mu}$, $d_{\beta\lambda}$, $d_{\alpha\lambda}$ and d_0 as defined in equations 9.45, 9.47, 9.48, 9.46 and 9.49. This individual gate pulse duration is obtained as shown in equation 9.50 below:

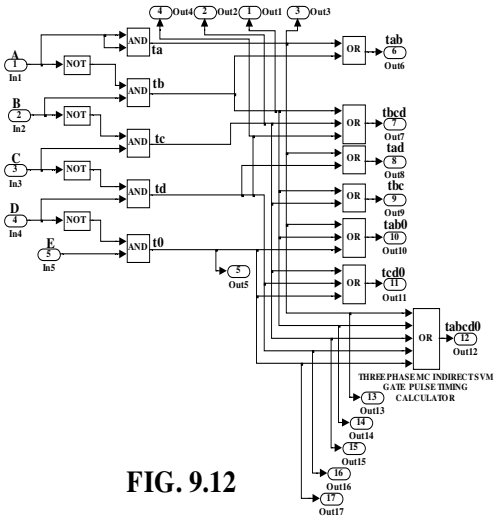


FIG. 9.12

$$t_a = (A \,\&\, A)$$

$$t_b = (\sim A \,\&\, B)$$

$$t_c = (\sim B \,\&\, C)$$
$$t_d = (\sim C \,\&\, D)$$
$$t_0 = (\sim D \,\&\, E) \ldots \qquad (9.50)$$

In equation 9.50, symbols (&) represents logical AND and (~) represents NOT operation respectively. To easily generate the MC gate pulse, the timing pulse in equation 9.50 are given to OR gates to obtain the following additional timing pulse:

$$t_{ab} = (t_a || t_b)$$
$$t_{bcd} = (t_b || t_c || t_d)$$
$$t_{ad} = (t_a || t_d)$$
$$t_{bc} = (t_b || t_c)$$
$$t_{ab0} = (t_a || t_b || t_0)$$
$$t_{cd0} = (t_c || t_d || t_0)$$
$$t_{abcd0} = (t_a || t_b || t_c || t_d || t_0) \ldots . . (9.51)$$

In equation 9.51, symbol (||) represents logical OR operation.

The complete gate timing for the nine bidirectional switches using Indirect SVM algorithm is given in Tables 9.7 and 9.8 below:

TABLE 9.7: Switching Pattern

Sl. No.	SI, SV	SSF_X HIGH	BIDIRECTIONAL SWITCH GATE PULSE PATTERN				
			ta	tb	tc	td	t0
1	I,I or IV,IV	ssf1	ABA	ACA	ACC	ABB	AAA
2	I,II or IV,V	ssf2	ABB	ACC	AAC	AAB	AAA
3	I,III or IV,VI	ssf3	AAB	AAC	CAC	BAB	AAA
4	I,IV or IV,I	ssf4	BAB	CAC	CAA	BAA	AAA
5	I,V or IV,II	ssf5	BAA	CAA	CCA	BBA	AAA
6	I,VI or IV,III	ssf6	BBA	CCA	ACA	ABA	AAA
7	II,I or V,IV	ssf7	ACA	BCB	BCC	ACC	CCC
8	II,II or V,V	ssf8	ACC	BCC	BBC	AAC	CCC
9	II,III or V,VI	ssf9	AAC	BBC	CBC	CAC	CCC
10	II,IV or V,I	ssf10	CAC	CBC	CBB	CAA	CCC
11	II,V or V,II	ssf11	CAA	CBB	CCB	CCA	CCC
12	II,VI or V,III	ssf12	CCA	CCB	BCB	ACA	CCC
13	III,I or VI,IV	ssf13	BCB	BAB	BAA	BCC	BBB
14	III,II or VI,V	ssf14	BCC	BAA	BBA	BBC	BBB
15	III,III or VI,VI	ssf15	BBC	BBA	ABA	CBC	BBB
16	III,IV or VI,I	ssf16	CBC	ABA	ABB	CBB	BBB
17	III,V or VI,II	ssf17	CBB	ABB	AAB	CCB	BBB
18	III,VI or VI,III	ssf18	CCB	AAB	BAB	BCB	BBB

9.4.5 GATE PULSE GENERATOR: The gate pulse generator for the MC is developed using Embedded MATLAB as shown in Fig. 9.9. The sector switch functions ssf1 to ssf18, gate pulse timing calculator outputs defined in equations 9.50 and 9.51 form the input modules and the outputs are the gate pulses for the nine bidirectional switches of the MC. In Table 9.8, the gate timing for the nine bidirectional switches are shown. The gate timing for switch SAa can be combined by logically ANDing the respective value with sector switch function ssf_x and ORing the value for each sector. Thus the gate timing pulse for switch SAa can be expressed as in equation 9.52 below:

$$SAa = ssf1\&(tabcd0) || ssf2\&(tabcd0) || \ldots || ssf18\&(tb) . . (9.52)$$

Program segment IV gives the method of generating the gate timing pulses for the nine bidirectional switches using the calculated sector timings given in Table 9.8.

TABLE 9.8: Gate Pulse Timing

Sl. No.	SI, SV	SSF_X HIGH	SAa	SBa	SCa	SAb	SBb	SCb	SAc	SBc	SCc
1	I,I or IV,IV	ssf1	tabcd0	0	0	t0	tad	tbc	tab0	td	tc
2	I,II or IV,V	ssf2	tabcd0	0	0	tcd0	ta	tb	t0	tad	tbc
3	I,III or IV,VI	ssf3	tab0	td	tc	tabcd0	0	0	t0	tad	tbc
4	I,IV or IV,I	ssf4	t0	tad	tbc	tabcd0	0	0	tcd0	ta	tb
5	I,V or IV,II	ssf5	t0	tad	tbc	tab0	td	tc	tabcd0	0	0
6	I,VI or IV,III	ssf6	tcd0	ta	tb	t0	tad	tbc	tabcd0	0	0
7	II,I or V,IV	ssf7	tad	tbc	t0	0	0	tabcd0	ta	tb	tcd0
8	II,II or V,V	ssf8	tad	tbc	t0	td	tc	tab0	0	0	tabcd0
9	II,III or V,VI	ssf9	ta	tb	tcd0	tad	tbc	t0	0	0	tabcd0
10	II,IV or V,I	ssf10	0	0	tabcd0	tad	tbc	t0	td	tc	tab0
11	II,V or V,II	ssf11	0	0	tabcd0	ta	tb	tcd0	tad	tbc	t0
12	II,VI or V,III	ssf12	td	tc	tab0	0	0	tabcd0	tad	tbc	t0
13	III,I or VI,IV	ssf13	0	tabcd0	0	tbc	t0	tad	tc	tab0	td
14	III,II or VI,V	ssf14	0	tabcd0	0	tb	tcd0	ta	tbc	t0	tad
15	III,III or VI,VI	ssf15	tc	tab0	td	0	tabcd0	0	tbc	t0	tad
16	III,IV or VI,I	ssf16	tbc	t0	tad	0	tabcd0	0	tb	tcd0	ta
17	III,V or VI,II	ssf17	tbc	t0	tad	tc	tab0	td	0	tabcd0	0
18	III,VI or VI,III	ssf18	tb	tcd0	ta	tbc	t0	tad	0	tabcd0	0

```
PROGRAM SEGMENT IV
function [SAa,SBa,SCa,SAb,SBb,SCb,SAc,SBc,SCc]  =
fcn(ssf1,ssf2,ssf3,ssf4,ssf5,ssf6,ssf7,ssf8,ssf9,ssf10,ssf11,ssf12,
ssf13,ssf14,ssf15,ssf16,ssf17,ssf18,ta,tb,tc,td,t0,tab,tbc,tad,tab0,tcd0,tbcd,tabcd0)
%%Narayanaswamy. P.R.Iyer
SAa =
ssf1&(tabcd0)||ssf2&(tabcd0)||ssf3&(tab0)||ssf4&(t0)||ssf5&(t0)||ssf6&(tcd0)||ssf7&(tad)||ssf8&(tad)||
ssf9&(ta)||ssf10&(0)||ssf11&(0)||ssf12&(td)||ssf13&(0)||ssf14&(0)||ssf15&(tc)||ssf16&(tbc)||ssf17&(tbc)||
ssf18&(tb);
SBa =
ssf1&(0)||ssf2&(0)||ssf3&(td)||ssf4&(tad)||ssf5&(tad)||ssf6&(ta)||ssf7&(tbc)||ssf8&(tbc)||ssf9&(tb)||ssf10&(0)||
ssf11&(0)||ssf12&(tc)||ssf13&(tabcd0)||ssf14&(tabcd0)||ssf15&(tab0)||ssf16&(t0)||   ssf17& (t0)||ssf18&(tcd0);
SCa =
ssf1&(0)||ssf2&(0)||ssf3&(tc)||ssf4&(tbc)||ssf5&(tbc)||ssf6&(tb)||ssf7&(t0)||ssf8&(t0)||ssf9&(tcd0)||
ssf10&(tabcd0)||ssf11&(tabcd0)|| ssf12&(tab0)||ssf13&(0)||ssf14&(0)||ssf15&(td)||ssf16&(tad)||
ssf17& (tad)||ssf18&(ta);
SAb =
ssf1&(t0)||ssf2&(tcd0)||ssf3&(tabcd0)||ssf4&(tabcd0)||ssf5&(tab0)||ssf6&(t0)||ssf7&(0)||ssf8&(td)||ssf9&(tad)||
ssf10&(tad)||ssf11&(ta) ||ssf12&(0)||ssf13&(tbc)||ssf14&(tb)||ssf15&(0)||ssf16&(0)||ssf17&(tc)||ssf18&(tbc);
SBb =
ssf1&(tad)||ssf2&(ta)||ssf3&(0)||ssf4&(0)||ssf5&(td)||ssf6&(tad)||ssf7&(0)||ssf8&(tc)||ssf9&(tbc)||ssf10&(tbc)||
ssf11&(tb)||ssf12&(0)||ssf13&(t0)||ssf14&(tcd0)||ssf15&(tabcd0)||ssf16&(tabcd0)||ssf17& (tab0)||ssf18&(t0);
SCb =
ssf1&(tbc)||ssf2&(tb)||ssf3&(0)||ssf4&(0)||ssf5&(tc)||ssf6&(tbc)||ssf7&(tabcd0)||ssf8&(tab0)||ssf9&(t0)||
ssf10&(t0)||ssf11&(tcd0)|| ssf12&(tabcd0)||ssf13&(tad)||ssf14&(ta)||ssf15&(0)||ssf16&(0)||
ssf17&(td)||ssf18&(tad);
SAc =
ssf1&(tab0)||ssf2&(t0)||ssf3&(t0)||ssf4&(tcd0)||ssf5&(tabcd0)||ssf6&(tabcd0)||ssf7&(ta)||ssf8&(0)||ssf9&(0)||
ssf10&(td)|| ssf11&(tad)|| ssf12&(tad)||ssf13&(tc)||ssf14&(tbc)||ssf15&(tbc)||ssf16&(tb)||ssf17&(0)||ssf18&(0);
SBc =
ssf1&(td)||ssf2&(tad)||ssf3&(tad)||ssf4&(ta)||ssf5&(0)||ssf6&(0)||ssf7&(tb)||ssf8&(0)||ssf9&(0)||ssf10&(tc)||
ssf11&(tbc)||ssf12&(tbc) ||ssf13&(tab0)||ssf14&(t0)||ssf15&(t0)||ssf16&(tcd0)|| ssf17&(tabcd0)||ssf18&(tabcd0);
SCc =
ssf1&(tc)||ssf2&(tbc)||ssf3&(tbc)||ssf4&(tb)||ssf5&(0)||ssf6&(0)||ssf7&(tcd0)||ssf8&(tabcd0)||ssf9&(tabcd0)||
ssf10&(tab0)||ssf11&(t0)||ssf12&(t0)||ssf13&(td)||ssf14&(tad)||ssf15&(tad)||ssf16&(ta)|| ssf17&(0)||ssf18&(0);
```

9.5 SIMULATION RESULTS: The simulation of the Three Phase ISVM MC was carried out in SIMULINK [51]. The parameters used for simulation are shown in Table 9.9. The ode15S(Stiff/NDF) solver was used. Simulation was carried out for two different output frequencies with all other parameters constant. The simulation results for the harmonic spectrum of line to neut-

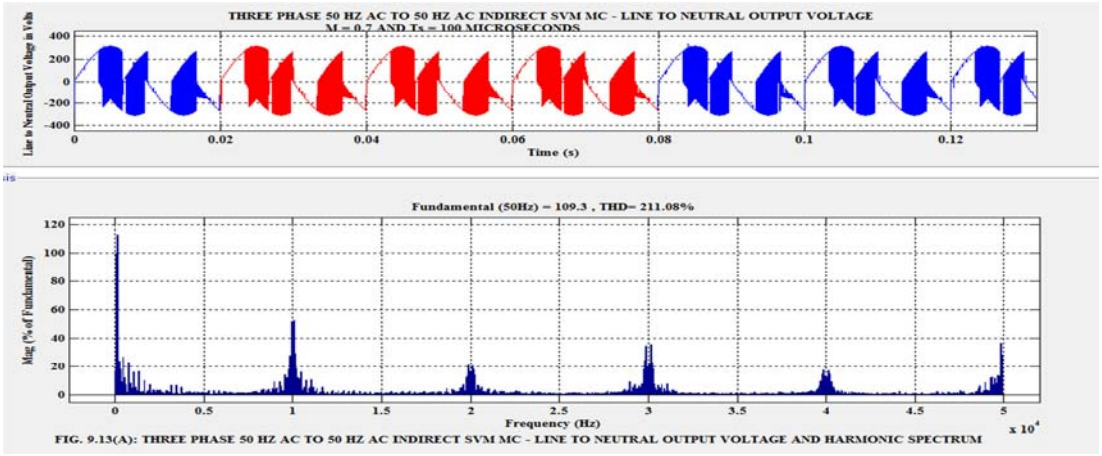


FIG. 9.13(A): THREE PHASE 50 HZ AC TO 50 HZ AC INDIRECT SVM MC - LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM

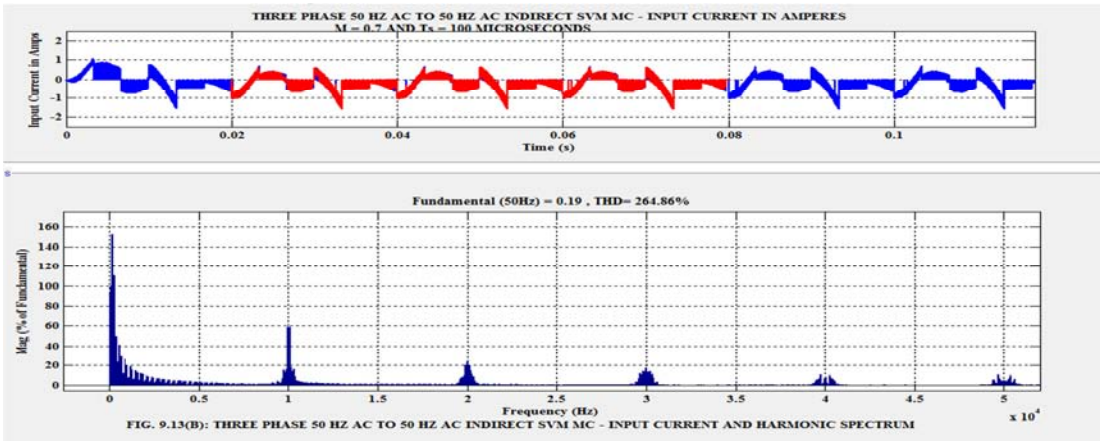


FIG. 9.13(B): THREE PHASE 50 HZ AC TO 50 HZ AC INDIRECT SVM MC - INPUT CURRENT AND HARMONIC SPECTRUM

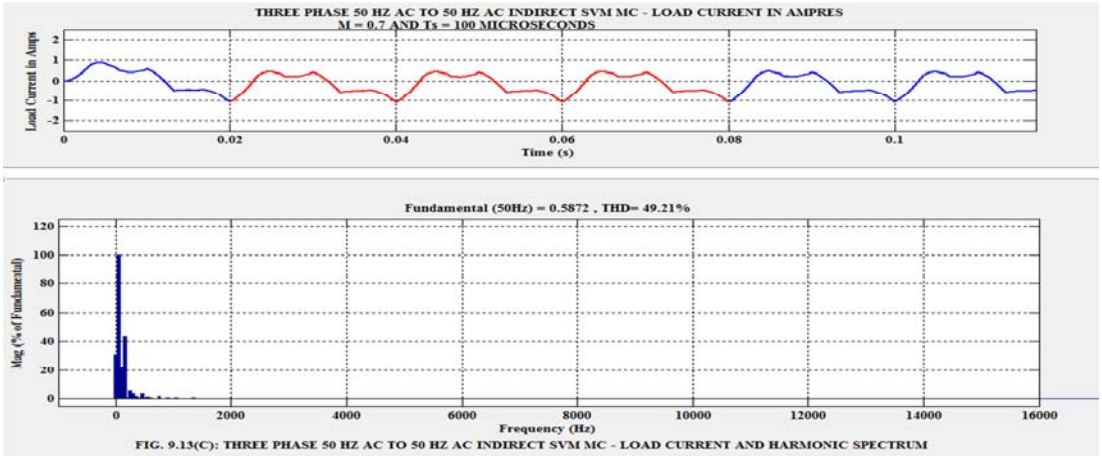


FIG. 9.13(C): THREE PHASE 50 HZ AC TO 50 HZ AC INDIRECT SVM MC - LOAD CURRENT AND HARMONIC SPECTRUM

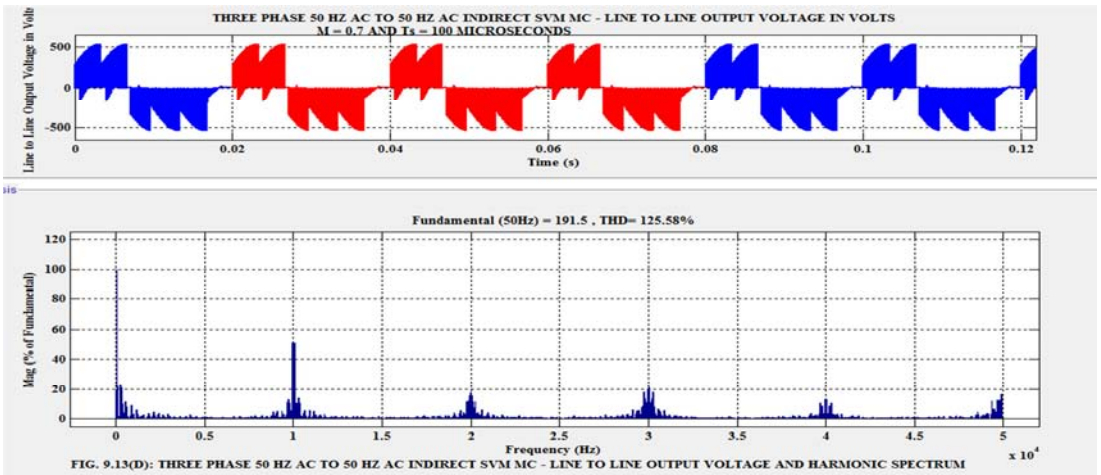
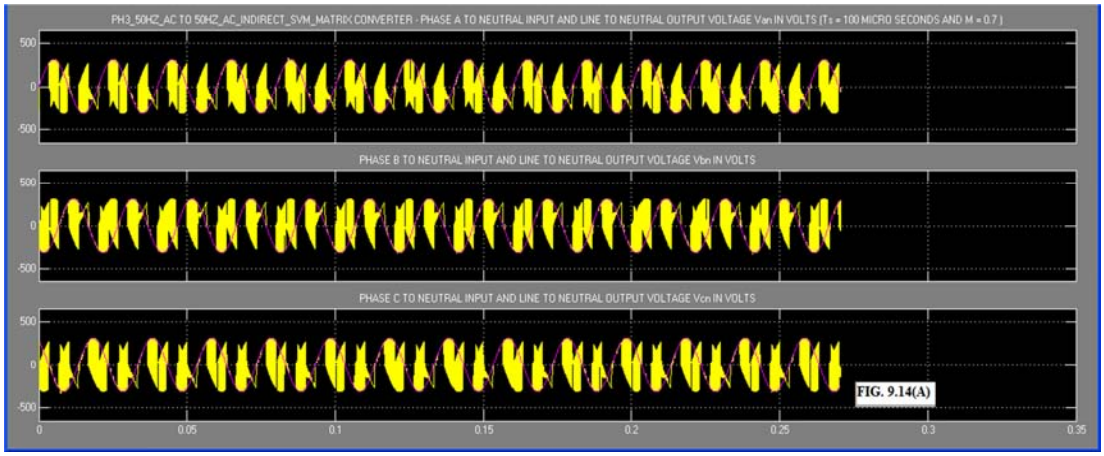
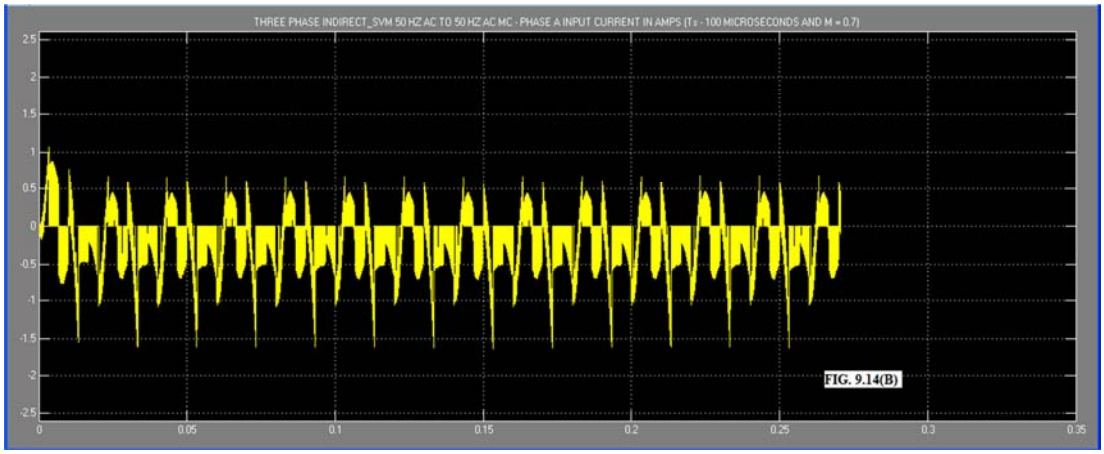
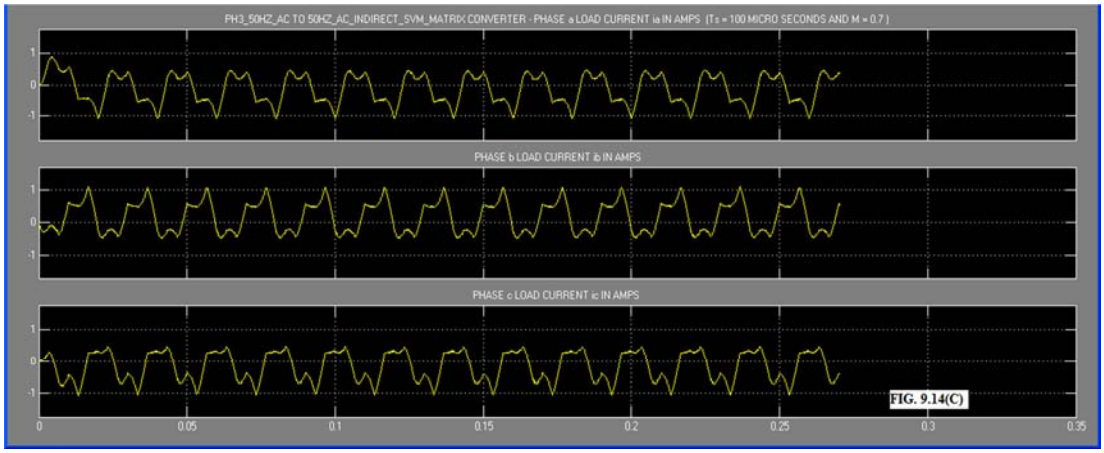
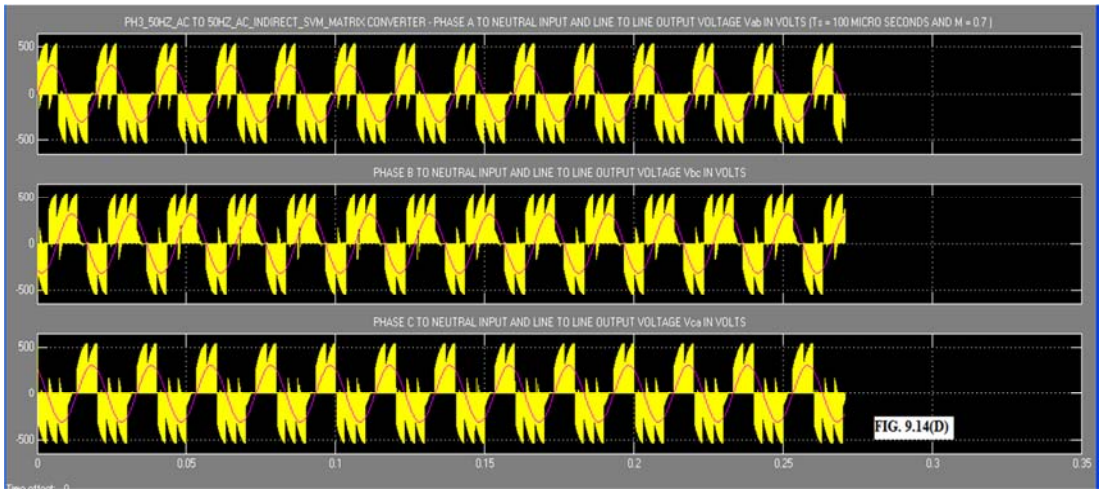


FIG. 9.13(D): THREE PHASE 50 HZ AC TO 50 HZ AC INDIRECT SVM MC - LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM


PH3_50HZ_AC TO 50HZ_AC_INDIRECT_SVM_MATRIX CONVERTER - PHASE A TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Van IN VOLTS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vbn IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vcn IN VOLTS
FIG. 9.14(A)


THREE PHASE INDIRECT_SVM 50 HZ AC TO 50 HZ AC MC - PHASE A INPUT CURRENT IN AMPS (Ts - 100 MICROSECONDS AND M = 0.7)
FIG. 9.14(B)


PH3_50HZ_AC TO 50HZ_AC_INDIRECT_SVM_MATRIX CONVERTER - PHASE a LOAD CURRENT ia IN AMPS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE b LOAD CURRENT ib IN AMPS
PHASE c LOAD CURRENT ic IN AMPS
FIG. 9.14(C)


PH3_50HZ_AC TO 50HZ_AC_INDIRECT_SVM_MATRIX CONVERTER - PHASE A TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vab IN VOLTS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vbc IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vca IN VOLTS
FIG. 9.14(D)

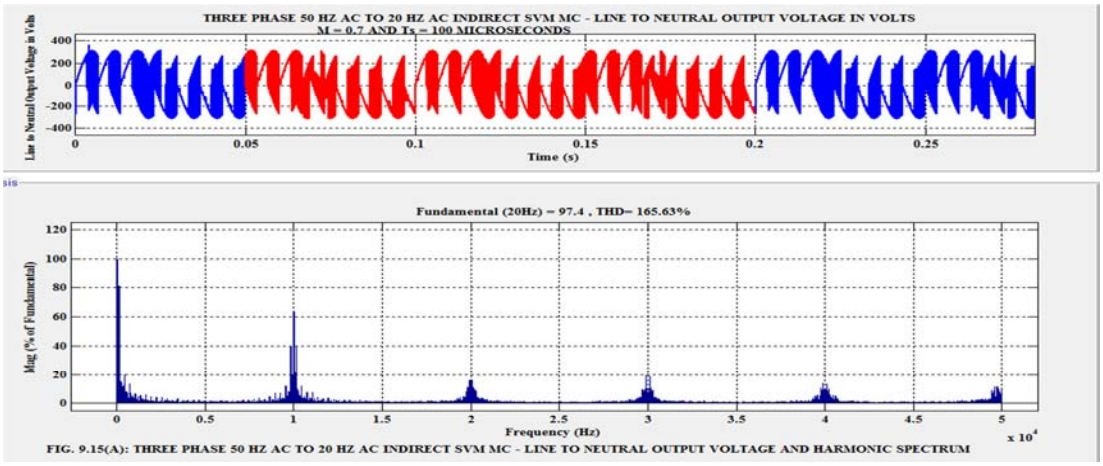


FIG. 9.15(A): THREE PHASE 50 HZ AC TO 20 HZ AC INDIRECT SVM MC - LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM

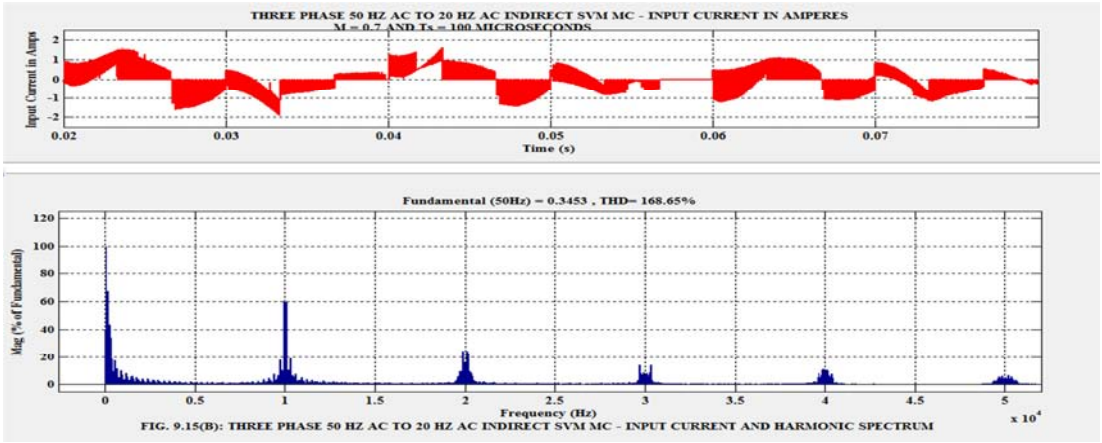


FIG. 9.15(B): THREE PHASE 50 HZ AC TO 20 HZ AC INDIRECT SVM MC - INPUT CURRENT AND HARMONIC SPECTRUM

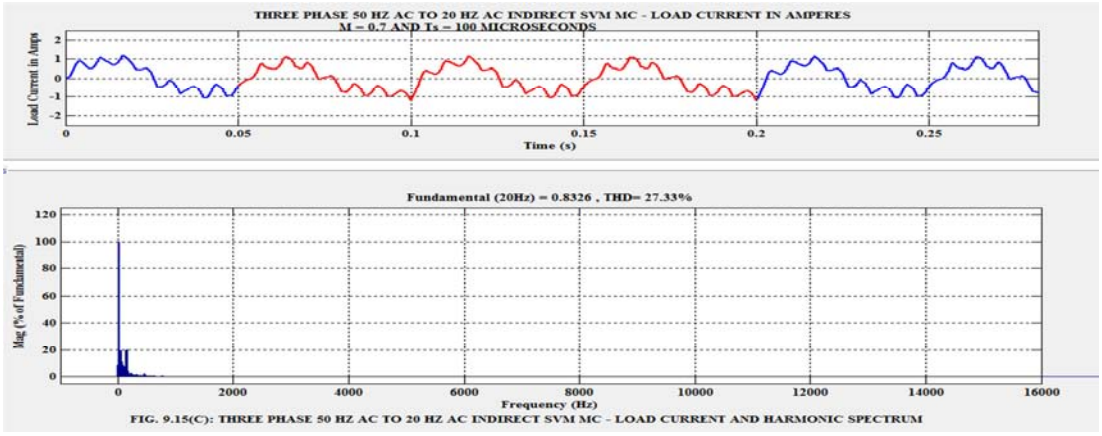


FIG. 9.15(C): THREE PHASE 50 HZ AC TO 20 HZ AC INDIRECT SVM MC - LOAD CURRENT AND HARMONIC SPECTRUM

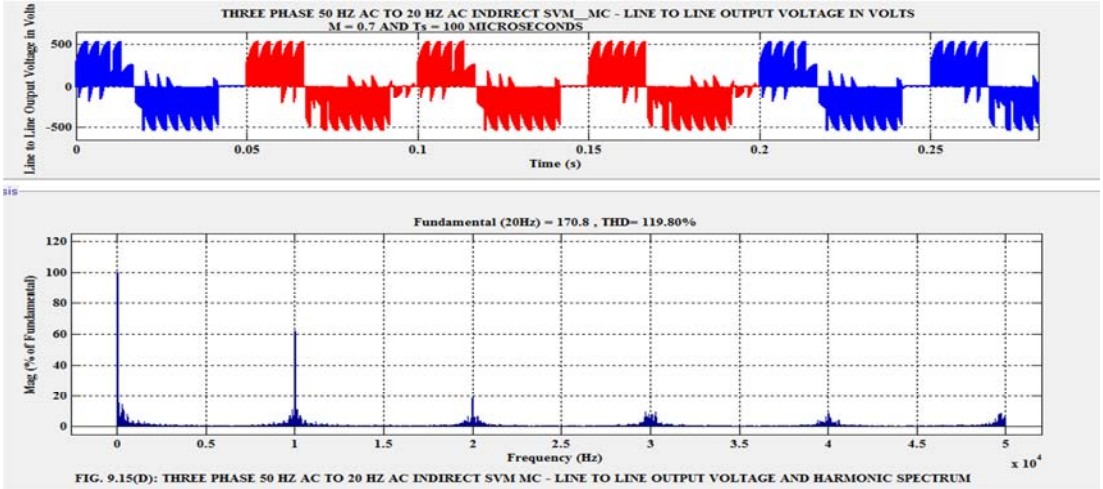
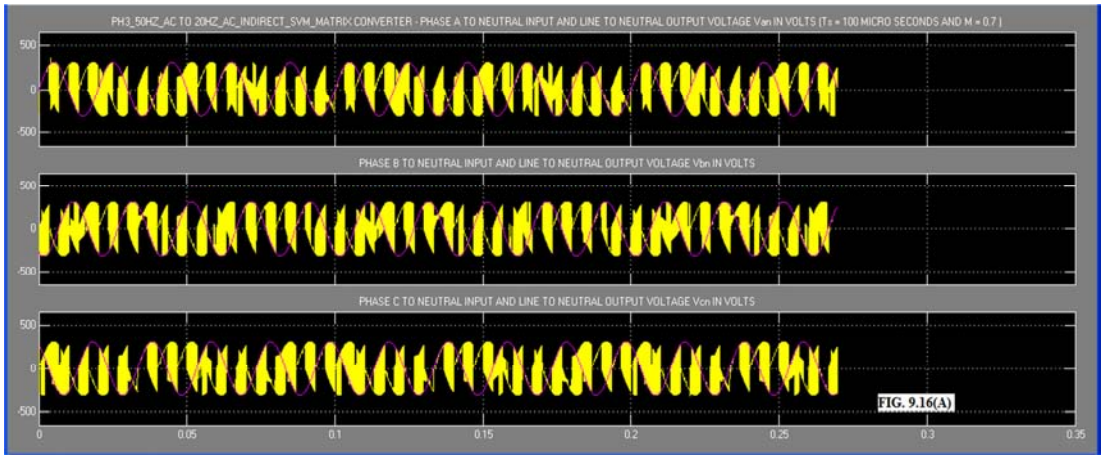
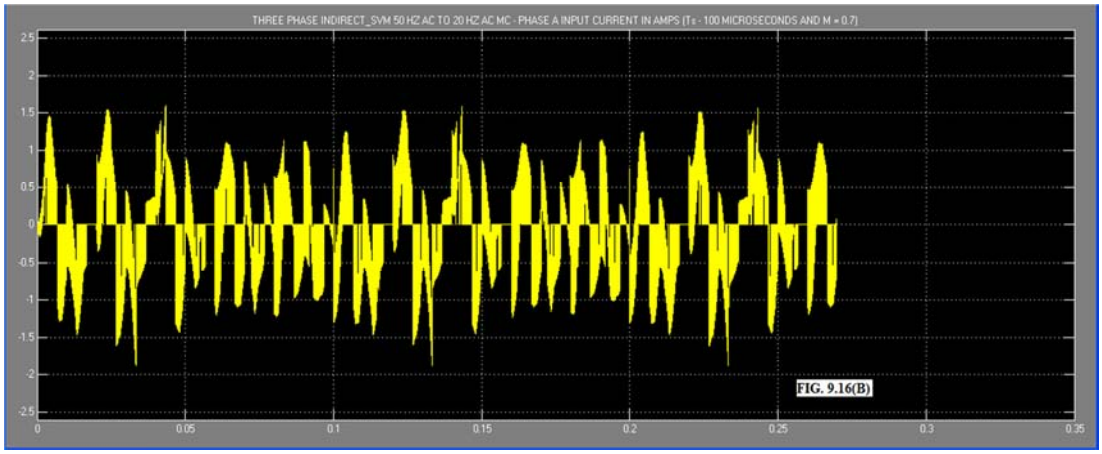
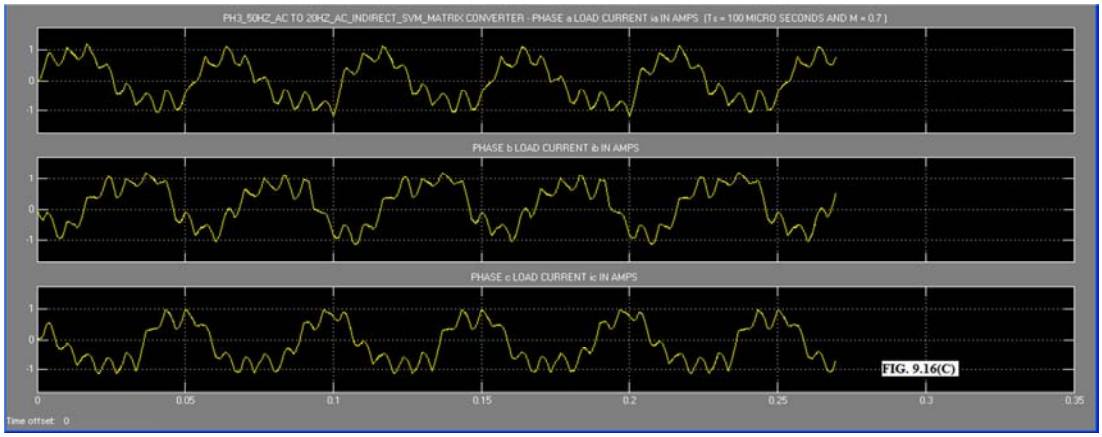


FIG. 9.15(D): THREE PHASE 50 HZ AC TO 20 HZ AC INDIRECT SVM MC - LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM


PH3_50HZ_AC TO 20HZ_AC_INDIRECT_SVM_MATRIX CONVERTER - PHASE A TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Van IN VOLTS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vbn IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vcn IN VOLTS
FIG. 9.16(A)


THREE PHASE INDIRECT_SVM 50 HZ AC TO 20 HZ AC MC - PHASE A INPUT CURRENT IN AMPS (Ts - 100 MICROSECONDS AND M = 0.7)
FIG. 9.16(B)


PH3_50HZ_AC TO 20HZ_AC_INDIRECT_SVM_MATRIX CONVERTER - PHASE a LOAD CURRENT ia IN AMPS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE b LOAD CURRENT ib IN AMPS
PHASE c LOAD CURRENT ic IN AMPS
FIG. 9.16(C)


PH3_50HZ_AC TO 20HZ_AC_INDIRECT_SVM_MATRIX CONVERTER - PHASE A TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vab IN VOLTS (Ts = 100 MICRO SECONDS AND M = 0.7)
PHASE B TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vbc IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vca IN VOLTS
FIG. 9.16(D)

TABLE 9.9: Model Parameters

Sl.No.	Parameter	Value	Unit
1	RMS Line to Neutral Input Voltage	220	V
2	Input Frequency fi	50	Hz
3	Modulation Index q	0.7	--
4	Output Frequency fo	50, 20	Hz
5	Carrier Sampling Frequency fsw	10	kHz
6	R-L-C Output Filter	10, 0.01e-3, 25.356e-6	Ω, H, F
7	R-L Load	100, 500e-3	Ω, H
8	Input Phase Displacement φi	0	Radians

ral output voltage, input current, load current and line to line output voltage for 50 Hz output frequency are shown in Fig. 9.13(A) to (D) and their respective oscilloscope waveforms are shown in Fig, 9.14(A) to (D) above. The same results in the above order for 20 Hz output frequency are shown in Fig. 9.15(A) to (D) and Fig. 9.16(A) to (D) above respectively. The simulation results are tabulated in Table 9.10 below:

TABLE 9.10: Simulation Results

Sl.No.	Three Phase Indirect SVM MC Input – Output Frequency Hz	THD of Line to Line Output Voltage p.u.	THD Of Line to Neutral Output Voltage p.u.	THD of Input Current p.u.	THD of Load Current p.u.
1)	50 – 50	1.2558	2.1108	2.6486	0.4921
2)	50 – 20	1.198	1.6563	1.6865	0.2733

9.6 DISCUSSION OF RESULTS: Indirect space vector modulation for three phase MC assumes the three phase MC to be considered equivalent to a three phase rectifier inverter converter and the SVM technique to be applied separately to the three phase rectifier and inverter and the combined duty-cycle timing for the MC is the product of the corresponding individual duty-cycle timing for the three phase rectifier and three phase inverter. It is also seen from Table 9.10 that as the output frequency is reduced, the THD of the line to neutral output voltage, line to line output voltages, input current and load current are reduced. The indirect SVM has eight commutations per carrier switching period. Also it is seen from the simulation results that the harmonic components of line to neutral output voltage, line to line output voltage, input current and load current tend to concentrate at integral multiples of carrier switching frequency.

9.7 CONCLUSIONS: This chapter presents an easy method of modeling a three phase Indirect SVM MC using Embedded MATLAB function, MATLAB function, Math blockset, Logic and Bit Operations toolbox and Sources block set. The input current, load current, Line to Neutral and Line to Line output voltage harmonic distortions are reduced with reduction in the output frequency. The three phase AC to three phase AC output voltage – input current SVM algorithm is systematically reviewed. A simple geometric presentation of the three phase AC to three phase AC MC SVM procedure is given. The indirect SVM algorithm uses eight commutations per carrier switching period. Harmonic components of line to neutral output voltage, line to line output voltage, input current and load current tend to concentrate at integral multiples of switching frequency. The model can be easily adapted for hardware implementation.

A9.1 APPENDIX: The matrix T_{phL} in equation 9.13 can be expressed as follows:

$$\left[\mathrm{T_{phL}}\right] = \mathrm{m} * \begin{bmatrix} \cos(\omega_o t - \varphi_o + 30°) \\ \cos(\omega_o t - \varphi_o + 30° - 120°) \\ \cos(\omega_o t - \varphi_o + 30° + 120°) \end{bmatrix}$$

$$* \left[\cos(\omega_i t - \varphi_i) \quad \cos(\omega_i t - \varphi_i - 120°) \quad \cos(\omega_i t - \varphi_i + 120°)\right] \qquad (A9.1.1)$$

$$Let\ (\omega_o . t - \varphi_o) = \alpha\ and\ (\omega_i . t - \varphi_i) = \beta \qquad (A9.1.2)$$

Simplifying using equations A9.1.1 and A9.1.2, we have the following equation:

$$\left[\mathrm{T_{phL}}\right] = \begin{bmatrix} \mathrm{m}.\cos(\alpha + 30°).\cos(\beta) & \mathrm{m}.\cos(\alpha + 30°).\cos(\beta - 120°) & \mathrm{m}.\cos(\alpha + 30°).\cos(\beta + 120°) \\ \mathrm{m}.\cos(\alpha - 90°).\cos(\beta) & \mathrm{m}.\cos(\alpha - 90°).\cos(\beta - 120°) & \mathrm{m}.\cos(\alpha - 90°).\cos(\beta + 120°) \\ \mathrm{m}.\cos(\alpha + 150°).\cos(\beta) & \mathrm{m}.\cos(\alpha + 150°).\cos(\beta - 120°) & \mathrm{m}.\cos(\alpha + 150°).\cos(\beta + 120°) \end{bmatrix} \qquad (A9.1.3)$$

Using equations 9.3, 9.11, 9.11 and A9.1.3, we have the following:

$$v_{ab} = \sqrt{3}.V_{om}.\cos(\alpha + 30°) = V_{im}.m.\cos(\alpha + 30°).\cos(\beta - 120°)$$

$$+ V_{im}.\mathrm{m}.\cos(\alpha + 30°°).\cos(\beta + 120° + \varphi_i).\cos(\beta + 120°) \qquad (A9.1..4)$$

i.e..$\sqrt{3}.V_{om}.\cos(\alpha + 30°) = V_{im}.m.\cos(\alpha + 30°) * [\cos(\varphi_i) * \{\cos^2(\beta) + \cos^2(\beta - 120°) + \cos^2(\beta + 120°)\} - \sin(\varphi_i) *$
$\{\sin(\beta).\cos(\beta) + \sin(\beta - 120°).\cos(\beta - 120°) + \sin(\beta + 120°).\cos(\beta + 120°)\}]$ $(A9.1.5)$

Simplifying equation A9.1.5, we have the following:

$$\sqrt{3}.V_{om}.\cos(\alpha + 30°) = \frac{3}{2}.V_{im}.m.\cos(\alpha + 30°).\cos(\varphi_i) \qquad (A9.1.6)$$

$$V_{om} = \frac{\sqrt{3}}{2}.V_{im}.m.\cos(\varphi_i) \qquad (A9.1.7)$$

A9.2 APPENDIX: In equation 9.15, let $(\omega_o t - \varphi_o - \varphi_L) = \gamma$ $(A9.2.1)$

$$i_{oL} = \frac{I_{om}}{\sqrt{3}} * \begin{bmatrix} \cos(\gamma + 30°) \\ \cos(\gamma - 90°) \\ \cos(\gamma + 150°) \end{bmatrix} \qquad (A9.2.2)$$

$$\left[T_{phL}\right]^T$$

$$= \begin{bmatrix} \mathrm{m}.\cos(\alpha + 30°).\cos(\beta) & \mathrm{m}.\cos(\alpha - 90°).\cos(\beta) & \mathrm{m}.\cos(\alpha + 150°).\cos(\beta) \\ \mathrm{m}.\cos(\alpha + 30°).\cos(\beta - 120°) & \mathrm{m}.\cos(\alpha - 90°).\cos(\beta - 120°) & \mathrm{m}.\cos(\alpha + 150°).\cos(\beta - 120°) \\ \mathrm{m}.\cos(\alpha + 30°).\cos(\beta + 120°) & \mathrm{m}.\cos(\alpha - 90°).\cos(\beta + 120°) & \mathrm{m}.\cos(\alpha + 150°).\cos(\beta + 120°) \end{bmatrix} \qquad (A9.2.3)$$

Using equation 9.4 and A9.2.3, we have the following:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \left[T_{phL}\right]^T * \frac{I_{om}}{\sqrt{3}} * \begin{bmatrix} \cos(\gamma + 30°) \\ \cos(\gamma - 90°) \\ \cos(\gamma + 150°) \end{bmatrix} \qquad (A9.2.4)$$

Simplifying for $\mathrm{i_a}$, we have the following:

$$i_a = m.\cos(\beta) * \frac{I_{om}}{\sqrt{3}} * [\{\cos(\alpha + 30°).\cos(\gamma + 30°)\} + \{\cos(\alpha - 90°).\cos(\gamma - 90°)\}$$

$$+ \{\cos(\alpha + 150°).\cos(\gamma + 150°)\}] \qquad (A9.2.5)$$

i.e..$i_a = m.\cos(\beta) * \frac{I_{om}}{\sqrt{3}} * \left[\frac{1}{2} * \cos(\alpha + \gamma + 60°) + \frac{1}{2} * \cos(\alpha - \gamma) + \frac{1}{2} * \cos(\alpha + \gamma - 180°) + \frac{1}{2} * \cos(\alpha - \gamma) + \frac{1}{2} *$
$\cos(\alpha + \gamma + 300°) + \frac{1}{2} * \cos(\alpha - \gamma)\right]$ $(A9.2.6)$

simplifying, $i_a = \frac{I_{om}}{\sqrt{3}} * \frac{3}{2} * m * \cos(\beta) * \cos(\alpha - \gamma)$ $(A9.2.7)$

Substituting for α, β and γ and further simplifying, we have the following:

$$I_{im} = \frac{\sqrt{3}}{2} * I_{om} * m * \cos(\varphi_L) \qquad (A9.2.8)$$

A9.3 APPENDIX: From equation 9.13, $[T_{VSR}(\omega_i)]^T$ is given in equation A9.3.1 below:

$$[T_{VSR}(\omega_i)]^T = \left[\cos(\omega_i t - \varphi_i) \quad \cos(\omega_i t - \varphi_i - 120°) \quad \cos(\omega_i t - \varphi_i + 120°)\right] \qquad (A9.3.1)$$

Multiplying equation A9.3.1 with equation 9.11, we have the following:

$$[T_{VSR}(\omega_i)]^T * v_{iph} = V_{im} * [\cos(\omega_i t) * \cos(\omega_i t - \varphi_i) + \cos(\omega_i t - 120°) * \cos(\omega_i t - \varphi_i - 120°) + \cos(\omega_i t + 120°) * \cos(\omega_i t - \varphi_i + 120°)]$$

$$= \frac{V_{im}}{2} * [\cos(2\omega_i t - \varphi_i) + \cos(2\omega_i t - 240° - \varphi_i) + \cos(2\omega_i t + 240° - \varphi_i) + 3 * \cos(\varphi_i)] \qquad A9.3.2$$

$$= \frac{3 * V_{im}}{2} * \cos(\varphi_i) \qquad A9.3.3$$

A9.4 APPENDIX: Equation 9.41 can be rewritten as follows:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} (d_\mu + d_\lambda) * (d_\alpha + d_\beta) & (d_\mu + d_\lambda) * (-d_\alpha) & (d_\mu + d_\lambda) * (-d_\beta) \\ -d_\mu * (d_\alpha + d_\beta) & d_\mu * d_\alpha & d_\mu * d_\beta \\ -d_\lambda * (d_\alpha + d_\beta) & d_\lambda * d_\alpha & d_\lambda * d_\beta \end{bmatrix} * \begin{bmatrix} v_{AO} \\ v_{BO} \\ v_{CO} \end{bmatrix} \qquad (A9.4.1)$$

Simplifying, we have the following:

$$v_{ab} = (d_\mu + d_\lambda) * [d_\alpha * v_{AB} + d_\beta * v_{AC}] \qquad (A9.4.2)$$

$$v_{bc} = (-d_\mu) * [d_\alpha * v_{AB} + d_\beta * v_{AC}] \qquad (A9.4.3)$$

$$v_{ca} = (-d_\lambda) * [d_\alpha * v_{AB} + d_\beta * v_{AC}] \qquad (A9.4.4)$$

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} (d_\mu * d_\alpha + d_\lambda * d_\alpha) & (d_\mu * d_\beta + d_\lambda * d_\beta) \\ -d_\mu * d_\alpha & -d_\mu * d_\beta \\ -d_\lambda * d_\alpha & -d_\lambda * d_\beta \end{bmatrix} * \begin{bmatrix} v_{AB} \\ v_{AC} \end{bmatrix} \qquad (A9.4.5)$$

Let

$$d_\mu * d_\alpha = d_{\alpha\mu}$$

$$d_\lambda * d_\alpha = d_{\alpha\lambda}$$

$$d_\mu * d_\beta = d_{\beta\mu}$$

$$d_\lambda * d_\beta = d_{\beta\lambda} \qquad (A9.4.6)$$

Using equation A9.4.6 in A9.4.5, we have the following:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} (d_{\alpha\mu} + d_{\alpha\lambda}) & (d_{\beta\mu} + d_{\beta\lambda}) \\ -d_{\alpha\mu} & -d_{\beta\mu} \\ -d_{\alpha\lambda} & -d_{\beta\lambda} \end{bmatrix} * \begin{bmatrix} v_{AB} \\ v_{AC} \end{bmatrix} \qquad (A9.4.7)$$

Equation A9.4.7 corresponds to equation 9.42.

A9.5 APPENDIX: Table 9.1 to 9.6 are derived using the phasor diagram of the output voltage and input current for each sector as given in Fig. A9.5.1(A) to A9.5.1(F) for the former and Fig. A9.5.2(A) to A9.5.2(F). Their sector numbers are marked in the diagram. For example let the reference output voltage and input current vectors are in sector II and sector IV respectively, then SV = II and SI = IV and hence Fig. A9.5.1(B) and Fig. A9.5.2(D) must be considered. The switching time order sequence is $T_{\alpha\mu}$, $T_{\beta\mu}$, $T_{\beta\lambda}$, $T_{\alpha\lambda}$ and T_O respectively. Referring to Fig. A9.5.1(B) and Fig. A9.5.2(D), during $T_{\alpha\mu}$ time interval, corresponding to I_α-V_μ vector I3-V1, input phase B correspond to positive terminal p of rectifier and input phase A correspond to negative terminal n of rectifier. Three phase output voltage vector V1 is p,n,n and therefor output phase a correspond to input phase B and the output phase b and c correspond to input phase A and A or a,b,c is connected to B,A,A respectively. Similarly during time interval $T_{\beta\mu}$, for I_β-V_μ vector corresponding to I4-V1, input phase C and A correspond to p and n terminal of rectifier, V1 correspond to p,n,n and the output phase a, b and c are connected to C,A,A

respectively. During $T_{\beta\lambda}$ and $T_{\alpha\lambda}$ time interval, the vectors are I4-V2 and I3-V2 respectively. During time interval $T_{\beta\lambda}$, input phase C and A are connected to p and n terminal of rectifier, V2 correspond to p,p,n and the output phases a,b,c are connected to C,C,A respectively. In the same way during $T_{\alpha\lambda}$ time interval, input phase B and A are connected to p and n terminal of rectifier, and as output voltage

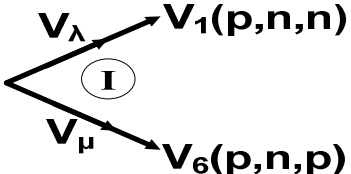


FIG. A9.5.1(A)

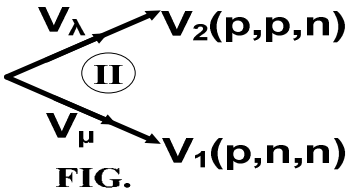


FIG. A9.5.1(B)

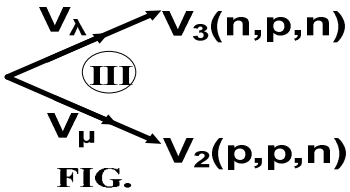


FIG. A9.5.1(C)

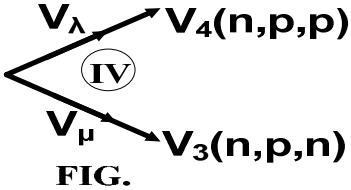


FIG. A9.5.1(D)

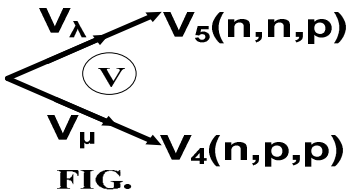


FIG. A9.5.1(E)

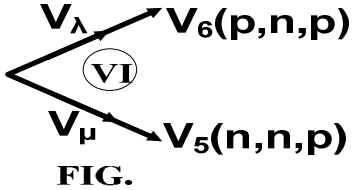


FIG. A9.5.1(F)

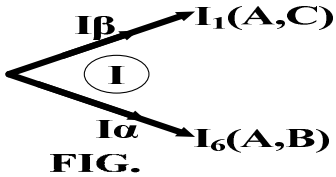


FIG. A9.5.2(A)

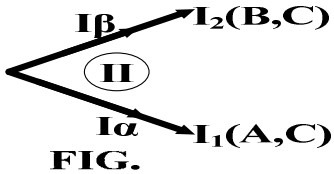


FIG. A9.5.2(B)

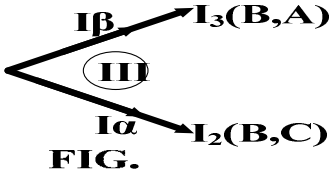


FIG. A9.5.2(C)

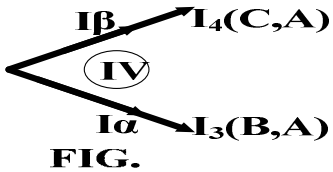


FIG. A9.5.2(D)

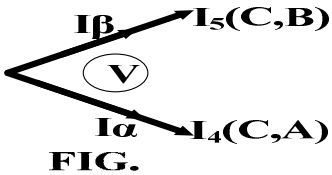


FIG. A9.5.2(E)

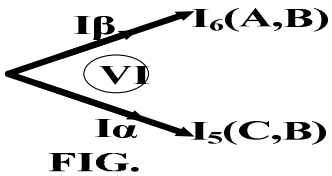


FIG. A9.5.2(F)

V2 correspond to p,p,n, output phases a,b,c are connected to B,B,A respectively. During time interval T_O, as the current vector SI is in IVth quadrant, the output phase a,b,c are connected to A,A,A respectively, as A is the common terminal to I3 and I4 input current vector. The Table 9.1 to 9.6 is filled in this way.

Chapter X

Dual Programmable AC to DC Rectifier Using Three Phase AC to Three Phase AC Matrix Converter Topology

10.1 INTRODUCTION: Three Phase AC to Three Phase AC Matrix Converter based dual AC to DC rectifier is reported in the literature [43-45]. But these reports only indicate that dual DC output voltages with fixed value is possible by setting the desired AC output voltage phase angle leading by 30 degrees and the frequency of output voltage zero in the model [43-44]. Detailed modelling studies using SIMULINK reveals that with the frequency of desired AC output voltage set to zero, as the AC output voltage phase angle is varied from 0 to $+\pi$ and 0 to $-\pi$, dual DC output voltages in multitude of combinations are possible such as a) Both voltages positive and unequal, b) Both voltages positive and equal, c) Any one voltage zero and the other positive, d) Any one Voltage positive and the other negative with unequal modulus value, e) Any one voltage positive and the other negative with equal modulus value, f) Any one Voltage zero and the other negative, g) Both voltages negative and unequal, h) Both voltages negative and equal. In this chapter, a detailed insight into this discovery is made with a mathematical derivation for the dual DC output voltage magnitude. Theoretical finding is confirmed by SIMULINK model simulation. The model is extended to verify the speed control, acceleration and braking of separately excited DC motors. Applications of this separately excited DC motor and Permanent Magnet DC (PMDC) motor for Hybrid Electric Vehicles (HEVs) and Electric Traction are highlighted.

10.2 OUTPUT VOLTAGE AMPLITUDE LIMIT OF DIRECT AC TO AC CONVERTERS: The three phase AC to three phase AC MC is shown in Fig. 3.1 of Chapter III. The model of the three phase AC to three phase AC MC in terms of modulation duty-cycle has been derived in equations 3.5 to 3.8 in section 3.2 of Chapter III. Venturini modulation algorithm which gives the solution of the modulation duty-cycle for the MC is also presented in equations 3.13 to 3.17 in section 3.2 of Chapter III. Now consider the three phase AC input voltage and desired three phase AC output voltage of the MC as defined in equations 3.9 and 3.11 in section 3.3 of chapter III. In order that the three phase output voltage waveform is synthesised or reconstructed from the three phase input voltage waveform without distortion, it is necessary to switch the bidirectional switches of the MC at a high sampling rate or carrier frequency much higher than the input frequency and the desired output frequency. It is also a requirement that the output voltage waveform so synthesised or reconstructed from the input voltage waveform must lie within the upper and lower bounds of the input voltage waveform at every instant of time. This requirement can be expressed as follows [2-3]:

$$v_{i\_LB}(t) \le v_o(t) \le v_{i\_UB}(t) \qquad (10.1)$$

where $v_{i\_LB}(t)$ and $v_{i\_UB}(t)$ represents the Lower and Upper Bounds of the input voltage $v_i(t)$.

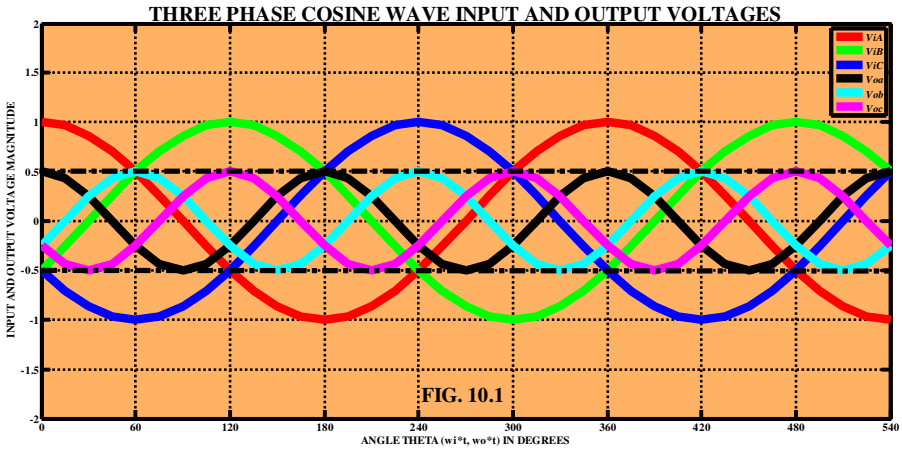


FIG. 10.1

Now considering the general case of the three phase input and three phase output voltage waveform defined in equations 3.9 and 3.11 in section 3.3 of chapter III, where the input and output frequency ω_i and ω_O are not correlated, the equation 10.1 can be expressed as follows [2-3]:

$$\underset{0 \le \omega_i.t \le 2\pi}{\underset{min}{v_{i\_UB}(t)}} \geq \underset{0 \le \omega_O.t \le 2\pi}{\underset{max}{v_{O\_UB}(t)}} \quad (10.2)$$

where

$\underset{max}{v_{O\_UB}}$ *is the maximum value of output voltage upper bound*

$\underset{min}{v_{i\_UB}}$ *is the minimum value of input voltage upper bound*

The condition given by equation 10.2 is shown in Fig. 10.1. Thus for a distortion less synthesis or reconstruction of the output voltage waveform from the three phase input voltage, the maximum value of the output voltage at any time should not exceed the input voltage value where $v_{iA} = v_{iB} = v_{iC}$ or at the intersecting point of the three phase input voltages. This can be expressed as follows:

$$V_{im} * cos(\omega_i.t) = V_{im} * cos\left(\omega_i.t - \frac{2\pi}{3}\right) = V_{im} * cos\left(\omega_i.t - \frac{4\pi}{3}\right) \quad (10.3)$$

Equation 10.3 is valid at intervals of $\pi/3$ radians and the magnitude at the intersecting point of the three phase input voltages is (0.5*Vim) [2-3]. This is illustrated in Fig. 10.1. The condition given in equation 10.2 requires the following equation to be valid [2-3]:

$$\left.\begin{aligned} v_O(t) &\le 0.5 * v_i(t) \\ V_{om} &= 0.5 * V_{im} \end{aligned}\right] \quad (10.4)$$

Equation 10.4 is independent of the conversion algorithm used. The maximum value of the output amplitude is obtained when the maximum value of the difference between the output voltage upper bound and output voltage lower bound coincides with minimum value of the difference between the input voltage upper bound and the input voltage lower bound. Referring to Fig. 10.1, the maximum value of the upper bound of the output voltage *Voa* varies from 0 to $0.5*V_{im}$ with respect to time while for the other two output phases Vob and Voc the lower bound of the output voltage varies from

0.5*Vim to -0.5*Vim and -0.5*Vim to +0.5*Vim respectively. At any instant of time during the positive half cycle of the output voltage *Voa*, this maximum value of the difference between the upper and lower bounds of the output voltage is therefor the phasor difference between *Voa* and *Vob* or *Voa* and *Voc* which can be expressed as follows [2-3]:

$$\left(\underset{0 \le \omega_O.t \le 2\pi}{MAX} \left(v_{O\_UB}(t) - v_{O\_LB}(t) \right) \right) = \left(\vec{V}_{oa} - \vec{V}_{ob} \right) = \left(\vec{V}_{oa} - \vec{V}_{oc} \right) = \left(\sqrt{3} \right) * V_{om} \qquad (10.5)$$

Equation 10.5 gives the maximum value of the line to line output voltage. From Fig. 10.1, for the three phase input voltage, the minimum value of the lower bound for ViA is -Vim and the minimum value of the upper bound for the input voltages ViB and ViC are +0.5*Vim respectively which can be expressed as follows [2-3]:

$$\left(\underset{0 \le \omega_i.t \le 2\pi}{MIN} \left(v_{i\_UB} - v_{i\_LB} \right) \right) = \left[+0.5 * V_{im} - \left(-V_{im} \right) \right] = \frac{3 * V_{im}}{2} \qquad (10.6)$$

Equating equations 10.5 and 10.6, the maximum output voltage amplitude obtainable can be expressed as follows [2-3]:

$$\left. \begin{aligned} V_{om} &= \frac{\sqrt{3}}{2} * V_{im} = 0.866 * V_{im} \\ V_O &= 0.866 * V_i \end{aligned} \right] \qquad (10.7)$$

Equation 10.7 gives the maximum output voltage amplitude obtainable for a three phase AC to three Phase AC MC.

10.3 PRINCIPLE OF DUAL PROGRAMMABLE AC TO DC RECTIFIER: For the three phase AC input voltage and the output voltage as defined in equations 3.9 and 3.11, Venturini modulation algorithm for Modulation Duty-Cycle which satisfies equations 3.11 and 3.12 assuming Unity Input Phase Displacement Factor is given in equation 3.17 in section 3.3 of Chapter III. For the above three phase MC to work as an AC to DC rectifier, the output frequency fo is to be set to zero [43-44]. This makes equation 3.10 and 3.11 given in section 3.3 of chapter III as follows:

$$io = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = I_{om} * \begin{bmatrix} cos(\varphi_o) \\ cos(\varphi_o - \frac{2\pi}{3}) \\ cos(\varphi_o + \frac{2\pi}{3}) \end{bmatrix} \qquad (10.8)$$

$$vo = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = q * V_{im} * \begin{bmatrix} cos(\varphi_o) \\ cos(\varphi_o - \frac{2\pi}{3}) \\ cos(\varphi_o + \frac{2\pi}{3}) \end{bmatrix} \qquad (10.9)$$

In equation 10.9, if the output voltage phase angle φ_O is set to +30 degrees, it is seen that the output voltage vb becomes zero, where as va and vc have equal magnitude [43-44]. In any three phase AC to three phase AC matrix converter, the intrinsic output voltage limit irrespective of control algorithm

used is given by equation 10.7 [2-3]. In the linear region of the modulation index q, the input-output voltage relation in an MC can be expressed as follows:

$$v_o = \quad q * v_i \qquad (10.10)$$

Combining equations 10.7 and 10.10, we have the following:

$$v_{om} = \quad 0.866 * q * V_{im} \qquad (10.11)$$

Three phase output voltage in equation 3.11 of chapter III is shown in Fig. 10.2(A). With b as virtual ground or virtual reference point, for any arbitrary angular frequency ω_O of the output voltage, vab and vcb which correspond to vo1 and vo2, leads va by $\pi/6$ and $\pi/2$ radians respectively. Now noting that for the three phase MC to work as a dual AC to DC rectifier the output frequency ω_O is zero, combining equation 10.11 and noting the phase lead of vab and vcb with respect to va, equations 10.12 and 10.13 follows:

$$V_{ab} = V_{o1} = \ 0.866 * q * V_{im} * \ cos\left(\varphi_o + \frac{\pi}{6}\right) \qquad (10.12)$$

$$V_{cb} = -V_{bc} = \ V_{o2} = \ 0.866 * q * V_{im} * \ cos\left(\varphi_o + \frac{\pi}{2}\right) \qquad (10.13)$$

Equations 10.12 and 10.13 are discussed in A10.1 Appendix. When a practical implementation is considered, a question arises whether the three phase AC voltage generated by the grid is a sine wave or cosine wave ? Evidently it is a sine wave of the form ViK = Vim*sin(ω_i.t – γ) where γ = 0, $2\pi/3$, $4\pi/3$ for K = A, B, C respectively. Considering this factor, a phase lag of $\pi/2$ radians is given to the three phase AC input and output voltage defined in equations 3.9 and 3.11 of chapter III. This permits three phase sine wave AC input voltage to be used for practical implementation. With a phase lag of $\pi/2$ radians given to the three phase output voltage defined in equation 3.11 of chapter III, the new

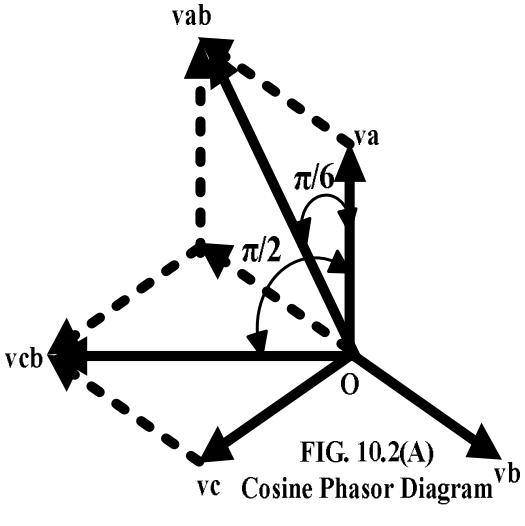


FIG. 10.2(A) Cosine Phasor Diagram

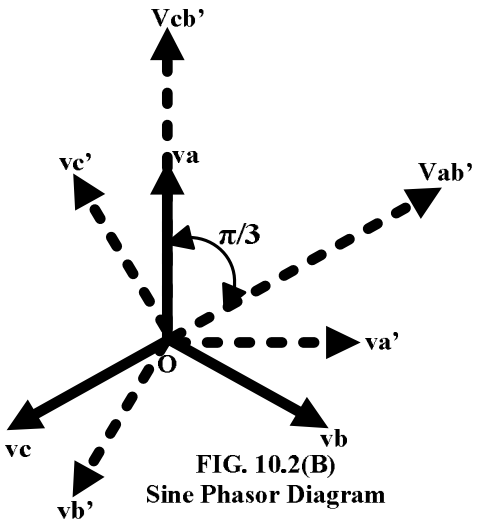


FIG. 10.2(B) Sine Phasor Diagram

phasor diagram is shown in Fig. 10.2(B). The new position of va, vb and vc are marked va', vb' and vc' respectively. The new position of vab and vcb are marked vab' and vcb' which lag the original position of vab and vcb in Fig. 10.2(A) by $\pi/2$ radians. Thus the new position of vab' and vcb' in Fig. 10.2(B), lag the original position of va in Fig. 10.2(A) by $\pi/3$ and zero radians respectively. Now noting that for the three phase MC to work as a dual AC to DC rectifier the output frequency ω_O is

zero, combining equation 10.11 and noting the phase lag of vab' and vcb' with respect to va, equations 10.14 and 10.15 follows:

$$V'_{ab} = V_{o1} = 0.866 * q * V_{im} * \cos\left(\varphi_O - \frac{\pi}{3}\right) \qquad (10.14)$$

$$V'_{cb} = -V'_{bc} = V_{o2} = 0.866 * q * V_{im} * \cos(\varphi_O) \qquad (10.15)$$

As can be seen from equations 10.14 and 10.15, when φ_O is varied from 0 to $+\pi$ and 0 to $-\pi$, multitude of combination of dual DC output voltages are possible. Thus by suitable changing the value of φ_O in the model of three phase MC, dual programmable DC output voltages can be obtained.

10.4 MODEL OF DUAL PROGRAMMABLE AC TO DC RECTIFIER: The model of the Dual programmable AC to DC rectifier is shown in Fig.10.3. The model is developed in SIMULINK [51]. Here Venturini algorithm for unity input phase displacement factor is assumed in generating the gate pulses for the bidirectional switches. Also three phase sine wave input and output voltages are used for developing the model. The above algorithm is proved valid for three phase sine wave input and output voltage in A3.3 Appendix in Chapter III. The model consists of a) Bidirectional switch gate pulse generator b) Output voltage phase angle varying device c) Three phase sine wave AC voltage source d) MC bidirectional switch matrix e) RLC output filter f) RL load. The parameters used for the model is given in Table 10.1.

TABLE 10.1: Dual Programable AC to DC Rectifier – SIMULINK Model Parameters

Sl.No.	Parameter	Value	Unit
1)	Maximum Line to Neutral Input Voltage Vim	(220*1.414)	Volts
2)	Modulation Index q	0.5	--
3)	Input Frequency	50	Hz
4)	Output Frequency	0	Hz
5)	Saw-tooth Carrier Switching Frequency	2	kHz
6)	Output R-L-C Filter	50, 10e-6, 633.9e-6	Ω, H, F
7)	R-L Load	50, 0.5	Ω, H

Bidirectional switch gate pulse generator is shown in Fig. 10.4(A). This consists of two embedded MATLAB functions. The first MATLAB function generates the nine modulation functions according to equations 3.17 of Chapter III, using inputs q, Vim, fi, fo, phi_o and the time module. The second MATLAB function generates the gate timing pulse for the nine bidirectional switches, by comparison of the modulation functions with a saw-tooth carrier vsaw. The code for generating the timing pulse for the bidirectional switches connected between input phase A, B, C and output phase a, b, c is given in section 3.4.1 of Chapter III. Output Voltage Phase Angle Varying Device is shown in Fig.10.3. This is using slider gain block. The constant block with value +pi/12 is given as input to the slider gain block whose multiplication constant can be varied from -12 to +12. Appropriate gain multiplier value is entered in the current value field of slider gain block. The output of slider gain provides the variable output voltage phase angle φ_O in radians. Three Phase AC Sine Wave voltage Source is shown in Fig. 10.4(B). This three phase AC sine wave source is from the SimPowerSystems blockset. This three phase sine wave AC source generates three phase voltage with a line to line RMS value of

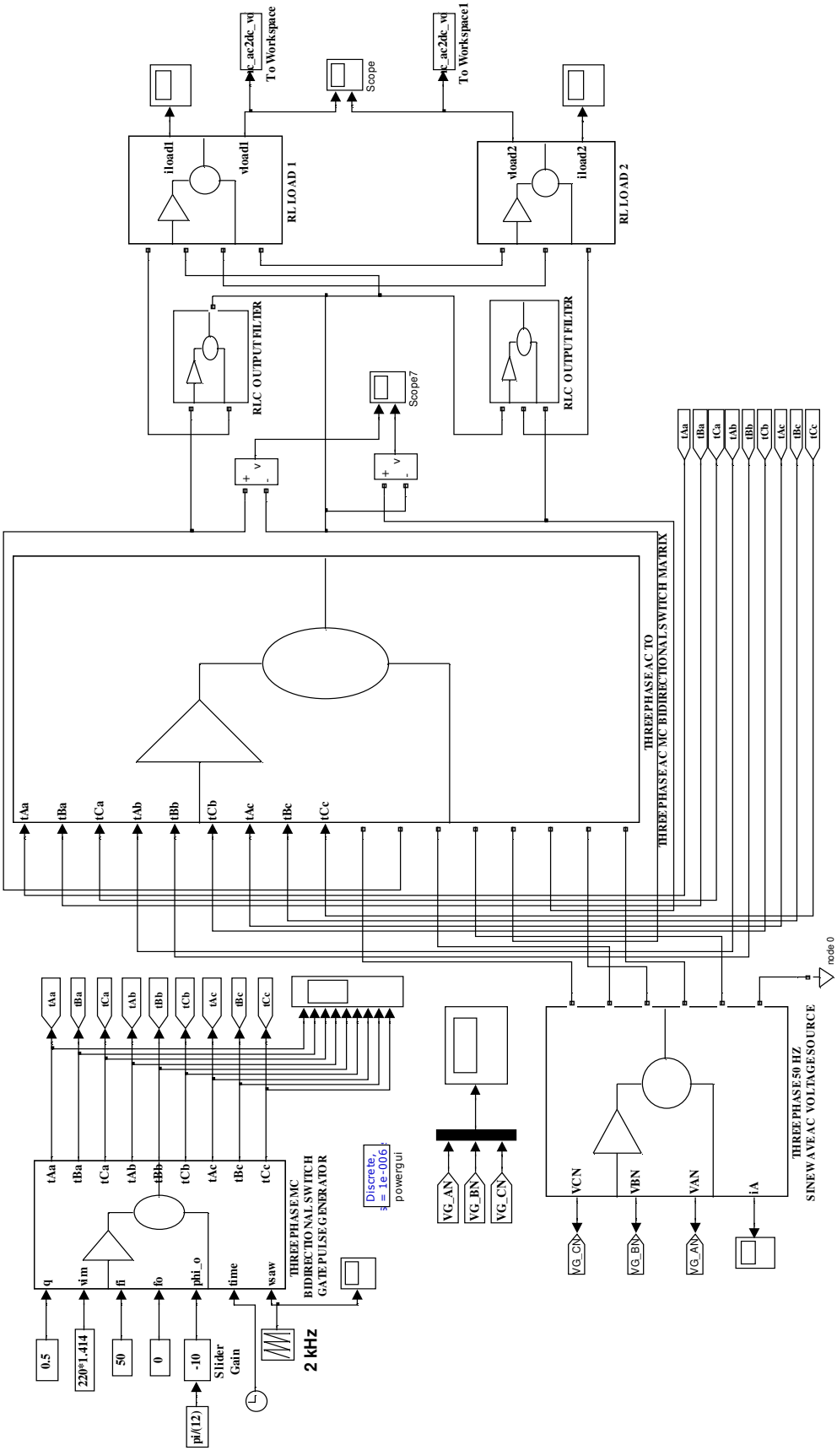


FIG. 10.3: DUAL PROGRAMMABLE AC TO DC RECTIFIER USING THREE PHASE MATRIX CONVERTER TOPOLOGY

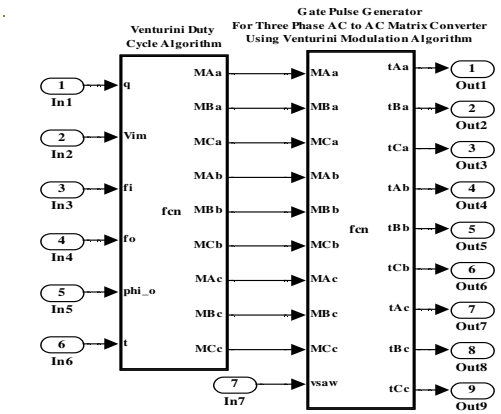


FIG. 10.4(A)

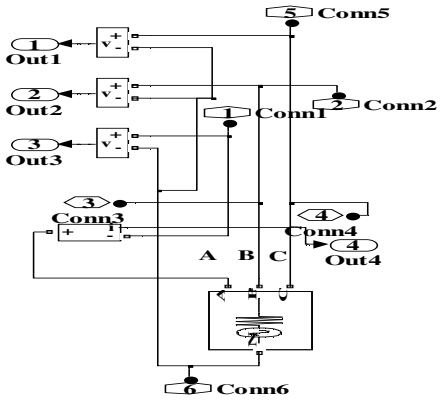


FIG. 10.4(B)

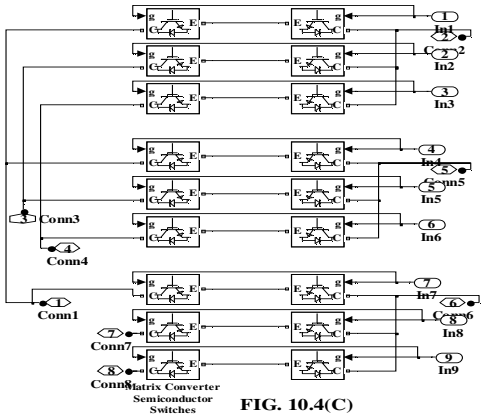


FIG. 10.4(C)

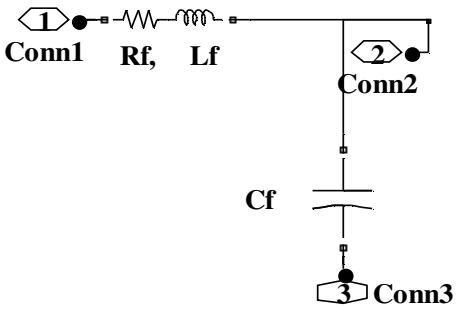


FIG. 10.4(D)

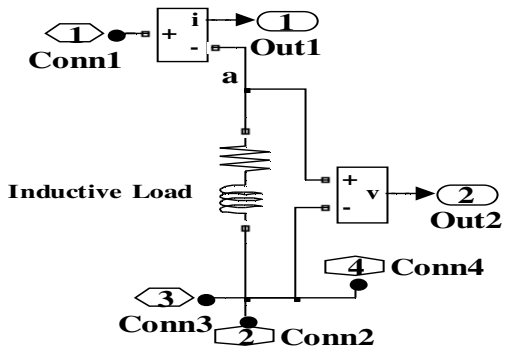


FIG. 10.4(E)

381.04 Volts and frequency 50 Hz. The nine MC Bidirectional Switch Matrix using IGBTs and diodes is shown in Fig. 10.4(C). RLC Output Filter is shown in Fig. 10.4(D). The L and C values are so chosen to resonate at the carrier switching frequency of 2 kHz. The output voltage is tapped across the filter capacitor. RL Load is shown in Fig. 10.4(E).

The theoretically computed value of the dual DC output voltages Vo1 and Vo2 using equations 10.14 and 10.15 for the parameters shown in Table 10.1 is given in Table 10.2 for various values of output voltage phase angle φ_O radians.

10.4.1 SIMULATION RESULTS: The simulation of the Dual Programmable AC to DC rectifier was carried out in SIMULINK [51]. The ode15s(Stiff/NDF) solver is used. The simulation results for the value of φ_O shown in the order in Table 10.2 are shown in Fig, 10.5(A) to (X). The simulation results are shown in Table 10.3. The model simulation results indicate that the magnitude and sign of vo1 and vo2 closely agree with the theoretically computed value shown in Table 10.2.

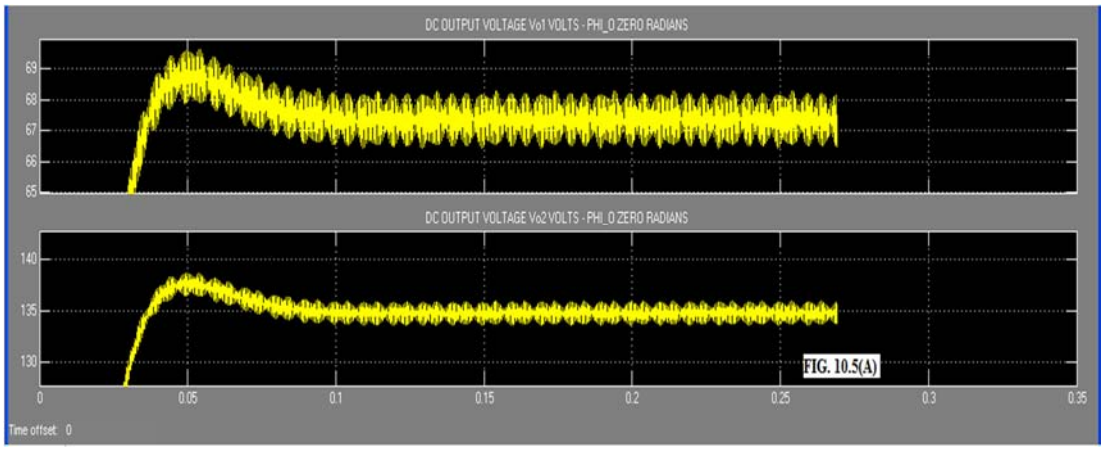
TABLE 10.2: Theoretically Computed Values

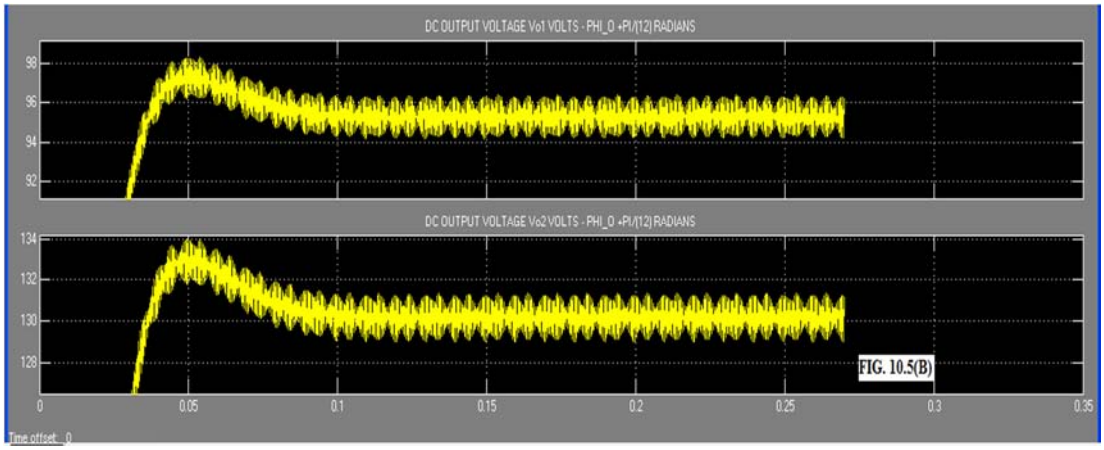
Sl.No.	φo radians	Vo1 Volts	Vo2 Volts	Sl.No.	φo radians	Vo1 Volts	Vo2 Volts
1	0	67.34	134.64	13	±π	-67.34	-134.69
2	+π/12	95.24	130.107	14	-11π/12	-95.24	-130.107
3	+π/6	116.64	116.64	15	-5π/6	-116.64	-116.64
4	+π/4	130.1	95.24	16	-3π/4	-130.107	-95.24
5	+π/3	134.69	67.34	17	-2π/3	-134.69	-67.34
6	+5π/12	130.107	34.86	18	-7π/12	-130.107	-34.86
7	+π/2	116.64	0	19	-π/2	-116.64	0
8	+7π/12	95.24	-34.8	20	-5π/12	-95.24	34.86
9	+2π/3	67.34	-67.34	21	-π/3	-67.34	67.34
10	+3π/4	34.86	-95.24	22	-π/4	-34.86	95.24
11	+5π/6	0	-116.64	23	-π/6	0	116.64
12	+11π/12	-34.86	-130.107	24	-π/12	34.86	130.107

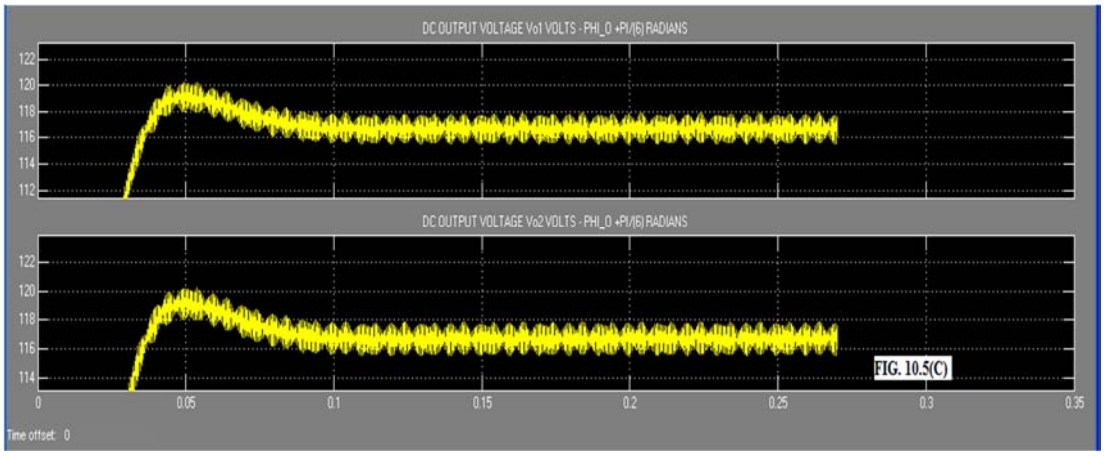
TABLE 10.3: Model Simulation Results

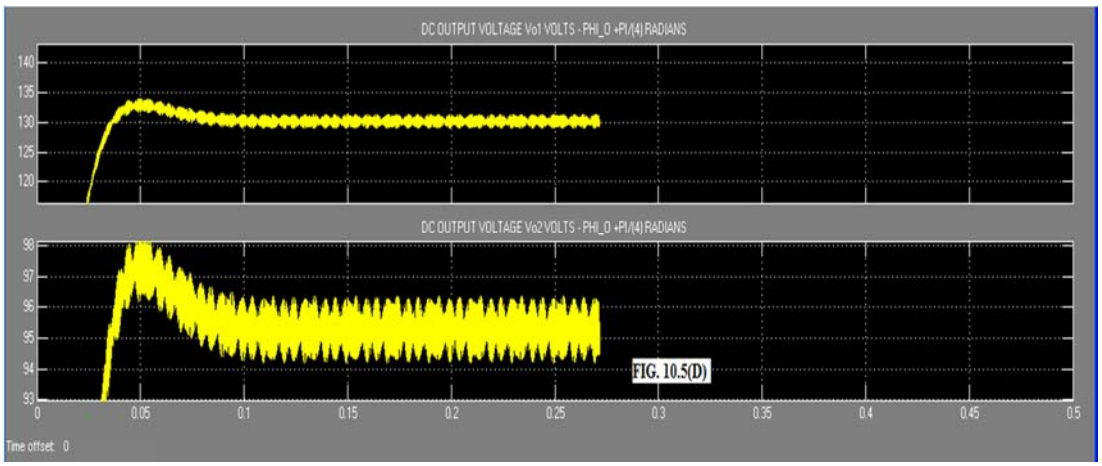
Sl.No.	φo radians	Vo1 Volts	Vo2 Volts	Sl.No.	φo radians	Vo1 Volts	Vo2 Volts
1	0	67.5	135	13	±π	-67.5	-135
2	+π/12	95.1	130	14	-11π/12	-95	-130
3	+π/6	117	117	15	-5π/6	-116.5	-116.5
4	+π/4	130	95.5	16	-3π/4	-130	-95
5	+π/3	135	67.5	17	-2π/3	-135	-67.5
6	+5π/12	130	35	18	-7π/12	-130	-35
7	+π/2	116	0	19	-π/2	-116.5	0
8	+7π/12	95	-35	20	-5π/12	-95	35
9	+2π/3	67.5	-67.5	21	-π/3	-67.5	67.5
10	+3π/4	35	-95	22	-π/4	-35	95
11	+5π/6	0	-117	23	-π/6	0	117
12	+11π/12	-35	-130	24	-π/12	35	130

10.5 MODEL OF DUAL PROGRAMMABLE AC TO DC RECTIFIER FED SEPARATELY EXCITED DC MOTORS: The model of the Dual programmable AC to DC rectifier fed DC Motor


DC OUTPUT VOLTAGE Vo1 VOLTS - PHI_0 ZERO RADIANS
DC OUTPUT VOLTAGE Vo2 VOLTS - PHI_0 ZERO RADIANS
FIG. 10.5(A)
Time offset: 0


DC OUTPUT VOLTAGE Vo1 VOLTS - PHI_0 +PI/(12) RADIANS
DC OUTPUT VOLTAGE Vo2 VOLTS - PHI_0 +PI/(12) RADIANS
FIG. 10.5(B)


DC OUTPUT VOLTAGE Vo1 VOLTS - PHI_0 +PI/(6) RADIANS
DC OUTPUT VOLTAGE Vo2 VOLTS - PHI_0 +PI/(6) RADIANS
FIG. 10.5(C)
Time offset: 0


DC OUTPUT VOLTAGE Vo1 VOLTS - PHI_0 +PI/(4) RADIANS
DC OUTPUT VOLTAGE Vo2 VOLTS - PHI_0 +PI/(4) RADIANS
FIG. 10.5(D)
Time offset: 0

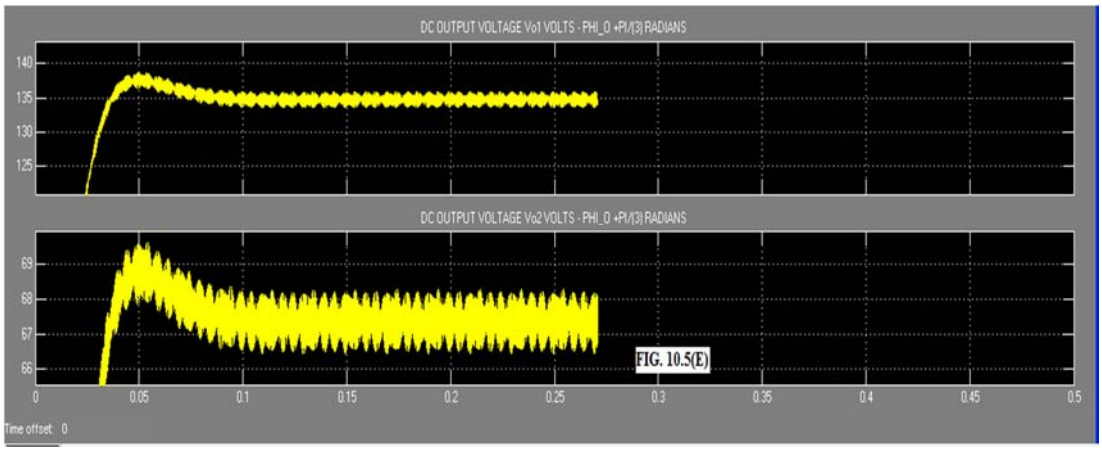


FIG. 10.5(E)

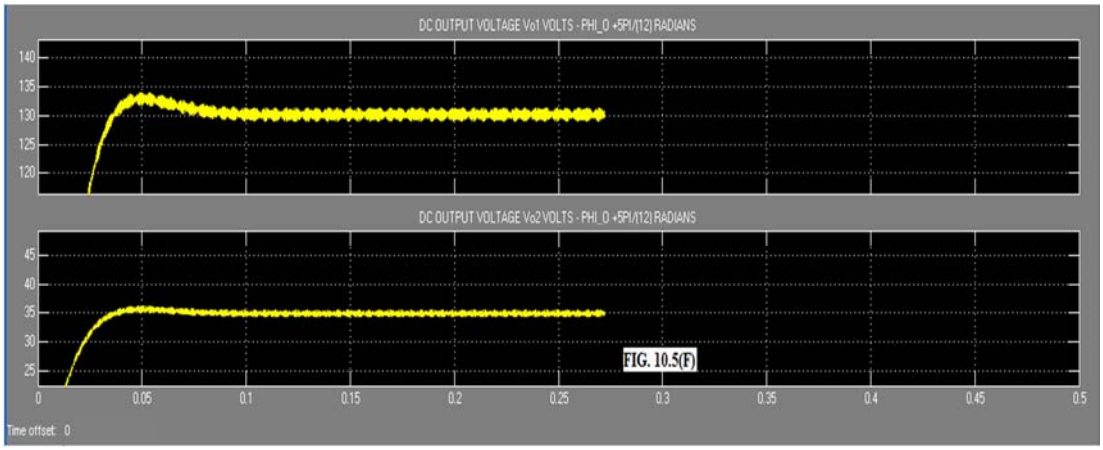


FIG. 10.5(F)

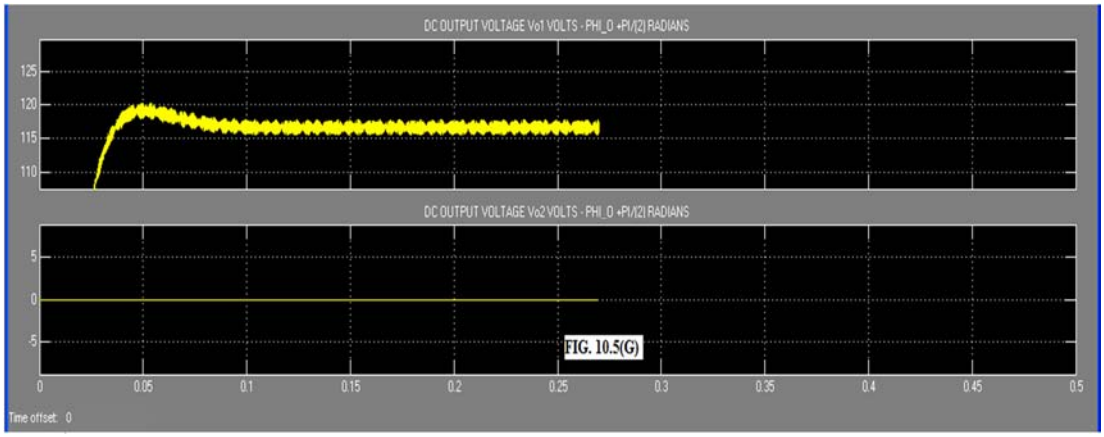


FIG. 10.5(G)

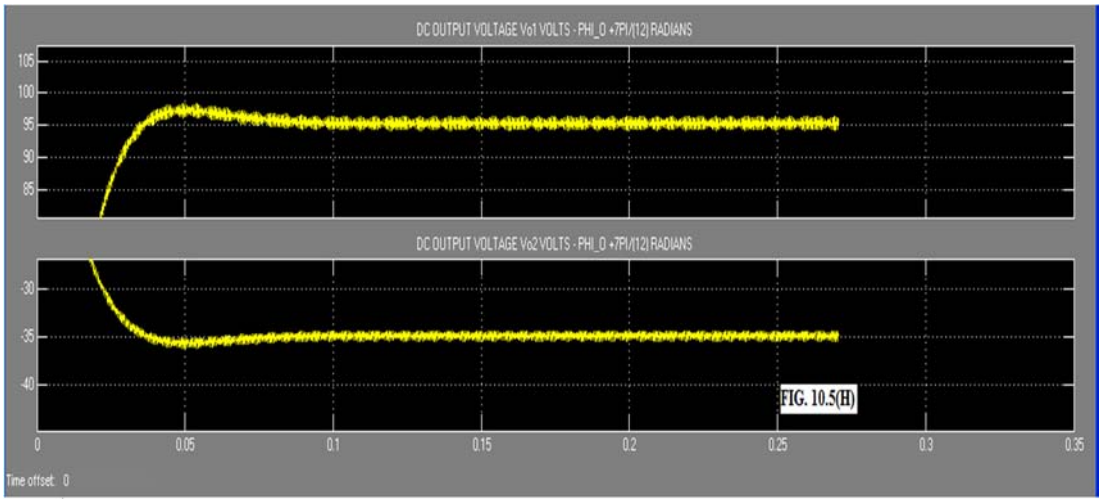


FIG. 10.5(H)

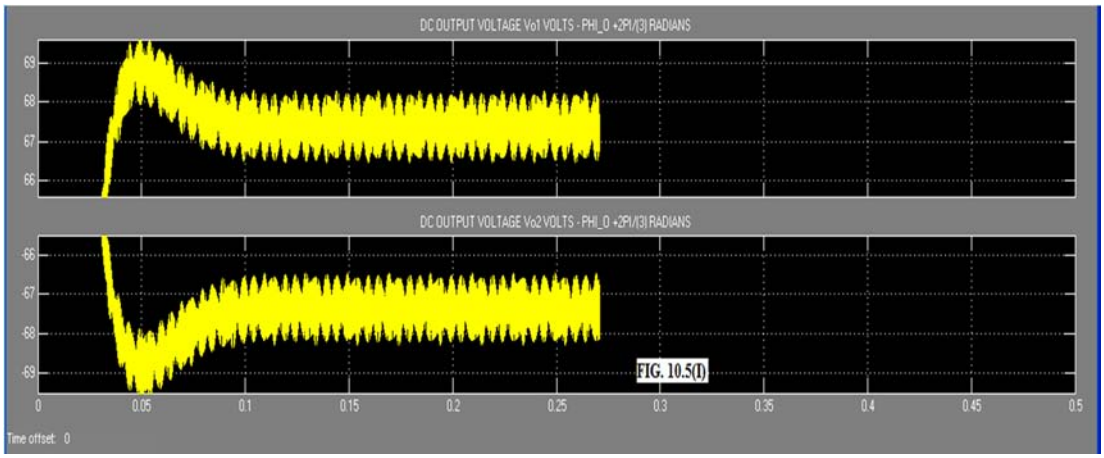


FIG. 10.5(I)

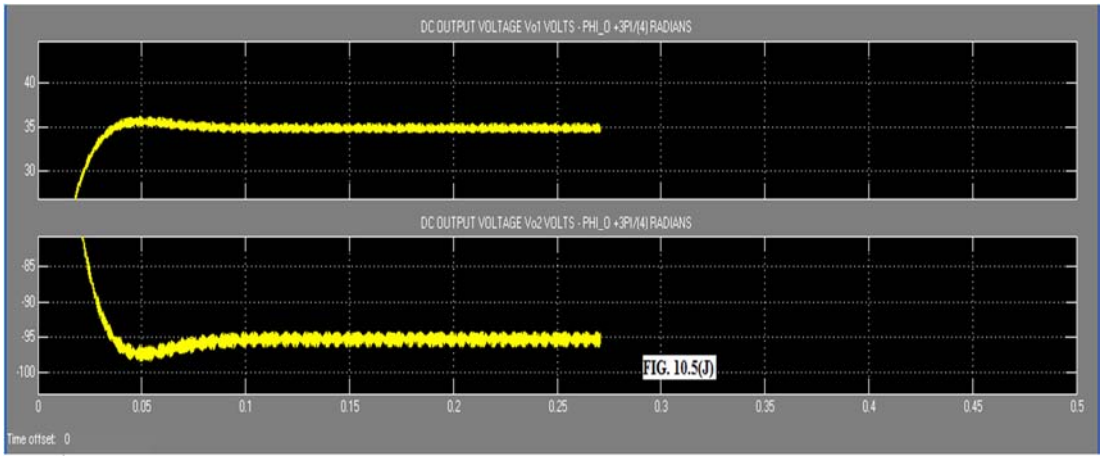


FIG. 10.5(J)

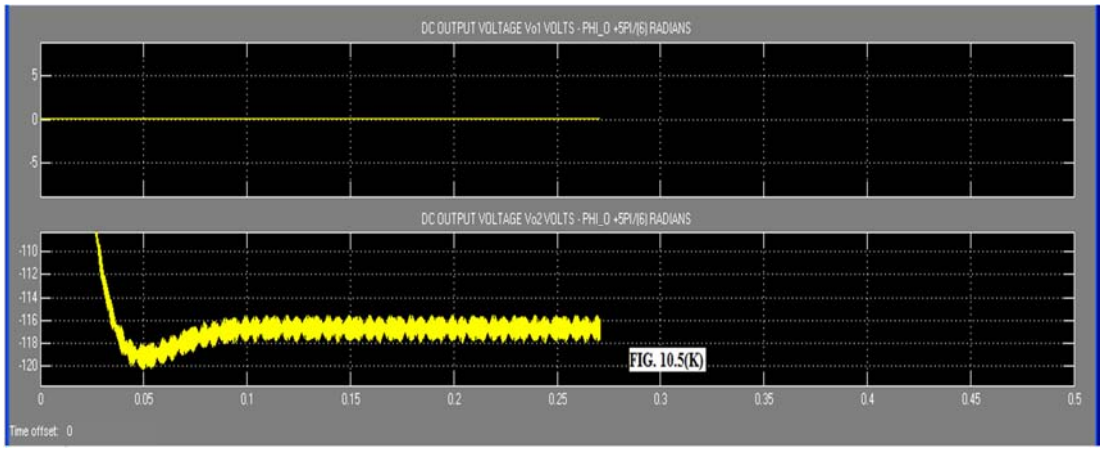


FIG. 10.5(K)

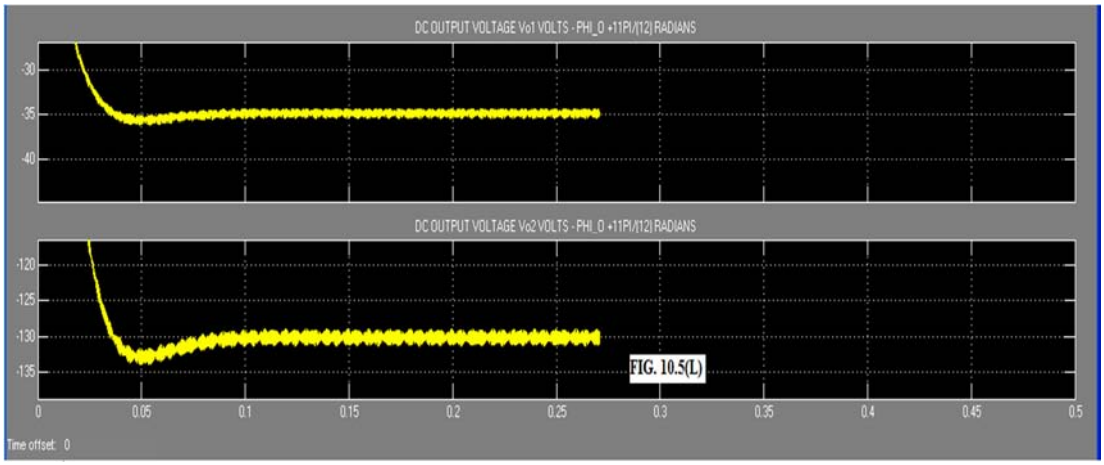


FIG. 10.5(L)

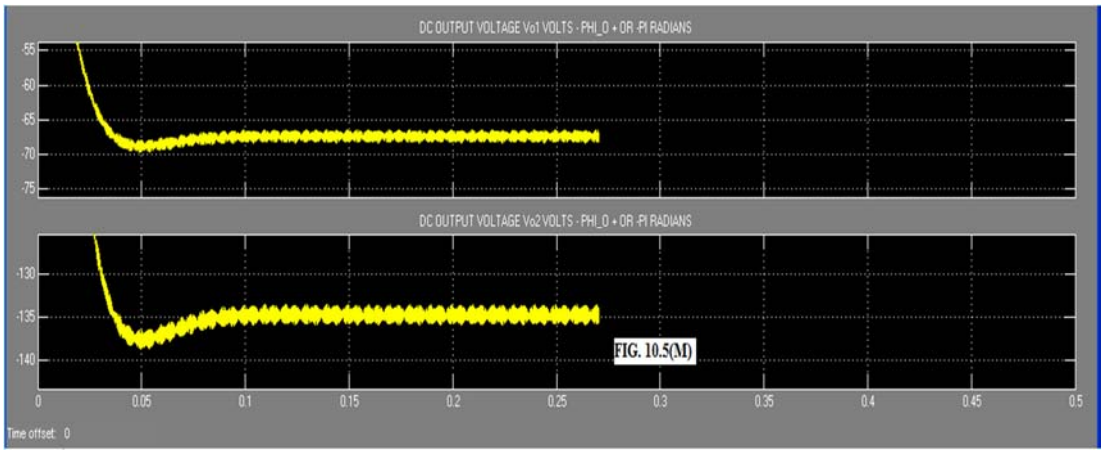


FIG. 10.5(M)

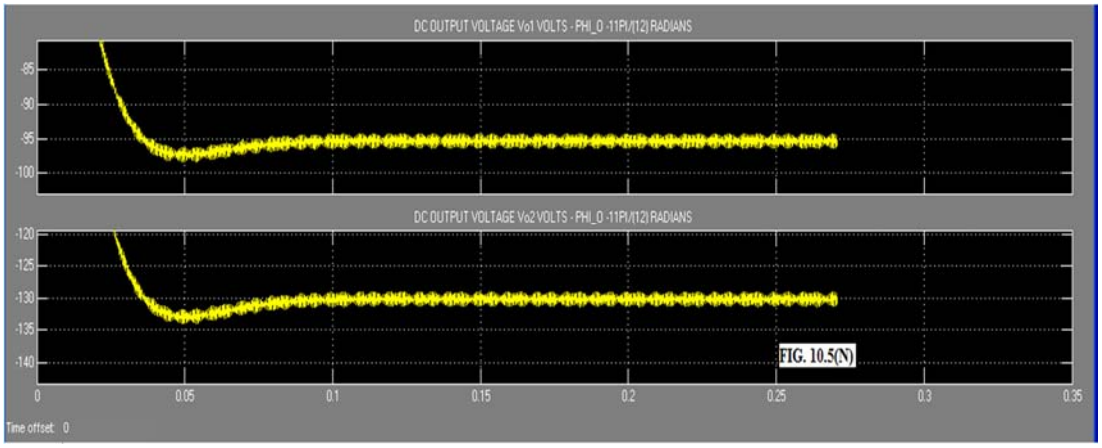


FIG. 10.5(N)

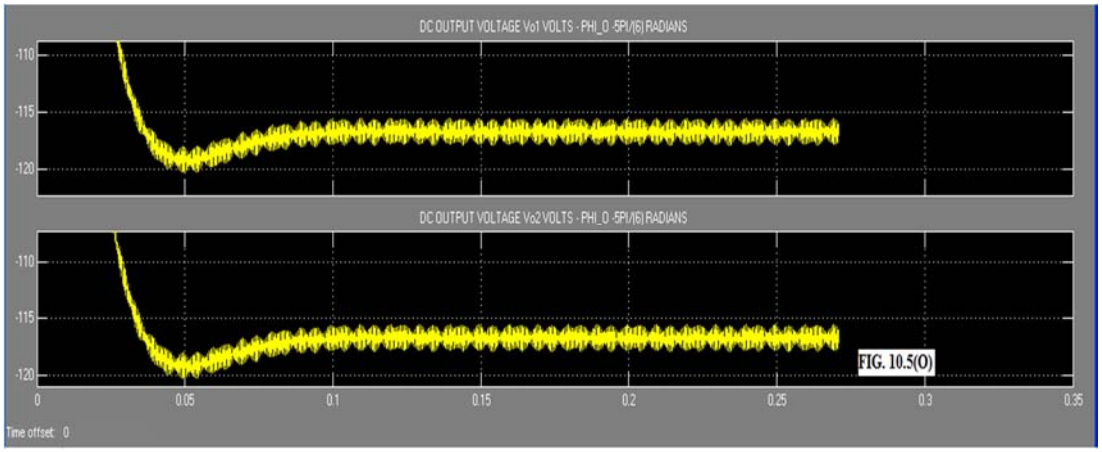


FIG. 10.5(O)

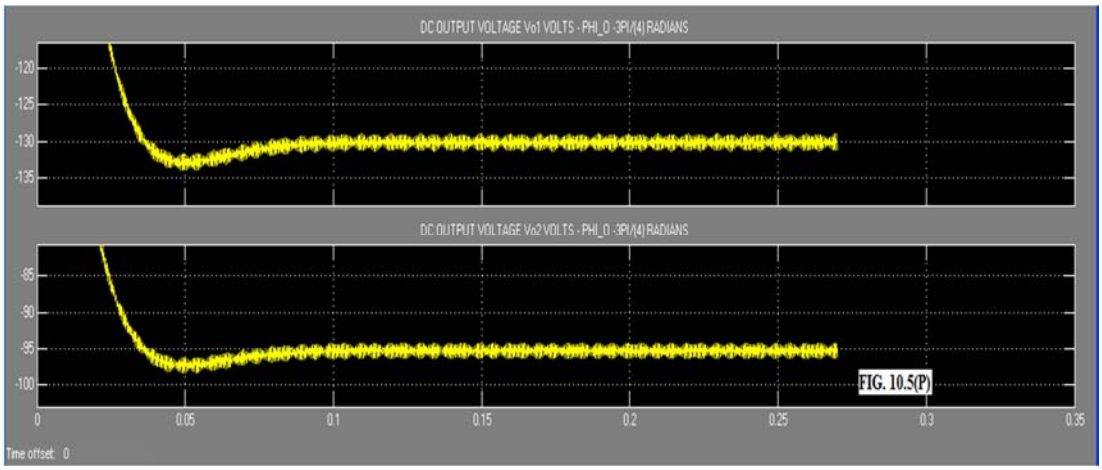
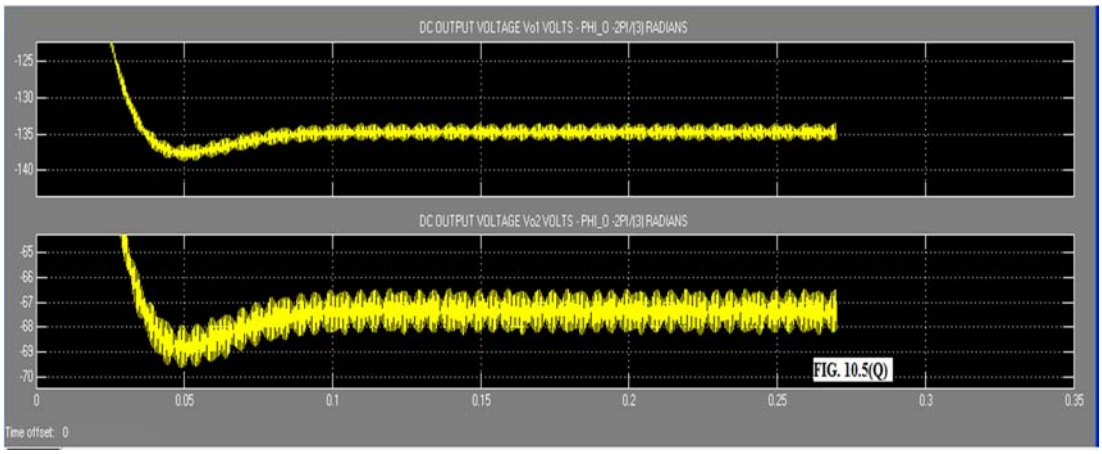
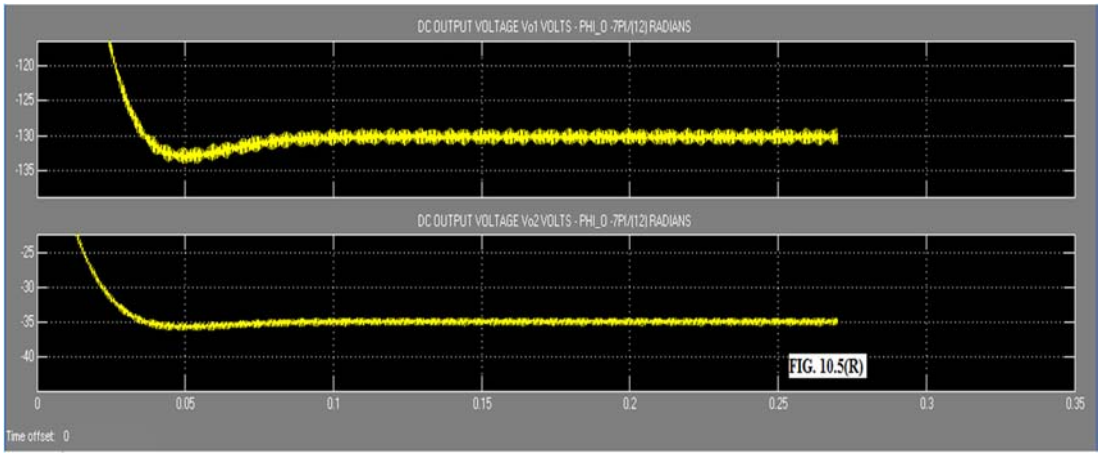
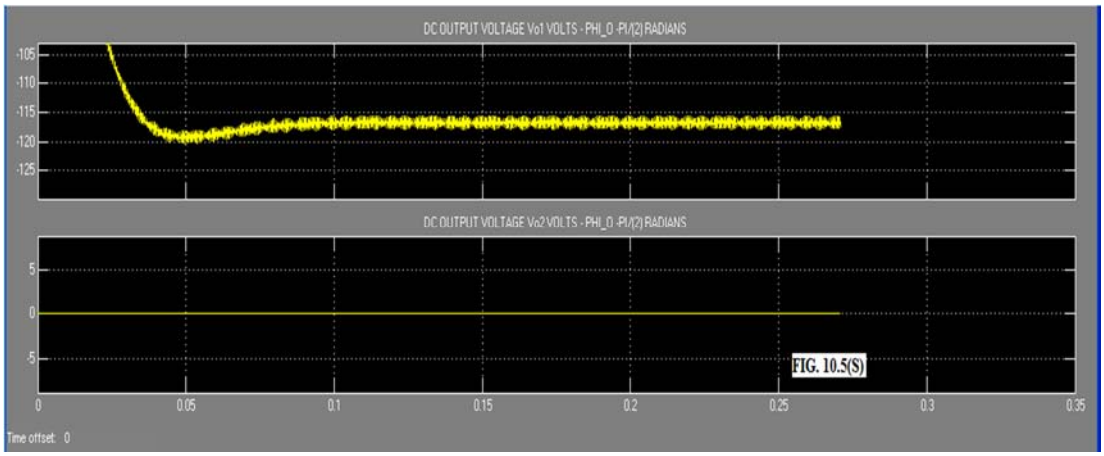
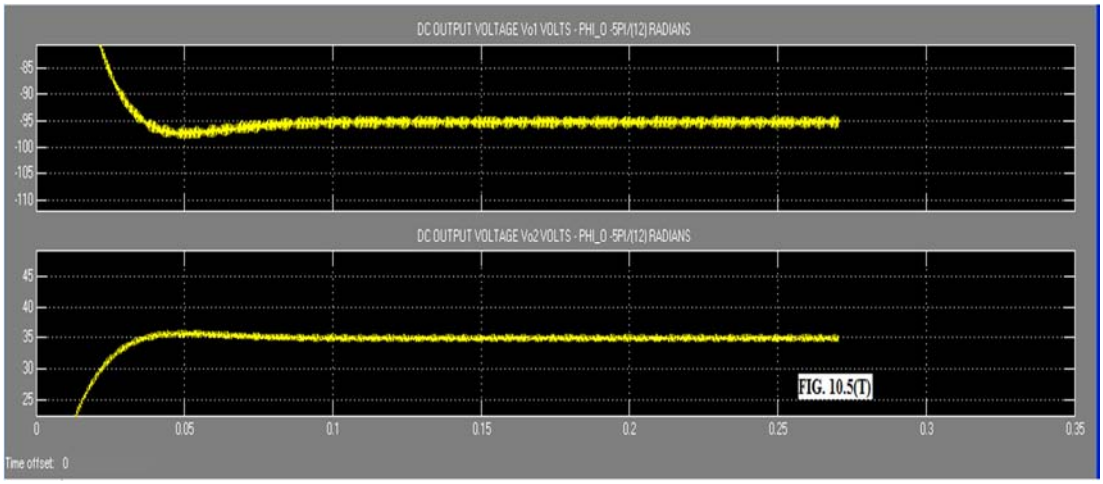


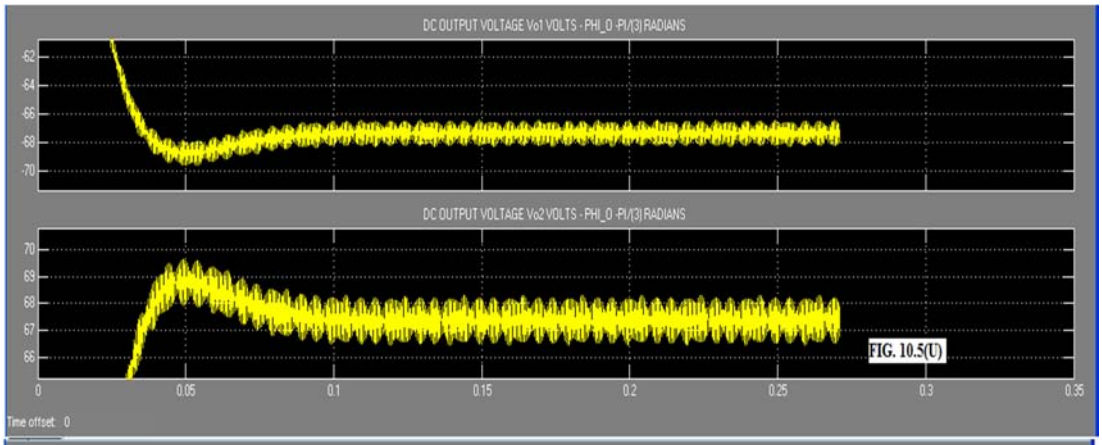
FIG. 10.5(P)

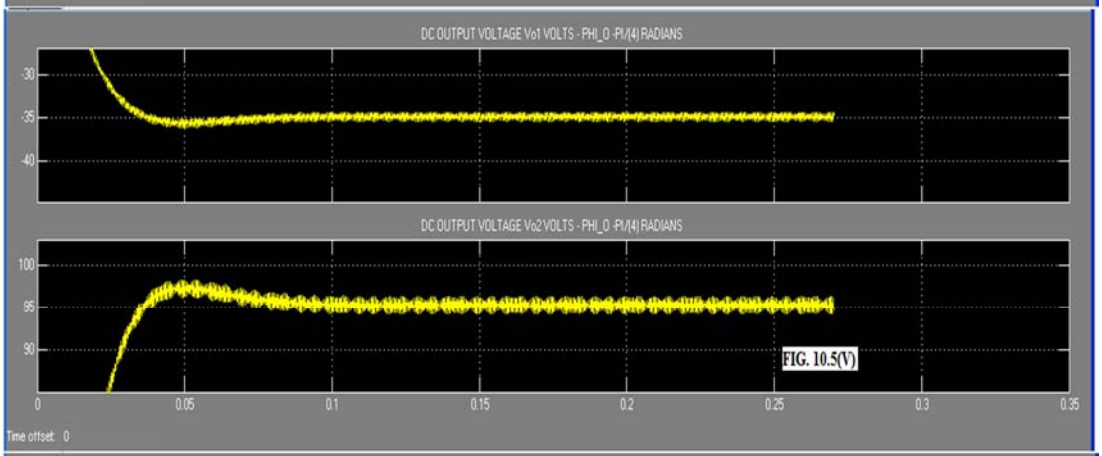

DC OUTPUT VOLTAGE Vo1 VOLTS - PHI_0 -2PI/(3) RADIANS
DC OUTPUT VOLTAGE Vo2 VOLTS - PHI_0 -2PI/(3) RADIANS
FIG. 10.5(Q)
Time offset: 0

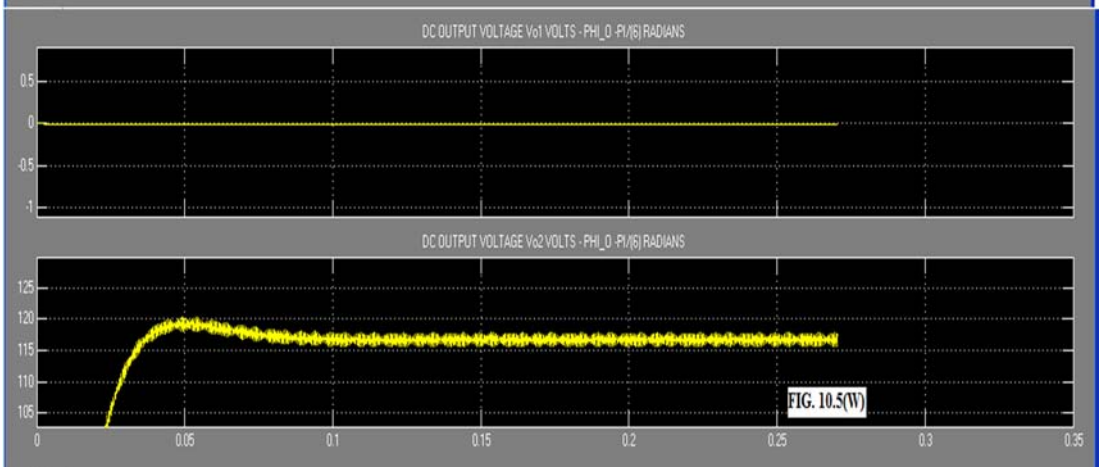

DC OUTPUT VOLTAGE Vo1 VOLTS - PHI_0 -7PI/(12) RADIANS
DC OUTPUT VOLTAGE Vo2 VOLTS - PHI_0 -7PI/(12) RADIANS
FIG. 10.5(R)
Time offset: 0

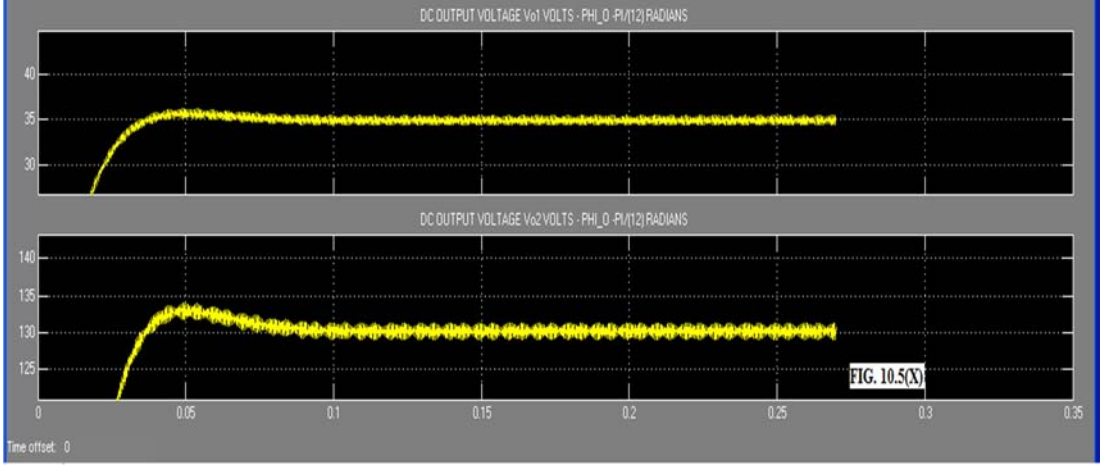

DC OUTPUT VOLTAGE Vo1 VOLTS - PHI_0 -PI/(2) RADIANS
DC OUTPUT VOLTAGE Vo2 VOLTS - PHI_0 -PI/(2) RADIANS
FIG. 10.5(S)
Time offset: 0


DC OUTPUT VOLTAGE Vo1 VOLTS - PHI_0 -5PI/(12) RADIANS
DC OUTPUT VOLTAGE Vo2 VOLTS - PHI_0 -5PI/(12) RADIANS
FIG. 10.5(T)
Time offset: 0


DC OUTPUT VOLTAGE Vo1 VOLTS - PHI_0 -PI/(3) RADIANS
DC OUTPUT VOLTAGE Vo2 VOLTS - PHI_0 -PI/(3) RADIANS
FIG. 10.5(U)
Time offset: 0


DC OUTPUT VOLTAGE Vo1 VOLTS - PHI_0 -PI/(4) RADIANS
DC OUTPUT VOLTAGE Vo2 VOLTS - PHI_0 -PI/(4) RADIANS
FIG. 10.5(V)
Time offset: 0


DC OUTPUT VOLTAGE Vo1 VOLTS - PHI_0 -PI/(6) RADIANS
DC OUTPUT VOLTAGE Vo2 VOLTS - PHI_0 -PI/(6) RADIANS
FIG. 10.5(W)
Time offset: 0


DC OUTPUT VOLTAGE Vo1 VOLTS - PHI_0 -PI/(12) RADIANS
DC OUTPUT VOLTAGE Vo2 VOLTS - PHI_0 -PI/(12) RADIANS
FIG. 10.5(X)
Time offset: 0

is shown in Fig.10.6. The model is developed in SIMULINK [51]. Here Venturini algorithm for unity input phase displacement factor is assumed in generating the gate pulses for the bidirectional switches. Also three phase sine wave input and output voltages are used for developing the model. The above algorithm is proved valid for three phase sine wave input and output voltage in A3.3 Appendix in Chapter III. The model consists of a) Bidirectional switch gate pulse generator b) Output voltage phase angle varying device c) Three phase sine wave AC voltage source d) MC bidirectional switch matrix e) RLC output filter f) Two Separately Excited DC Motor Loads. The parameters used for the model excluding the two R-L loads are shown in Table 10.1. The parameters of the two separately excited DC Motors are shown in Table 10.4. In the model sub units given above, item a, c, d, and e have already been explained in Section 10.4 above.

The output voltage phase angle varying device is shown in Fig. 10.6. This is a multiport switch. The first port at the top is the control port and the remaining ports are data ports. Here the number of data ports are eight, numbered from top to bottom. The sequence generator connected to the control port has the numbers from one to eight at specified intervals of time. Depending on the number displayed at a specific time by the sequence generator, the input corresponding to that data port number appears at the output of the multiport switch. For example if the number at any time interval displayed by the sequence generator is six, then $8\pi/12$ appears at the output of multiport switch.

The two separately excited DC motors have parameters as shown in Table 10.4 [51]. The above DC motor model is shown in Fig. 10.7.

TABLE 10.4: DC Motors Parameters

Sl.No.	Parameters	DC Machine 1		DC Machine 2	
		Value	Unit	Value	Unit
1	Power Output	10	HP	5	HP
2	Rated Terminal Voltage	500	Volts	240	Volts
3	Speed	1750	RPM	1750	RPM
4	Field Voltage	300	Volts	300	Volts
5	Armature Resistance	4.712	Ohms	2.581	Ohms
6	Armature Inductance	0.0527	H	0.028	H
7	Field Resistance	180	Ohms	281.3	Ohms
8	Field Inductance	71.4	H	156	H
9	Field-Armature Mutual Inductance	1.345	H	0.9483	H
10	Total Inertia	0.0425	kg-m^2	0.0221	kg-m^2
11	Damping Coefficient	0.0034	Nw-m-s	0.0029	Nw-m-s

10.5.1 SIMULATION RESULTS: The simulation of the Dual Programmable AC to DC rectifier fed separately excited DC motors was carried out in SIMULINK [51]. The ode15s(Stiff/NDF) solver is used. At intervals of 0.2 seconds, the numbers from 1 to 8 are given as input to control port of multiport switch. The output of φ_O during this time intervals are $+\pi/12$, $+\pi/6$, $+\pi/4$, $+7\pi/12$, 0, $+2\pi/3$,

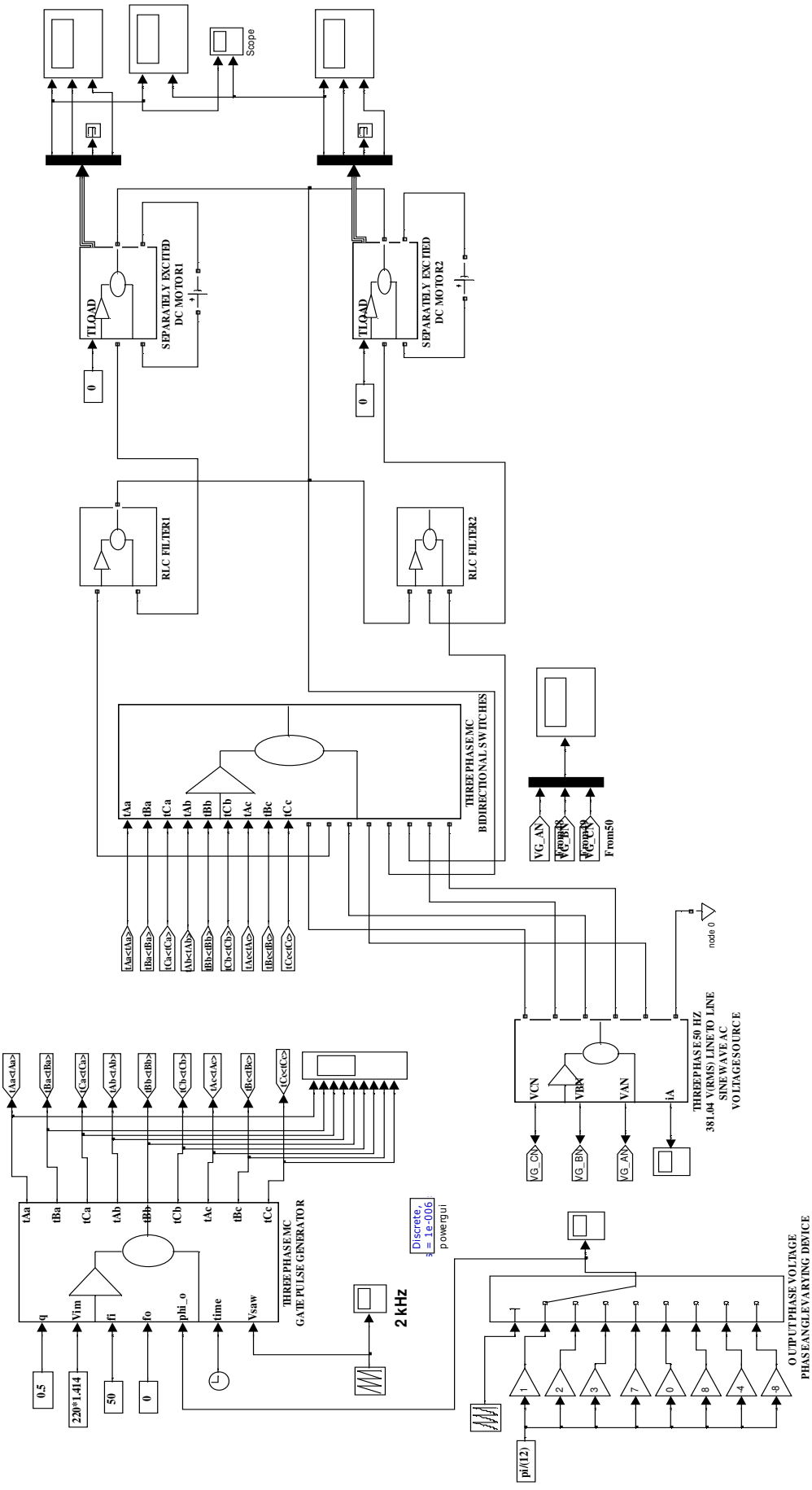


FIG. 10.6: MODEL OF DUAL PROGRAMMABLE AC TO DC RECTIFIER FED SEPARATELY EXCITED DC MOTORS

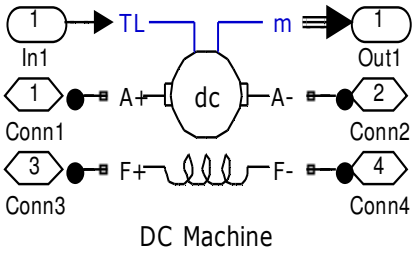
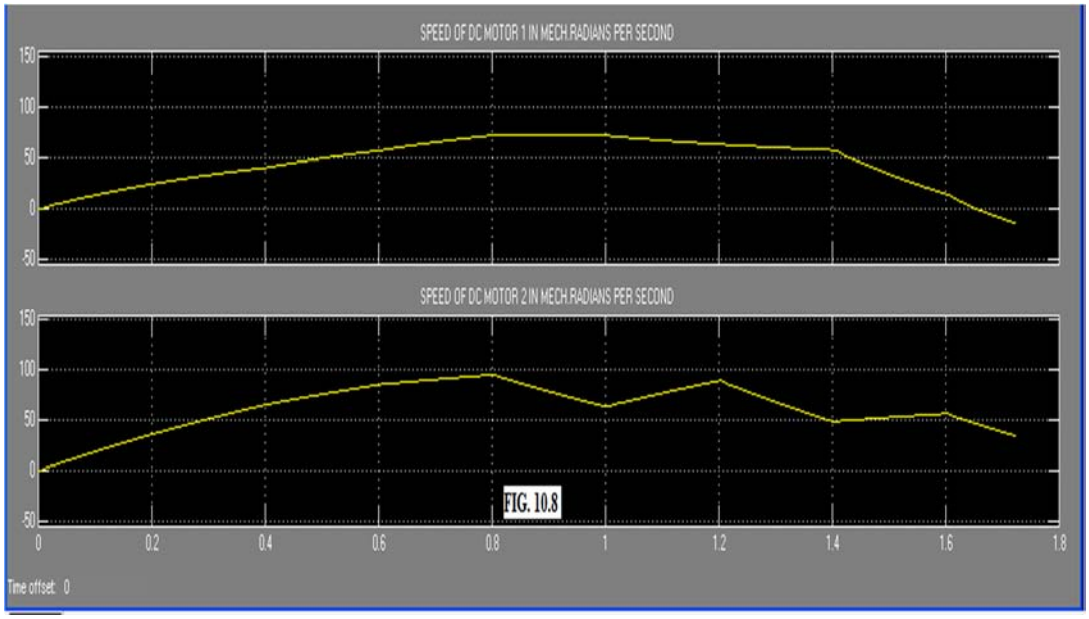
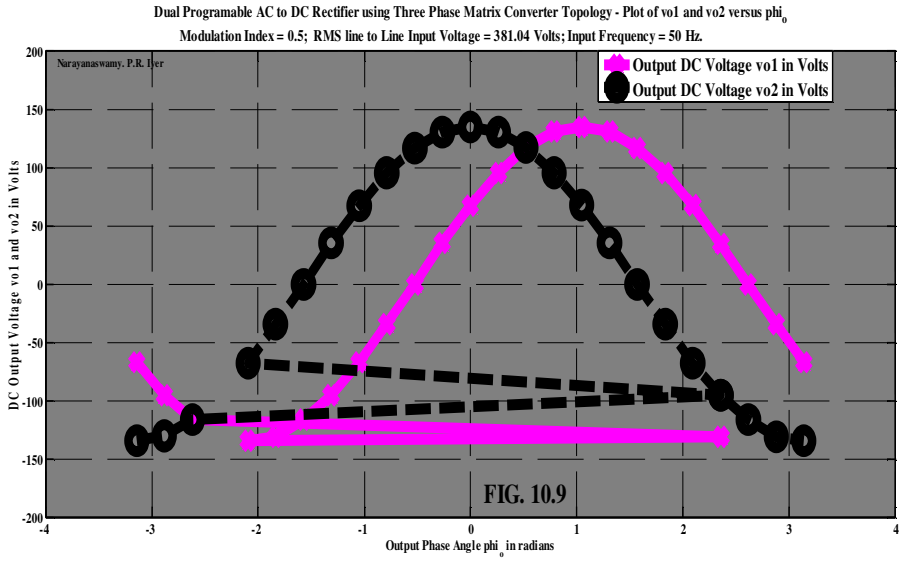


FIG. 10.7

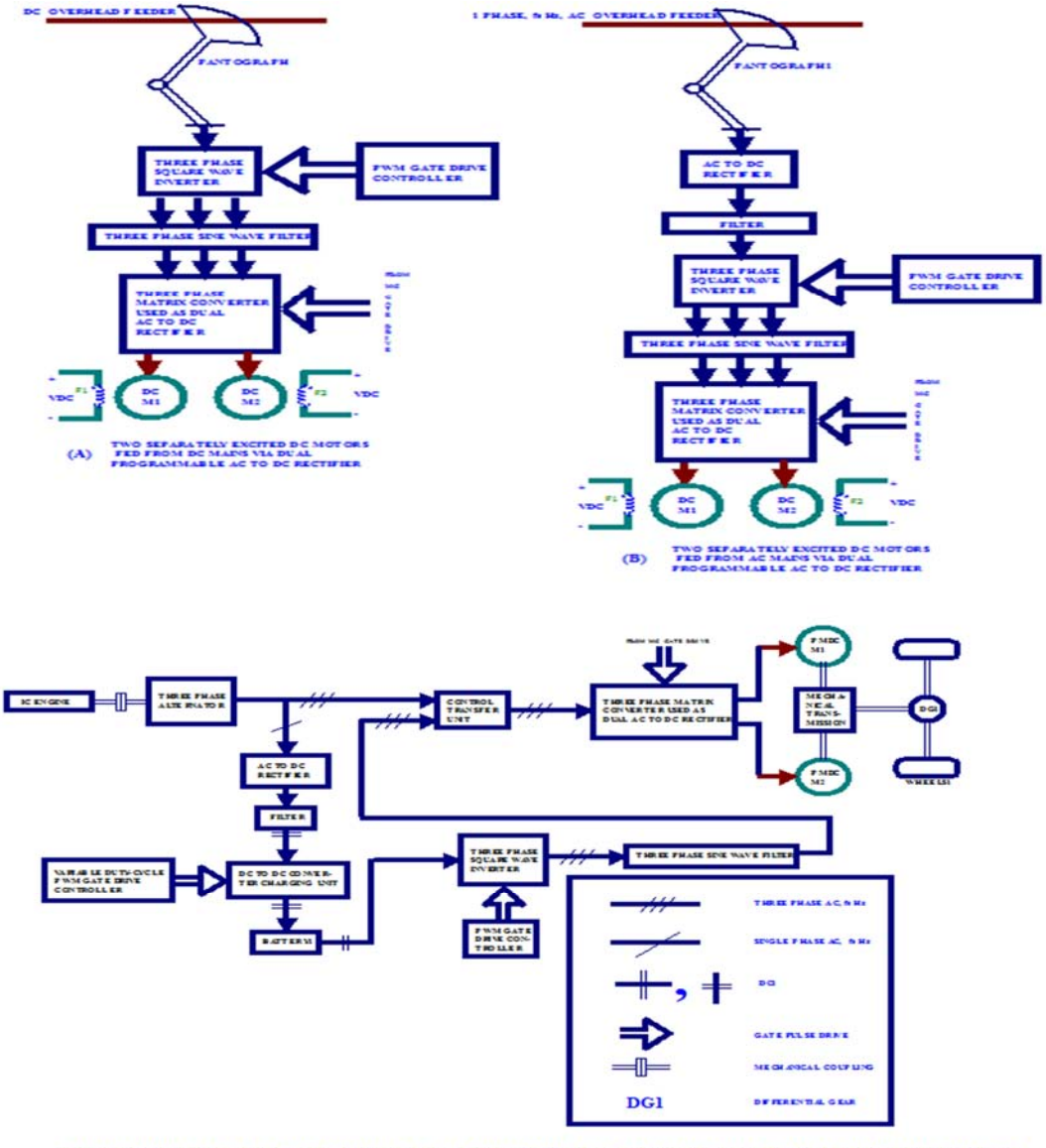
-π/3, -2π/3. The output voltage Vo1 and Vo2 for DC machines 1 and 2 can be obtained from Table 10.3. These values from Table 10.3 indicate that DC machine 1 is accelerating, decelerating,, coasting, and braking whereas DC machine 2 is accelerating, reduced acceleration or decelerating, braking, accelerating, braking, accelerating and braking. The simulation result for the motor speed of DC machines 1 and 2 is shown in Fig, 10.8 above, which confirm the above finding using Table 10.3. The variation of the two DC output voltages Vo1 and Vo2 with respect to φ_O is shown in Fig. 10.9.

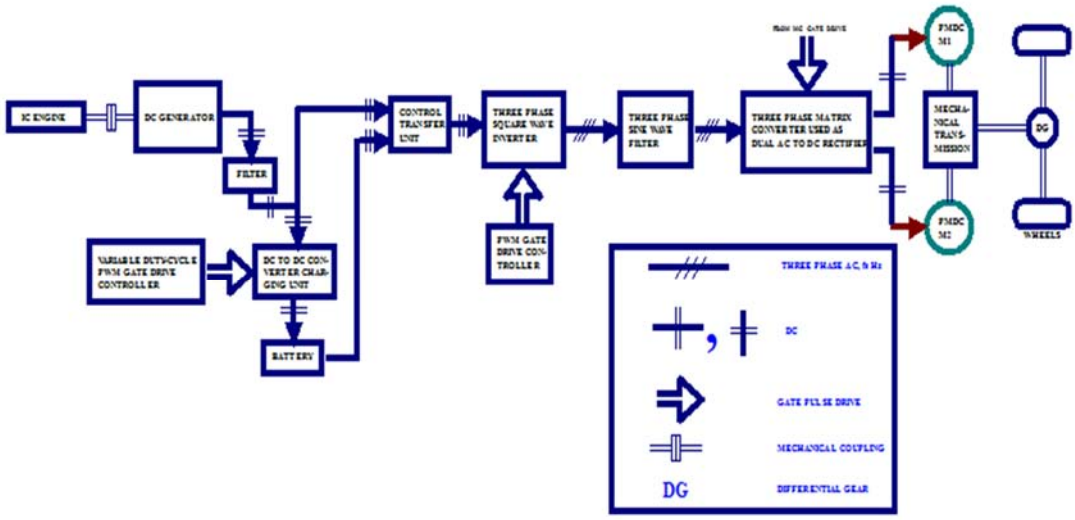




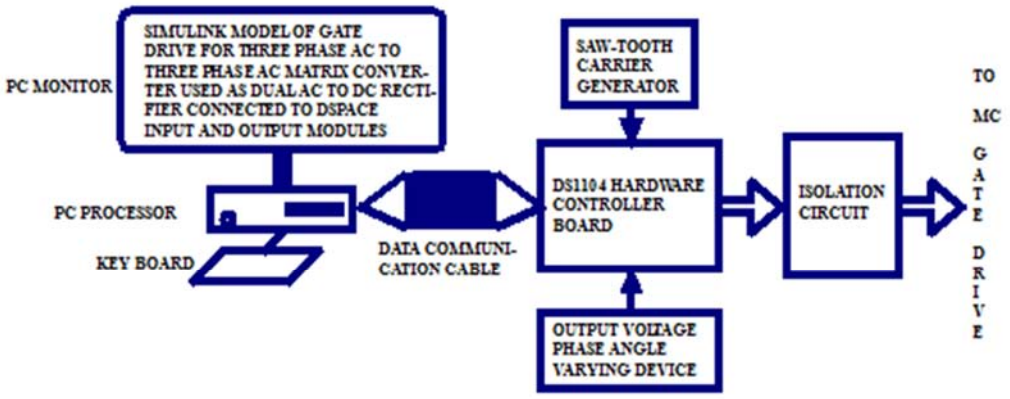
10.6 REAL TIME IMPLEMENTATION: Simulation results in Section 10.5.1 indicates that this Dual programmable AC to DC rectifier can be used for the speed control of either two separately excited DC motor drives or else two Permanent Magnet DC Motor Drives thus rendering them suitable for Hybrid Electric Vehicle [63] and Electric Traction applications. Some of these applications are highlighted in Fig. 10.10(A), (B), (C) and (D). The dSPACE implementation scheme of the gate drive for the bidirectional switches of the three phase MC used as Dual Programmable AC to DC rectifier is shown in Fig. 10.10(E).

Fig. 10.11 shows one method of developing a output voltage phase angle device using two op.amps. When the switch SS1 is thrown to A or B, the output of the first op.amp. will be $+\pi$ or $-\pi$ Volts respectively. The second op.amp. has 12E3 (12 K) Ohms as the input resistor and twelve 1E3 (1 K) Ohms in series as feedback resistor with tappings for each feedback resistor. By throwing the switch SS2 from position 1 to 12, output voltage in the range $\pm\pi/12$ to $\pm\pi$ can be obtained in steps of $\pm\pi/12$ Volts.





(D) TWO SEPARATELY EXCITED DC MOTORS FED BY DUAL PROGRAMMABLE AC TO DC RECTIFIER FROM DC GENERATOR



(E) SCHME FOR DSPACE IMPLEMENTATION

FIG. 10.10:

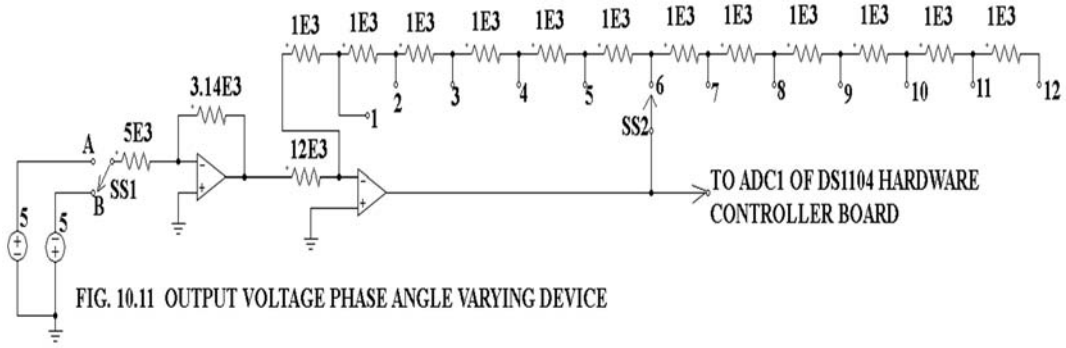


FIG. 10.11 OUTPUT VOLTAGE PHASE ANGLE VARYING DEVICE

Fig. 10.12 shows one of several methods of generating a 2 kHz saw-tooth carrier pulse with a peak value of 1 volt and minimum value of zero. The astable multi using NE555 by Texas Instruments generates a 2 kHz square pulse with peak value of 5 Volts, ON time of 495 microseconds and OFF

time of 5 microseconds. This output is compared using an Op.Amp. comparator with a +1 Volt DC voltage obtained using a +10 Volts power supply and potential divider. The output of this comparator

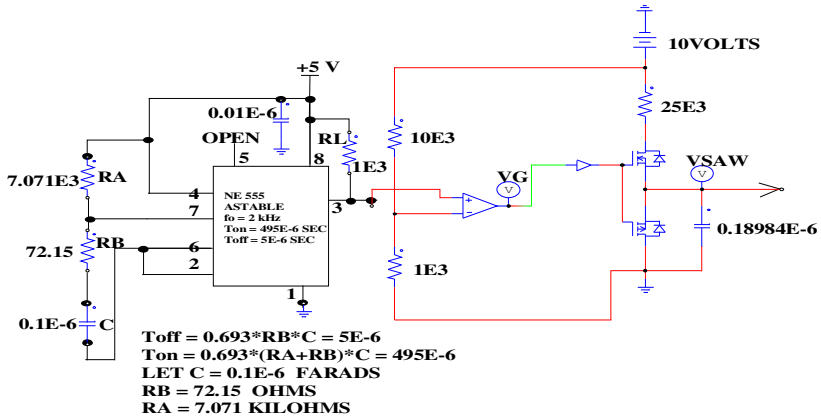
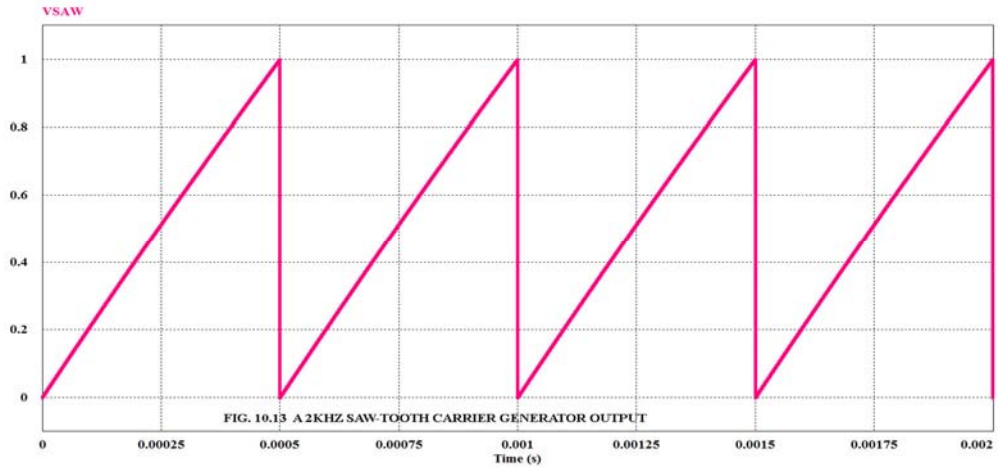


FIG. 10.12: A 2 KHz SAW-TOOTH CARRIER GENERATOR

drives a pair of N and P MOSFET switches in series with a 25 Kilohms resistor connected to the +10 Volts power supply. Across the P channel MOSFET switch a capacitor of 0.18984e-6 Farads capacitor is connected. The simulation Fig. 10.12 using PSIM with the NE555 astable multi replaced by a 2 kHz square clock pulse generator with ON and OFF duration of 495e-6 and 5e-6 seconds is shown in Fig. 10.13.

Another method of generating the 2 kHz saw-tooth carrier generator using PIC16F84A microcontroller is shown in Appendix I.



10.7 DISCUSSION OF RESULTS: Dual Programmable AC to DC rectifier is a new concept hitherto NOT reported in the literature references. The simulation results of the Dual Programmable AC to DC rectifier well agree with the theoretically computed results. As the dual DC output voltages varies in magnitude and takes both positive and negative values with the variation of output voltage phase angle φ_O, this method is suitable for speed control, acceleration and braking of Separately Excited DC Motors and Permanent magnet DC Motors. Practical applications for HEV[63] and Electric traction are highlighted. One method of implementing the above rectifier in real time using dSPACE is shown. Although only one simulation result is shown in Fig. 10.8 for one set of output

voltage phase angle φ_O value, it is possible to have number of combination of φ_O values to suit the individual requirement. By looking at Fig. 10.9, it is possible to select the output phase angle φ_O required for either acceleration or deceleration or braking of the two DC motors. This Dual Programmable AC to DC rectifier is sure to find applications involving the speed control of Separately Excited DC Motors and Permanent Magnet DC Motors such as in Hybrid Electric Vehicles (HEVs)[63] and in Electric Traction.

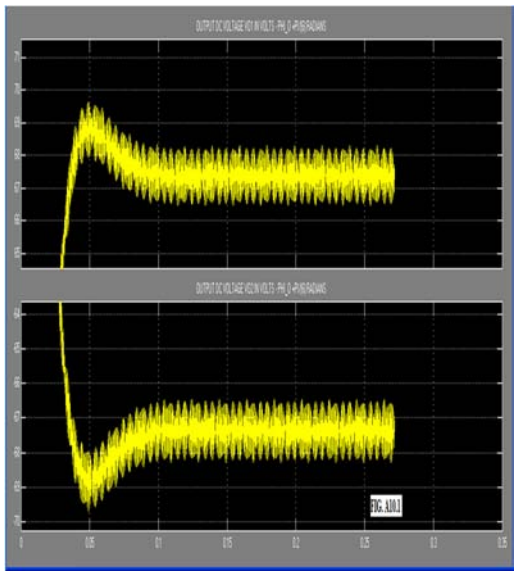
10.8 CONCLUSIONS: A novel concept of Dual Programmable AC to DC rectifier using three phase AC to three phase AC MC topology is presented in this chapter. Simulation results and theoretically computed values closely well agree. Venturini algorithm for the maximum output voltage magnitude of direct AC to AC converter forms the basis for the behaviour of dual programmable AC to DC rectifier. The proposed scheme can be implemented in real time as this has applications in the speed control, acceleration and breaking by plugging of separately excited DC motor and Permanent Magnet DC Motor.

A10.1 APPENDIX: Equations 10.12 and 10.13 are derived using three phase cosine wave input and output voltages. The three phase source used is from the Electrical Source library in the SimPowerSystems blockset of SIMULINK. Here in the box corresponding to Phase Angle of Phase A (degrees), a value of 90 is entered. All other boxes are filled with appropriate values as used in the above model. The simulation results obtained for various values of φ_O are tabulated in Table A10.1. The plot of vo1 and vo2 for a φ_O of $+\pi/6$ radians is shown in Fig. A10.1. From Fig. A10.1 it is clear that for the output voltage phase angle φ_O of $+\pi/6$ radians, simulation results for Vo1 and Vo2 are +67.5 Volts and -67.5 Volts respectively which closely agree with the theoretically computed value given in Table A10.1.

TABLE A10.1 : Theoretically Computed Values

q = 0.5, Vim = (220*1.414) Volts, fi = 50 Hz.

Sl.No.	φ_O radians	V_{O1} Volts	V_{O2} Volts
1	0	116.64	0
2	$+\pi/6$	67.34	-67.34
3	$+\pi/4$	34.86	-95.24
4	$+\pi/3$	0	-116.64
5	$+\pi/2$	-67.34	-134.69
7	$+2\pi/3$	-116.64	-116.64
8	$+5\pi/6$	-134.69	-67.34
9	$\pm\pi$	-116.64	0
10	$-5\pi/6$	-67.34	67.34
11	$-2\pi/3$	0	116.64
12	$-\pi/2$	67.34	134.69
13	$-\pi/3$	116.64	116.64
14	$-\pi/4$	130.1	95.24
15	$-\pi/6$	134.69	67.34



Chapter XI

Delta-Sigma Modulation of Three Phase AC to Three Phase AC Matrix Converter

11.1 INTRODUCTION: Matrix converter directly converts the AC input voltage at any given frequency to AC output voltage with arbitrary amplitude at any unrestricted frequency without the need for a dc link capacitor storage element at the input side. Since inception, several carrier based modulation techniques have been proposed for matrix converter. All these techniques use either a saw-tooth carrier[1-8] or a triangle carrier voltage signal[13-14, 16-17] to be compared with modulation voltage signals to generate gate switching pulses for the bidirectional switches of matrix converter. These modulation voltage signals are generated using Venturini algorithm [1-5] or using other recently proposed algorithms [11-14, 16-17]. This chapter examines the recently proposed delta-sigma modulation technique for matrix converter [46-49]. A model of the three phase AC to three phase AC matrix converter (MC) using delta-sigma modulation technique is developed in SIMULINK [51]. Both Venturini[1-5] as well as advanced modulation algorithm [13-14, 16-17] are used for generating the modulation voltage signals. Simulation is carried out for a given sampling frequency. It is seen from simulation results that voltage harmonic peaks are reduced at integral multiples of sampling frequency[46-48]. Also simulation of three phase Induction Motor (IM) fed by MC using delta-sigma modulation is presented. The delta-sigma modulation technique can reduce noise peaks in the output voltage as compared to conventional PWM technique and has the advantage of maintaining noise regulation.

11.2 REVIEW OF MATRIX CONVERTER GATE PULSE GENERATION: The three phase AC to three phase MC is shown in Fig. 3.1 of Chapter III. Gate pulses for three phase matrix converter bidirectional switches have to be generated to comply with some specific requirement. Referring to Fig. 3.1 of Chapter III, it is seen that if two or more bidirectional switches connected to same output phase such as SAa, SBa and SCa are turned ON simultaneously, there will be a dead short circuit. These gate pulses have to be on in sequence, one after the other. Also it is required that one of the above bidirectional switches should remain closed. This is achieved by carrier PWM technique [1-5] and also by Delta-Sigma modulation technique [46-48].

11.2.1 SAW-TOOTH CARRIER PWM TECHNIQUE: In carrier PWM technique, the nine modulation functions defined in equation 3.17 of Chapter III are developed using Embedded MATLAB Function in SIMULINK [51]. These are then compared with a saw-tooth carrier voltage signal using comparators and the resulting output is given to logic gates. The method of generating the gate pulses for output phase a is shown in Fig. 11.1(A). Gate pulses tAa, tBa and tCa correspond to bidirectional switches SAa, SBa and SCa respectively. Similar hardware circuit applies to output phase b and c.

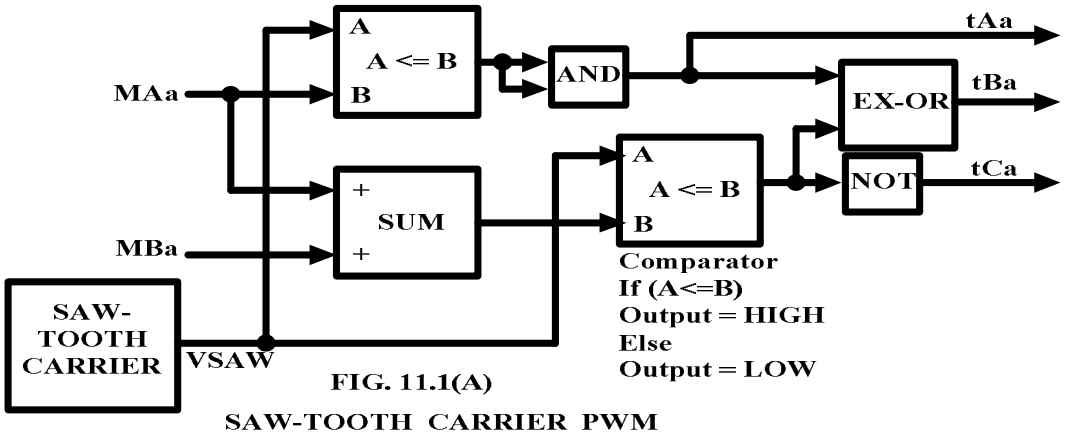


FIG. 11.1(A)

SAW-TOOTH CARRIER PWM

11.2.2 TRIANGLE CARRIER PWM TECHNIQUE: In triangle carrier PWM, the nine modulation functions defined in equation 4.40 of Chapter IV are derived using Embedded MATLAB Function in SIMULINK [51]. These are then compared with a triangle carrier voltage signal using comparators and the resulting output is given to logic gates. The method of generating the gate pulses for output phase a is shown in Fig. 11.1(B). Gate Pulses tAa, tBa and tCa correspond to bidirectional switches SAa, SBa and SCa respectively. Similar hardware circuit applies to output phase b and c.

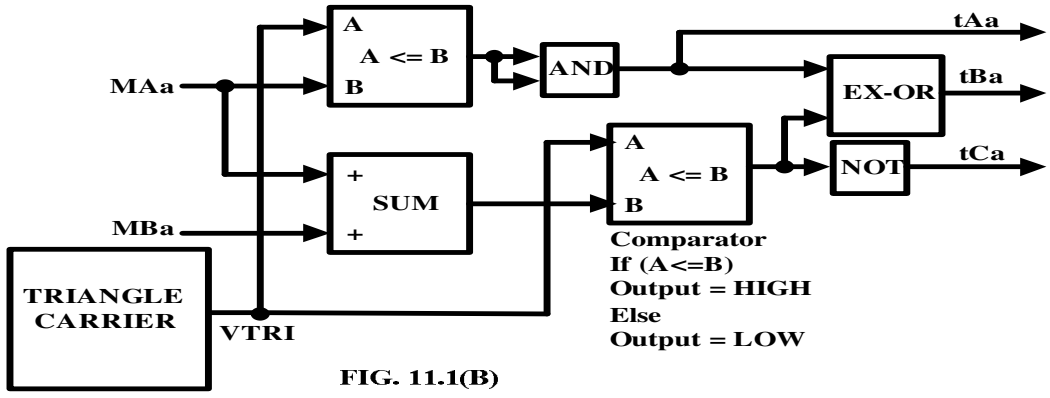


FIG. 11.1(B)

TRIANGLE CARRIER PWM

11.2.3 DELTA-SIGMA PWM TECHNIQUE: This is a recently proposed technique for three phase Matrix Converters [46-48]. In Delta-Sigma modulation high frequency noise peaks in the output voltages due to switching operation does not occur and this becomes an advantage for clearing noise regulations [46-48]. Fig. 11.1(C) and (D) shows the first order Delta-Sigma modulator [49]. Analysis of Fig. 11.1(C) gives the following:

$$X(z) - z^{-1} * Y(z) + z^{-1} * E(z) = E(z) \qquad (11.1)$$

Analysis of Fig. 11.1(D) gives the following:

$$X(z) - z^{-1} * Y(z) + z^{-1} * E(z) = E(z) \qquad (11.2)$$

In sample time, equations 11.1 and 11.2 can be expressed as follows:

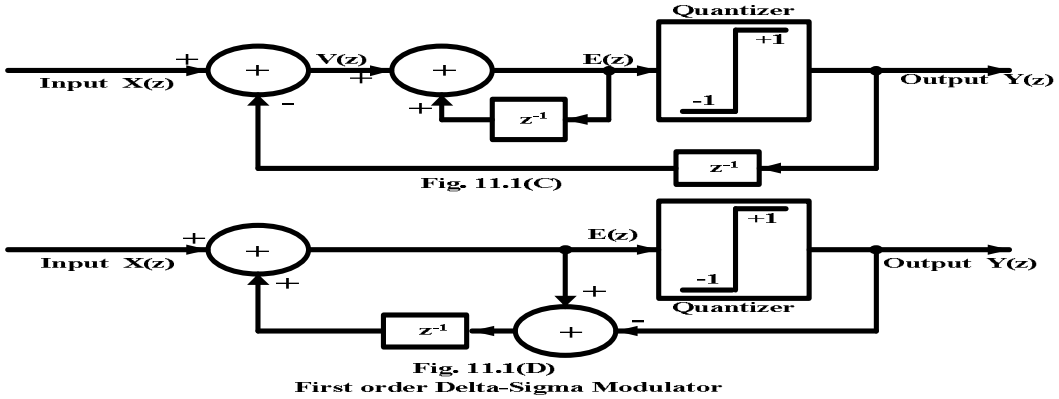
$$x(k) - y(k-1) + e(k-1) = e(k) \qquad (11.3)$$

Equations 11.1 and 11.2 agree well and there for Fig. 11.1(C) and (D) are identical.

Quantizer characteristics can be expressed as follows:

$$y(k) = sgn[e(k)] \qquad (11.4)$$

The quantizer output is +1 if its input exceeds the threshold and -1 if its input is below threshold value. The quantizer output is used to control the bidirectional switches.



11.3 DELTA-SIGMA MODULATOR INTERFACE: This section discusses the implementation aspects of a Delta-Sigma modulator for a three phase matrix converter. The Delta-Sigma modulator for the output phase a of three phase matrix converter is shown in Fig. 11.2. Similar circuit applies to output phase b and c of the matrix converter. In Fig. 11.2, the quantizer output is given to comparator. The comparator output is HIGH when its input greater than or equal to zero, else the output is LOW

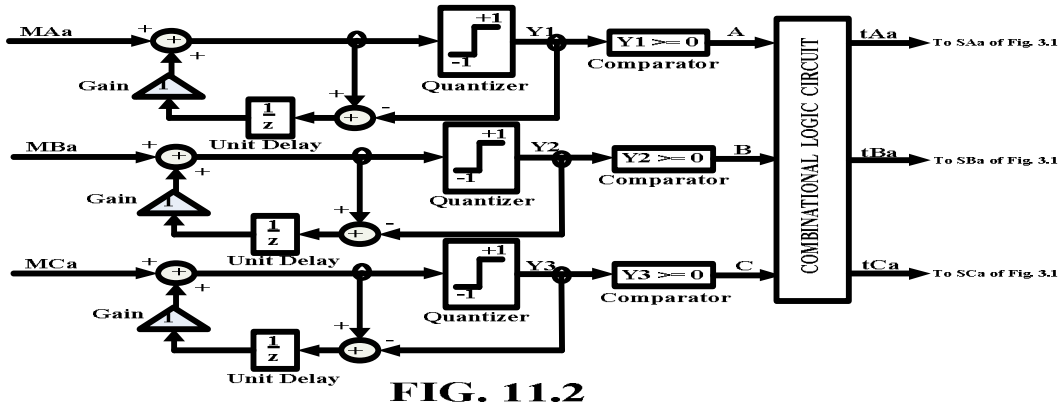


FIG. 11.2

Delta-Sigma Modulator for Output Phase a of Three Phase Matrix Converter

The comparator outputs A, B and C form the input to the combinational logic circuit which generates the gate pulse for the bidirectional switches. The combinational logic circuit must be so designed to comply with the gate drive requirement specified under section 11.2 above. Table 11.1 shows one method of generating the gate pulse for the bidirectional switches connected to output phase a. Gate pulse tAa, tBa and tCa can be expressed as follows:

TABLE 11.1: Digital Logic Interface Truth Table

	Inputs			Outputs		
Sl. No.	A	B	C	tAa	tBa	tCa
1	0	0	0	1	0	0
2	0	0	1	0	0	1
3	0	1	0	0	1	0
4	0	1	1	0	1	0
5	1	0	0	1	0	0
6	1	0	1	0	0	1
7	1	1	0	1	0	0
8	1	1	1	1	0	0

$$tAa = (A \cap B) \cup (\overline{B} \cap \overline{C}) \qquad (11.5)$$

$$tBa = (\overline{A} \cap B) \qquad (11.6)$$

$$tCa = (\overline{B} \cap C) \qquad (11.7)$$

Gate pulse expressions for bidirectional switches connected to output phase b and c can be expressed as follows:

$$tAb = \left(D \cap \overline{F}\right) \qquad (11.8)$$

$$tBb = \left(\overline{D} \cap \overline{F}\right) \cup (E \cap F) \qquad (11.9)$$

$$tCb = \left(\overline{E} \cap F\right) \qquad (11.10)$$

$$tAc = \left(G \cap \overline{I}\right) \qquad (11.11)$$

$$tBc = \left(\overline{G} \cap H\right) \qquad (11.12)$$

$$tCc = (G \cap I) \cup \left(\overline{G} \cap \overline{H}\right) \qquad (11.13)$$

In equations 11.5 to 11.13, the symbols $\cap, \cup, -$ represent logical AND, OR and NOT operation respectively. For the output phase b and c, inputs to delta-sigma modulator in Fig. 11.2, MAa, MBa and MCa are replaced by MAb, MBb, MCb and MAc, MBc, MCc respectively. Similarly the inputs A, B, C to the combinational logic circuit in Fig. 11.2 are replaced by D, E, F for output phase b and G, H, I for output phase c for the sake of clarity.

11.4 VENTURINI MODEL OF THREE PHASE MATRIX CONVERTER USING DELTA-SIGMA MODULATION: The Venturini model of the three phase AC to three phase AC MC using delta-sigma modulation is shown in Fig. 11.3. The Embedded MATLAB Function generates the nine modulation duty-cycles as defined in equation 3.17 of Chapter III. These nine modulation functions are applied as inputs to first order Delta-Sigma modulators as shown in Fig. 11.2. The combinational logic interface are designed as described in Section 11.3 above. The principle of operation of the Delta-Sigma modulator is explained in Section 11.2.3 above. The nine gate pulses from the output of combinational logic circuit is applied to the respective gates of the bidirectional switches.

11.4.1 SIMULATION RESULTS: The simulation of the delta-sigma modulated MC shown in Fig. 11.3 was carried out using SIMULINK [51]. The simulation parameters are shown in Table 11.2.

TABLE 11.2: Delta-Sigma Modulated PH3 AC to PH3 AC MC – SIMULINK Model Parameters

Sl.No.	Parameter	Value	Unit
1)	RMS Line to Neutral Input Voltage	220	Volts
2)	Input Frequency	50	Hz
3)	Output Frequency	50, 10	Hz
4)	Sampling Frequency	5	kHz
5)	Modulation Index	0.5	---
6)	RL Load	50, 0.5	Ω, H
7)	Output RLC Filter	10, 1e-3, 1.0132e-006	Ω, H, F

The ode15s(Stiff/NDF) solver was used. The simulation results for the harmonic spectrum of line to neutral output voltage, input current, load current and line to line output voltage and their respective oscilloscope waveforms for an output frequency of 50 Hz are shown in Fig. 11.4(A) to (D) and Fig. 11.5(A) to (D) respectively. The same harmonic spectrum and waveforms in the above order for an output frequency of 10 Hz are shown in Fig. 11.6(A) to (D) and Fig. 11.7(A) to (D) respectively. The simulation results are tabulated in Table 11.3.

TABLE 11.3: SIMULINK Model Simulation Results

Sl.No.	Frequency Input-Output Hz	Line to Neutral Output voltage THD (p.u.)	Line to Line Output Voltage THD (p.u.)	Input current THD (p.u.)	Load current THD (p.u.)
1)	50 – 50	1.14	1.195	1.198	0.1155
2)	50 – 10	2.36	2.22	1.165	0.449

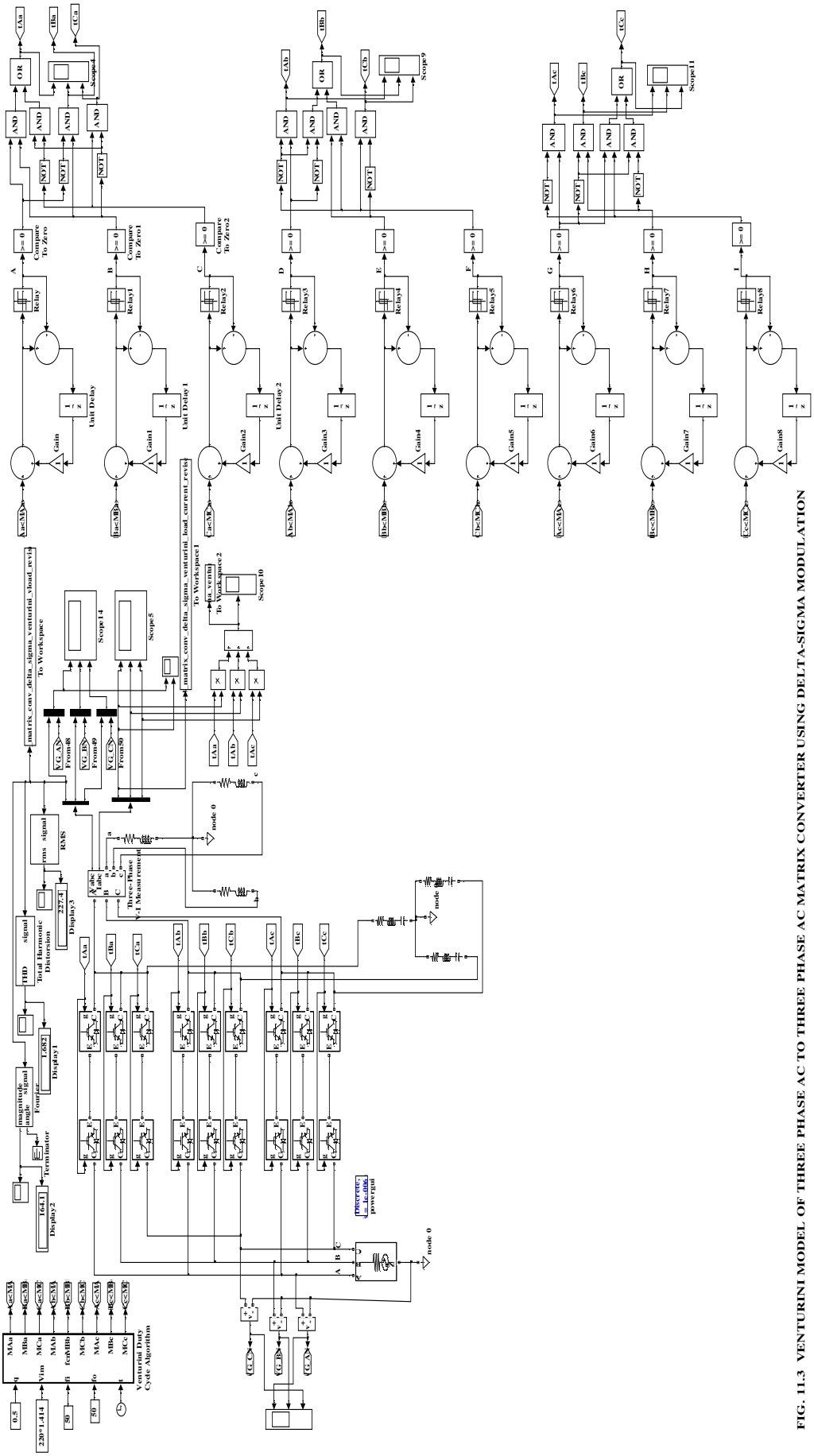


FIG. 11.3 VENTURINI MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING DELTA-SIGMA MODULATION

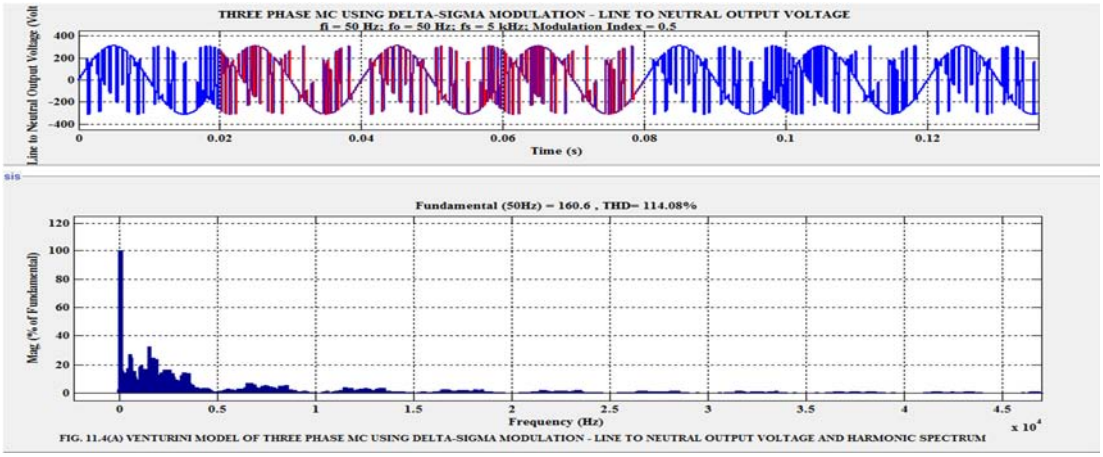


FIG. 11.4(A) VENTURINI MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM

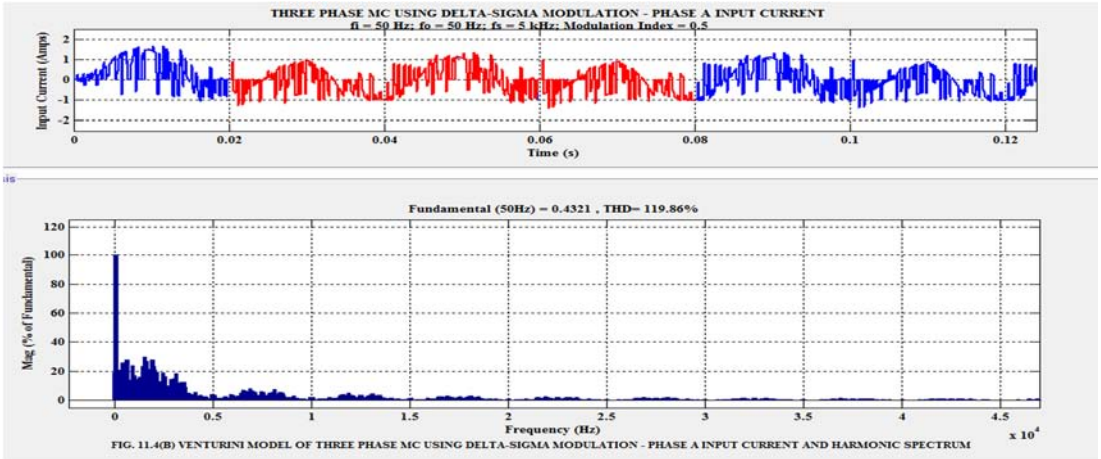


FIG. 11.4(B) VENTURINI MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - PHASE A INPUT CURRENT AND HARMONIC SPECTRUM

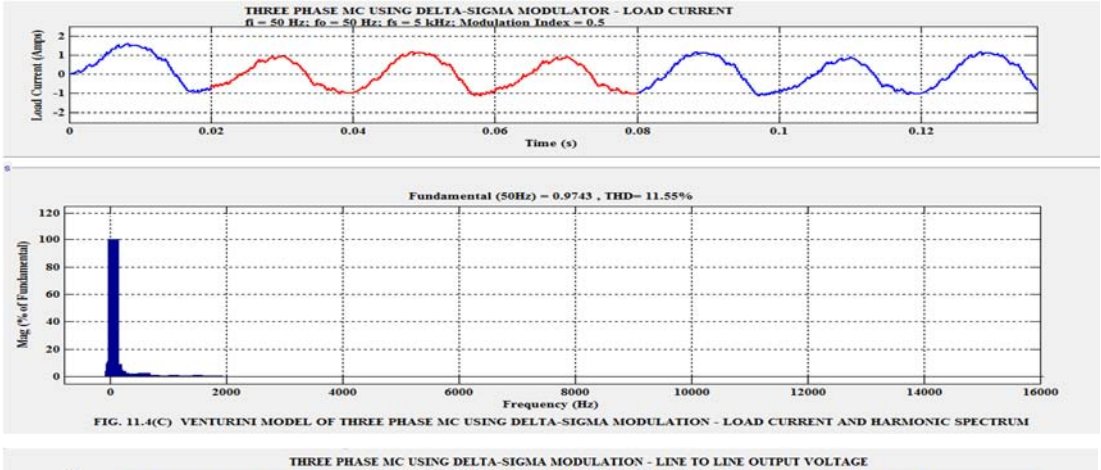


FIG. 11.4(C) VENTURINI MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - LOAD CURRENT AND HARMONIC SPECTRUM

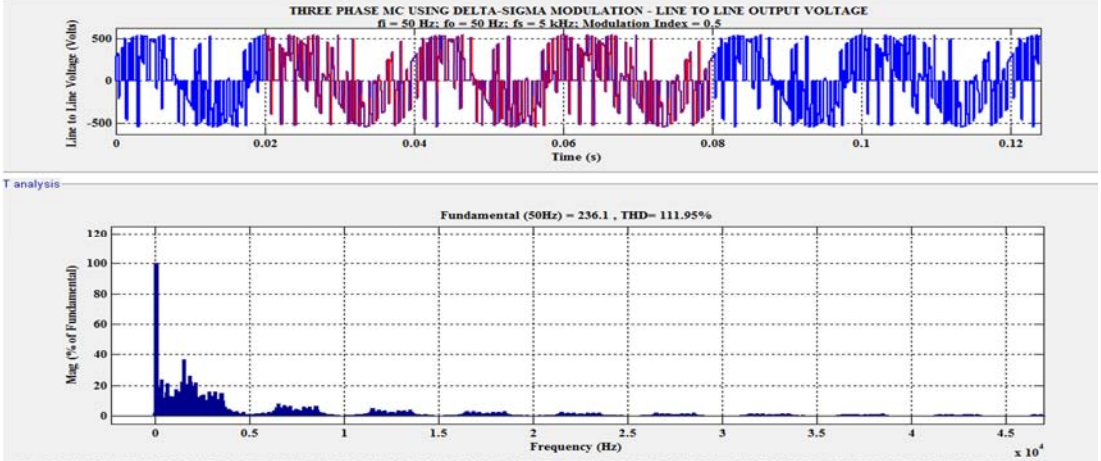
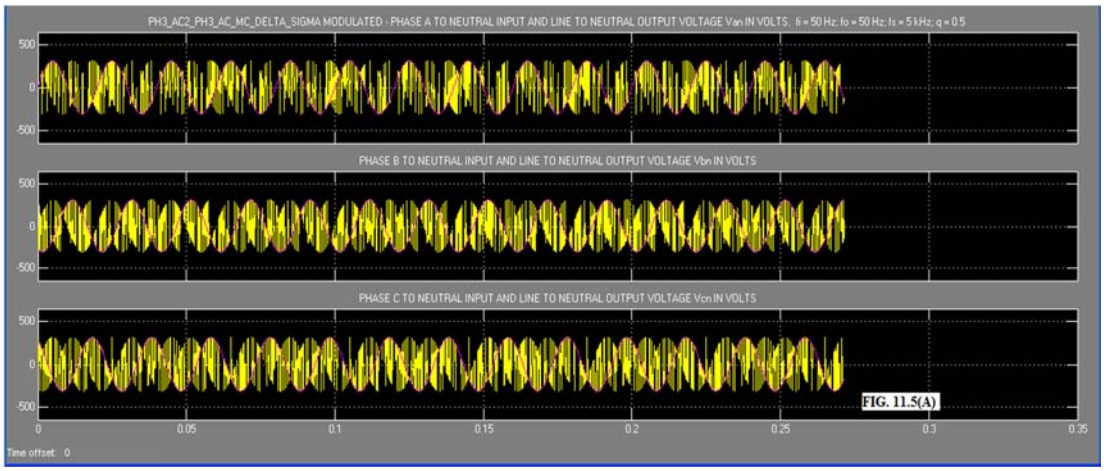
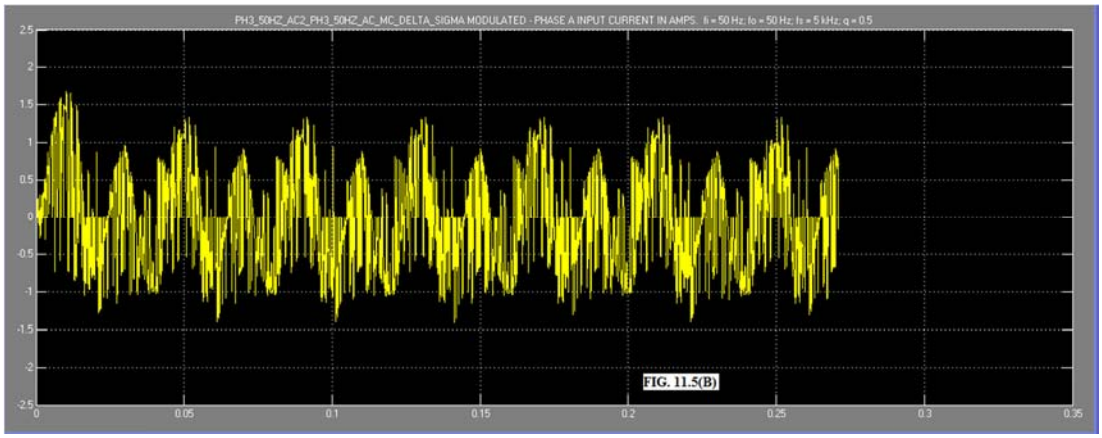
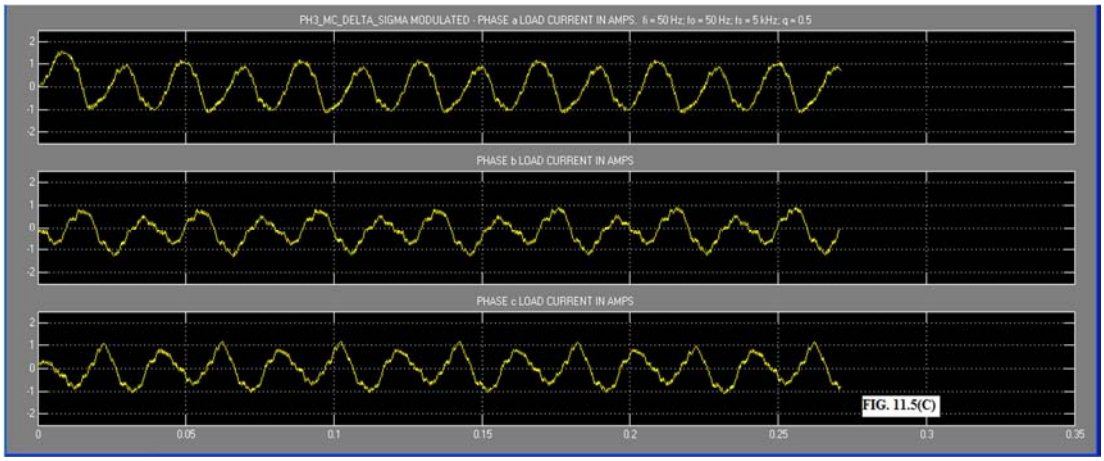
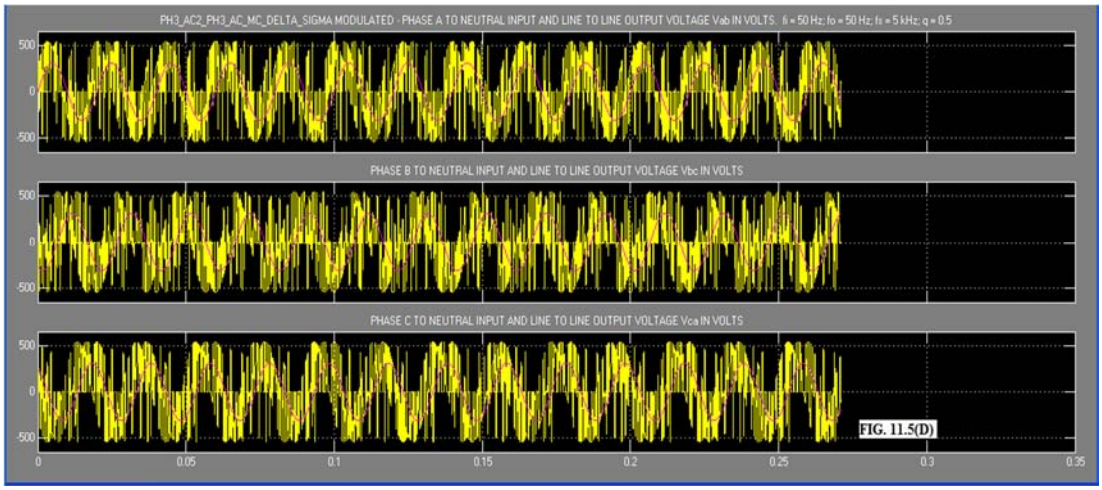


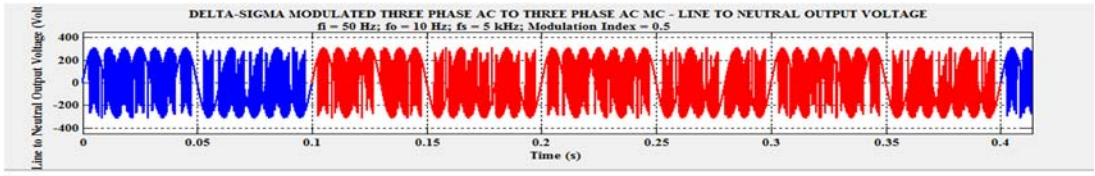
FIG. 11.4(D) VENTURINI MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM


PH3_AC2_PH3_AC_MC_DELTA_SIGMA MODULATED - PHASE A TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Van IN VOLTS. fi = 50 Hz; fo = 50 Hz; fs = 5 kHz; q = 0.5
PHASE B TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vbn IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vcn IN VOLTS
FIG. 11.5(A)
Time offset: 0


PH3_50HZ_AC2_PH3_50HZ_AC_MC_DELTA_SIGMA MODULATED - PHASE A INPUT CURRENT IN AMPS. fi = 50 Hz; fo = 50 Hz; fs = 5 kHz; q = 0.5
FIG. 11.5(B)


PH3_MC_DELTA_SIGMA MODULATED - PHASE a LOAD CURRENT IN AMPS. fi = 50 Hz; fo = 50 Hz; fs = 5 kHz; q = 0.5
PHASE b LOAD CURRENT IN AMPS
PHASE c LOAD CURRENT IN AMPS
FIG. 11.5(C)


PH3_AC2_PH3_AC_MC_DELTA_SIGMA MODULATED - PHASE A TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vab IN VOLTS. fi = 50 Hz; fo = 50 Hz; fs = 5 kHz; q = 0.5
PHASE B TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vbc IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vca IN VOLTS
FIG. 11.5(D)



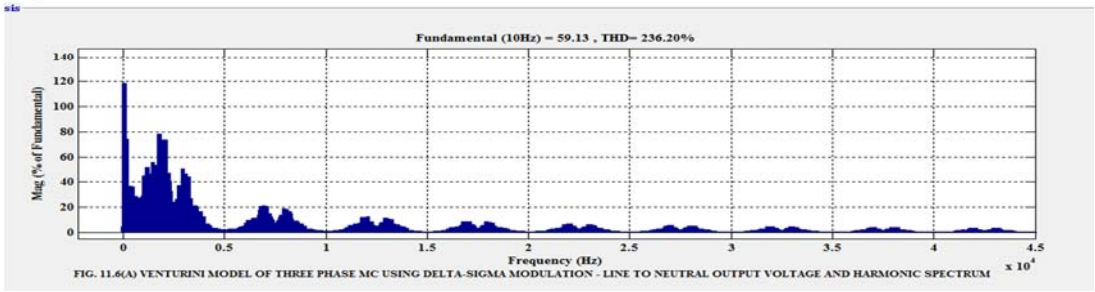
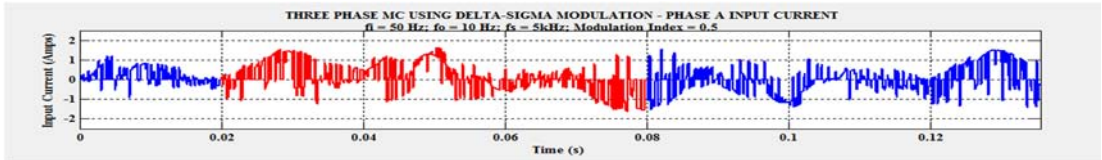


FIG. 11.6(A) VENTURINI MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM



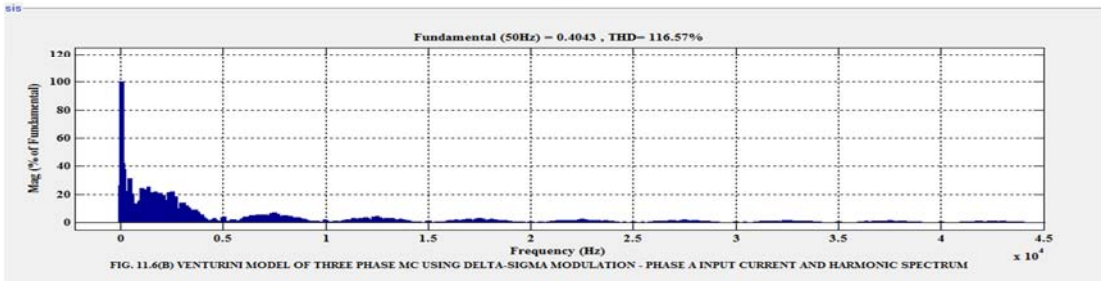
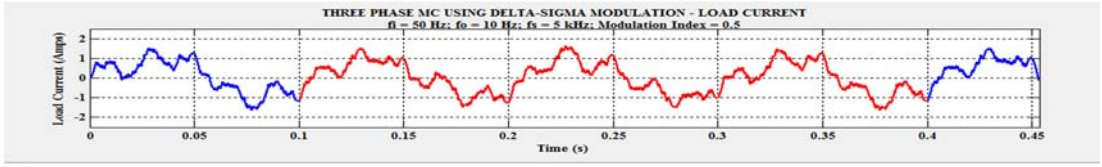


FIG. 11.6(B) VENTURINI MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - PHASE A INPUT CURRENT AND HARMONIC SPECTRUM



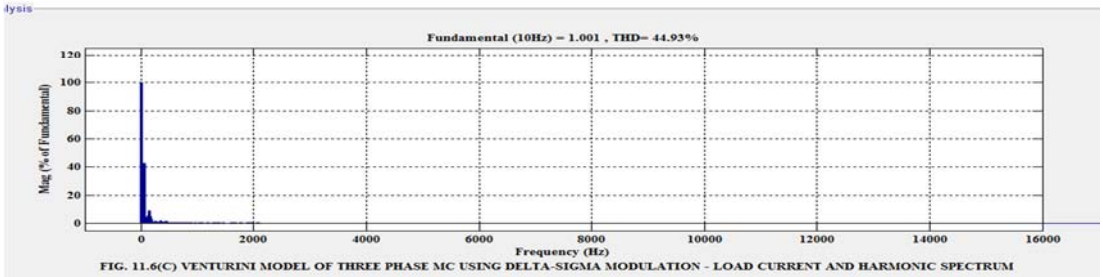
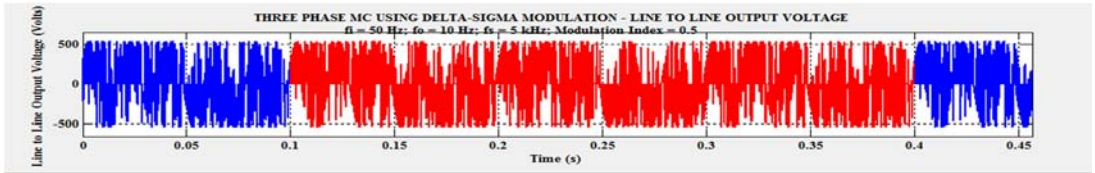


FIG. 11.6(C) VENTURINI MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - LOAD CURRENT AND HARMONIC SPECTRUM



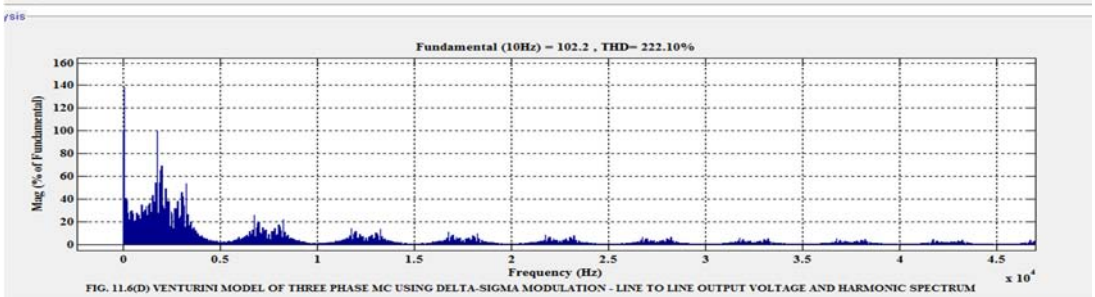
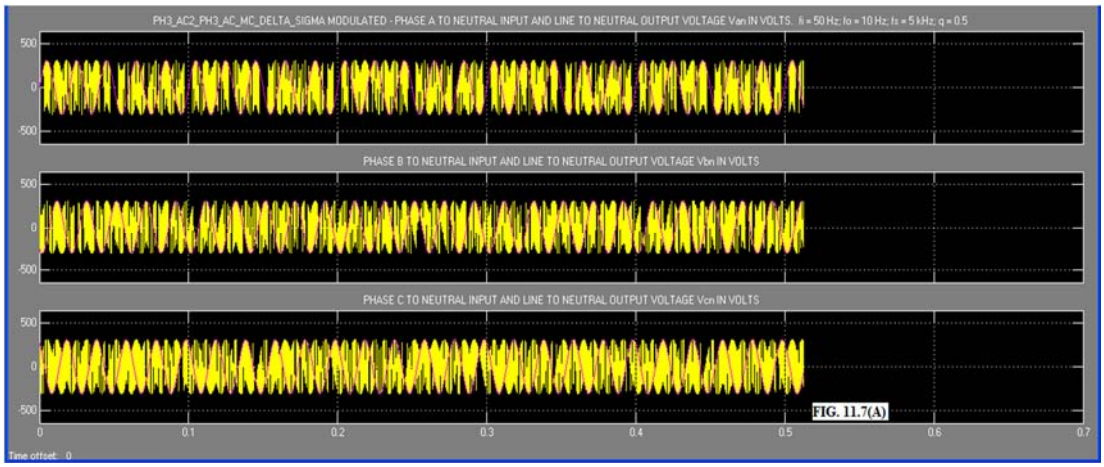
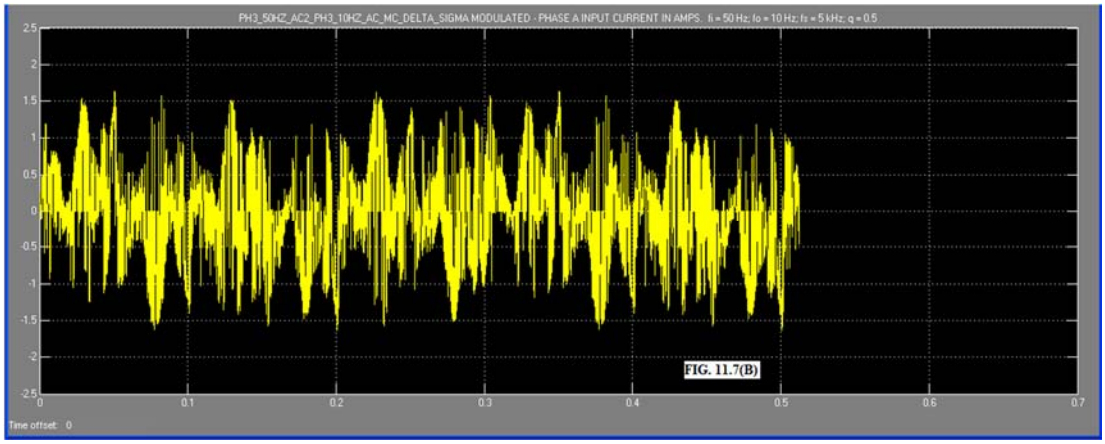
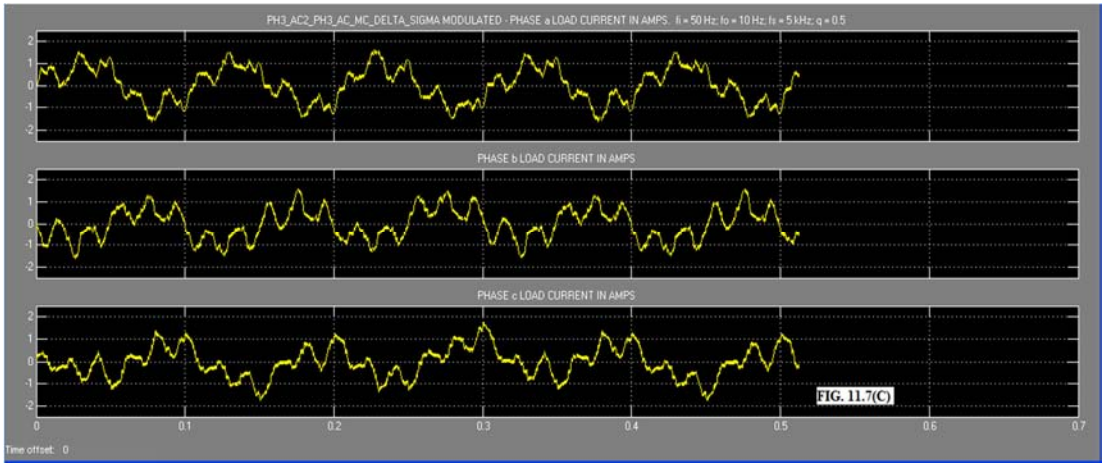
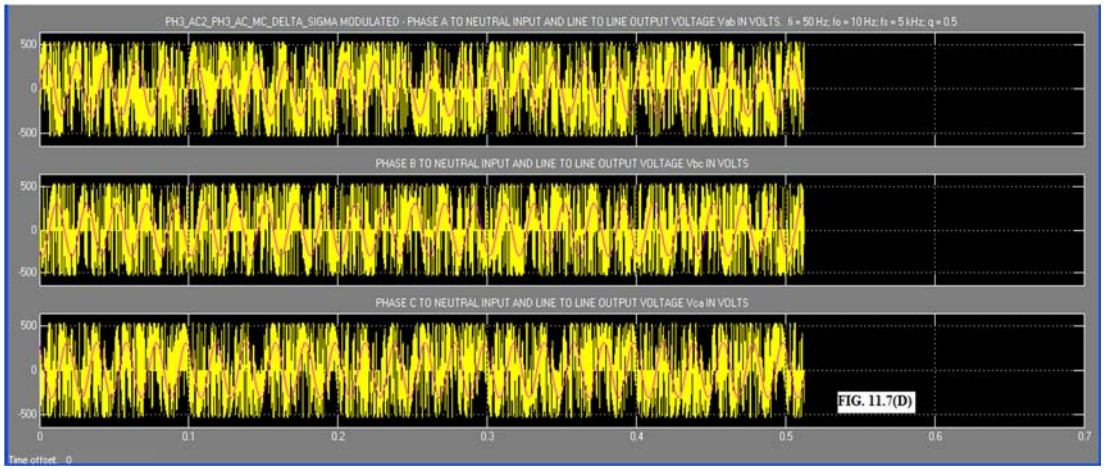


FIG. 11.6(D) VENTURINI MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM


PH3_AC2_PH3_AC_MC_DELTA_SIGMA MODULATED - PHASE A TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Van IN VOLTS. fi = 50 Hz; fo = 10 Hz; fs = 5 kHz; q = 0.5
PHASE B TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vbn IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vcn IN VOLTS
FIG. 11.7(A)
Time offset: 0


PH3_50HZ_AC2_PH3_10HZ_AC_MC_DELTA_SIGMA MODULATED - PHASE A INPUT CURRENT IN AMPS. fi = 50 Hz; fo = 10 Hz; fs = 5 kHz; q = 0.5
FIG. 11.7(B)
Time offset: 0


PH3_AC2_PH3_AC_MC_DELTA_SIGMA MODULATED - PHASE a LOAD CURRENT IN AMPS. fi = 50 Hz; fo = 10 Hz; fs = 5 kHz; q = 0.5
PHASE b LOAD CURRENT IN AMPS
PHASE c LOAD CURRENT IN AMPS
FIG. 11.7(C)
Time offset: 0


PH3_AC2_PH3_AC_MC_DELTA_SIGMA MODULATED - PHASE A TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vab IN VOLTS. fi = 50 Hz; fo = 10 Hz; fs = 5 kHz; q = 0.5
PHASE B TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vbc IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vca IN VOLTS
FIG. 11.7(D)
Time offset: 0

11.5 ADVANCED MODEL OF THREE PHASE MATRIX CONVERTER USING DELTA-SIGMA MODULATION: A novel carrier-based modulation scheme is proposed which requires no sector information and look-up table to calculate duty ratios, with output voltage amplitude 0.866 times that of the input voltage and the input power factor controllable [13, 16-17]. This has already been explained under section 4.4 of Chapter IV. The advanced model of the MC using delta-sigma modulation technique is shown in Fig. 11.8. The Embedded MATLAB Function along with the min and max block generates the nine modulation duty-cycles as defined in equation 4.40 of Chapter IV. These nine modulation functions are applied as inputs to first order Delta-Sigma modulators as shown in Fig. 11.2. The combinational logic interface are designed as described in section 11.3 above. The principle of operation of the Delta-Sigma modulator is explained in Section 11.2.3 above. The nine gate pulses from the output of combinational logic circuit is applied to the respective gates of the bidirectional switches.

11.5.1 SIMULATION RESULTS: The simulation of the delta-sigma modulated MC shown in Fig. 11.8 was carried out using SIMULINK [51]. The simulation parameters are shown in Table 11.4.

TABLE 11.4: Delta-Sigma Modulated PH3 AC to PH3 AC MC – Advanced Model Parameters

Sl.No.	Parameter	Value	Unit
1)	RMS Line to Neutral Input Voltage	220	Volts
2)	Input Frequency	50	Hz
3)	Output Frequency	50, 10	Hz
4)	Sampling Frequency	5	kHz
5)	Modulation Index k	0.26667	---
6)	RL Load	50, 20E-3	Ω, H
7)	Output RLC Filter	10, 1e-3, 1.0132e-006	Ω, H, F

The ode15s(Stiff/NDF) solver was used. The simulation results for the harmonic spectrum of line to neutral output voltage, input current, load current and line to line output voltage and their respective oscilloscope waveforms for an output frequency of 50 Hz are shown in Fig. 11.9(A) to (D) and Fig. 11.10(A) to (D) respectively. The same harmonic spectrum and waveforms in the above order for an output frequency of 10 Hz are shown in Fig. 11.11(A) to (D) and Fig. 11.12(A) to (D) respectively. The simulation results are tabulated in Table 11.5.

TABLE 11.5: SIMULINK Advanced Model Simulation Results

Sl.No.	Frequency Input-Output Hz	Line to Neutral Output voltage THD (p.u.)	Line to Line Output Voltage THD (p.u.)	Input current THD (p.u.)	Load current THD (p.u.)
1)	50 – 50	0.8267	0.5823	0.5982	0.4626
2)	50 – 10	4.90	3.56	1.049	3.267

11.6 THREE PHASE INDUCTION MOTOR LOAD: A three phase cage Induction motor is used as load to the Venturini model and also the advanced model of MC using delta-sigma modulation. The parameters of the cage I.M. rated 4 kW, 400 Volts, Three Phase, 50 Hz, 4 poles, 1430 r.p.m. are given in Table 11.6 [51]. The Venturini model of the Delta-Sigma modulated MC driving the three phase IM is shown Fig. 11.13. The R-L load in the model shown in Fig. 11.3 is disconnected and a three phase cage IM whose parameters are in Table 11.6 is connected as load. The simulation results of stator currents, rotor speed and e.m. torque of the three phase IM as load is shown in Fig. 11.14 for zero external mechanical load.

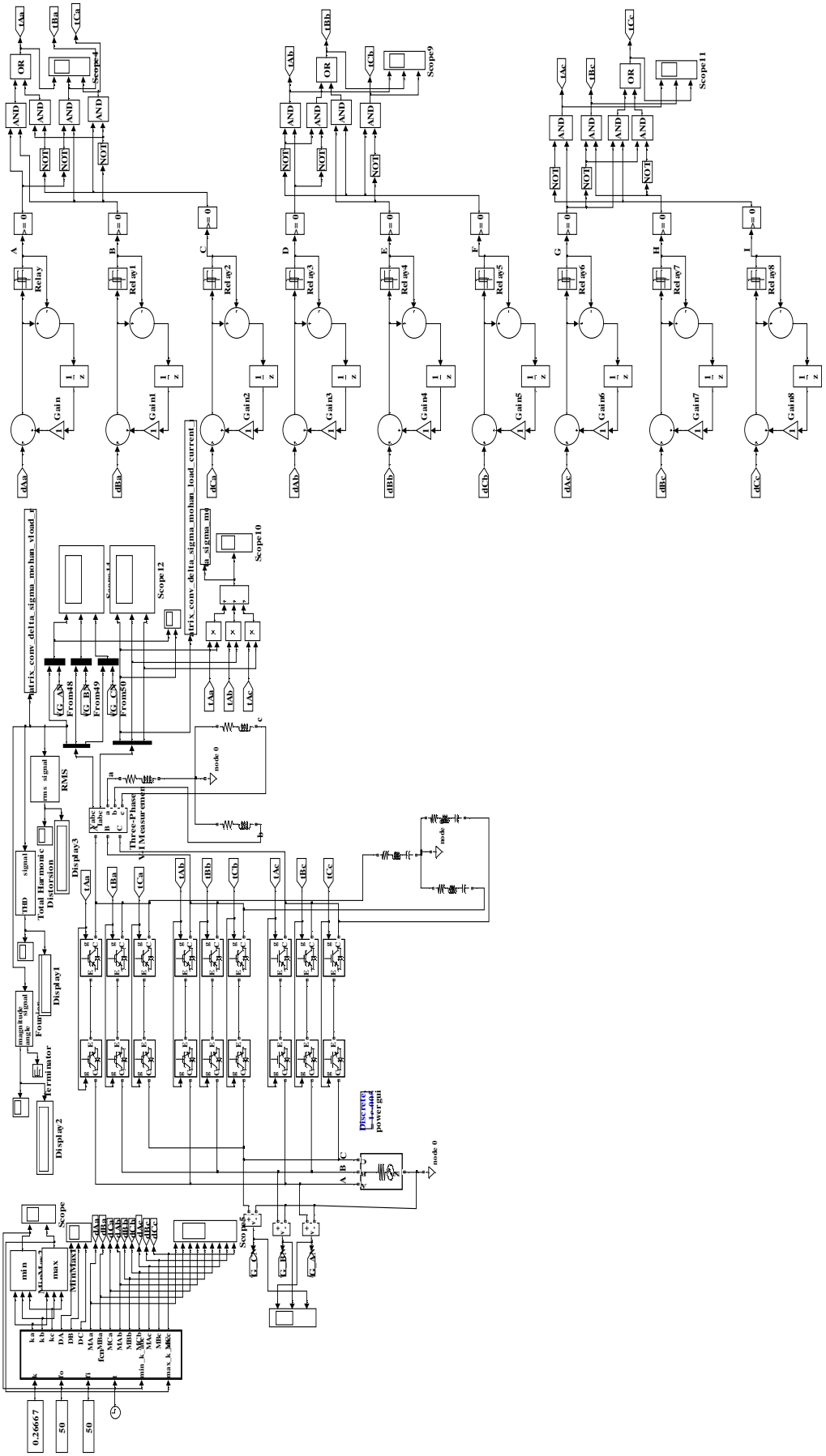


FIG. 11.8 MODEL OF DELTA-SIGMA MODULATED THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING ADVANCED MODULATION ALGORITHM

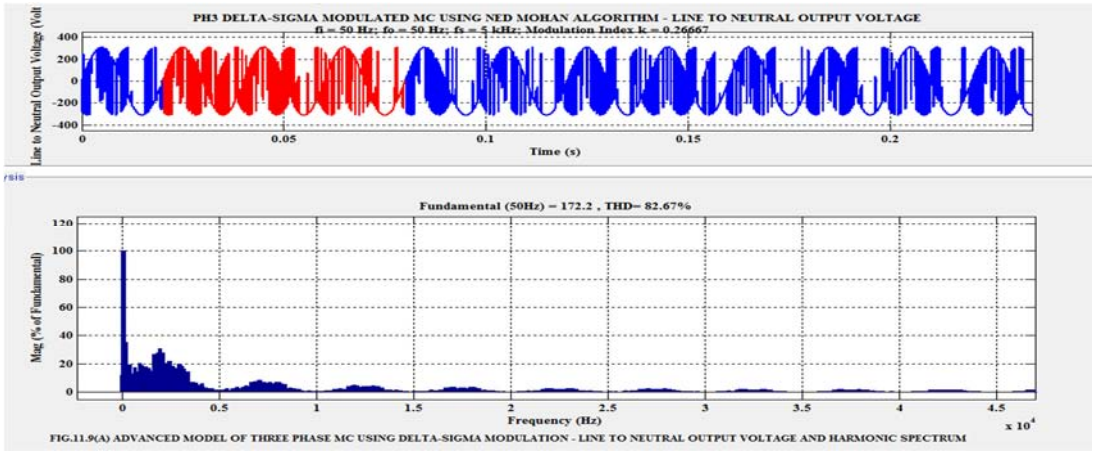


FIG.11.9(A) ADVANCED MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM

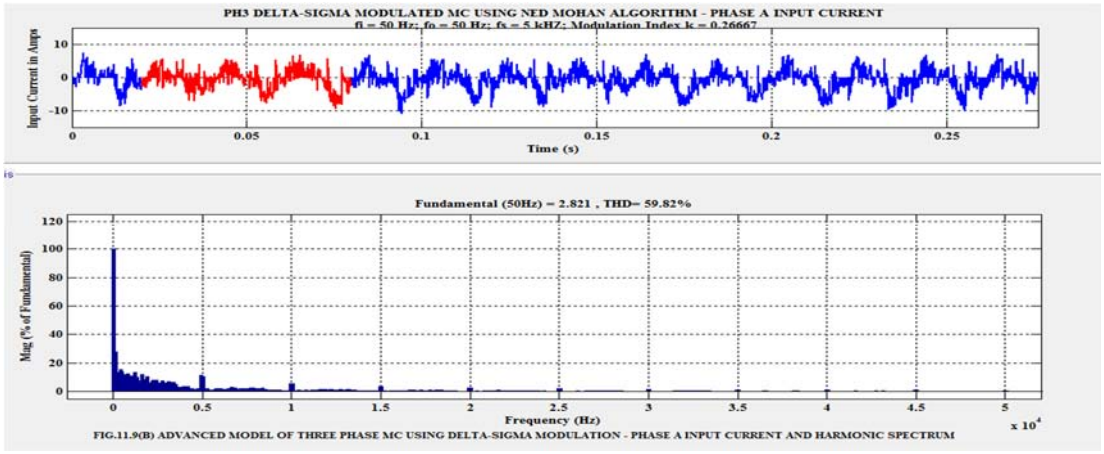


FIG.11.9(B) ADVANCED MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - PHASE A INPUT CURRENT AND HARMONIC SPECTRUM

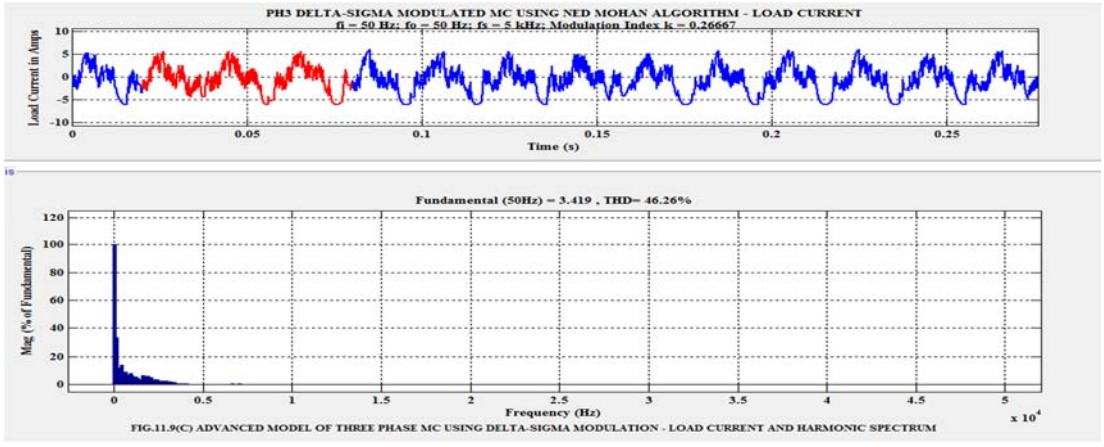


FIG.11.9(C) ADVANCED MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - LOAD CURRENT AND HARMONIC SPECTRUM

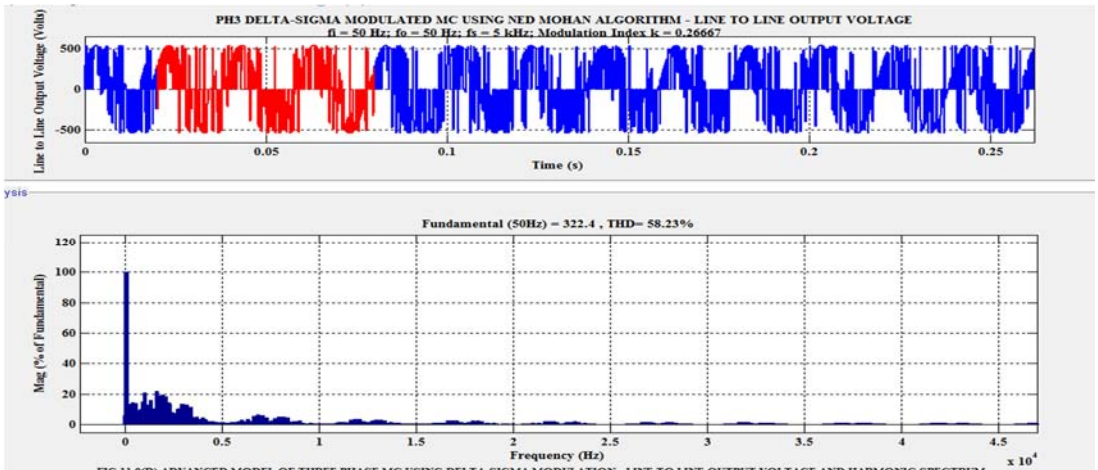
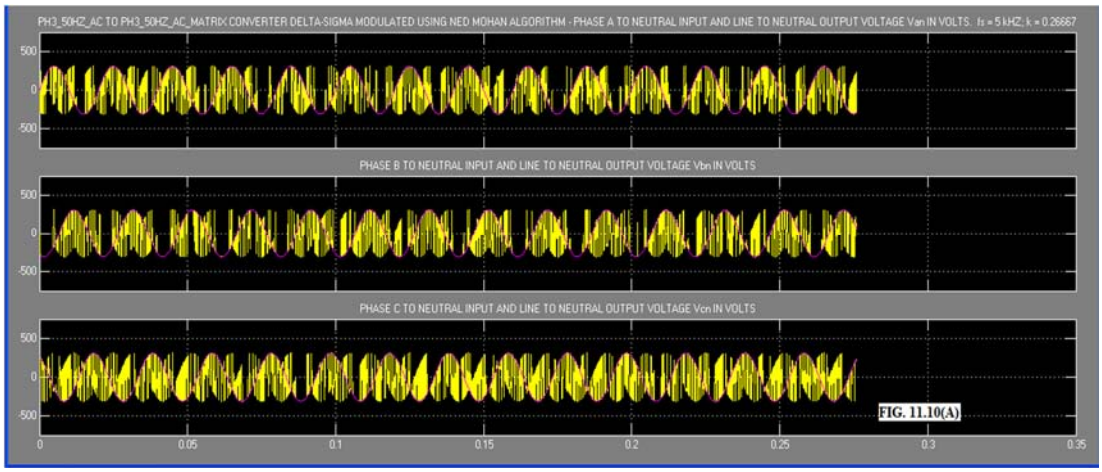
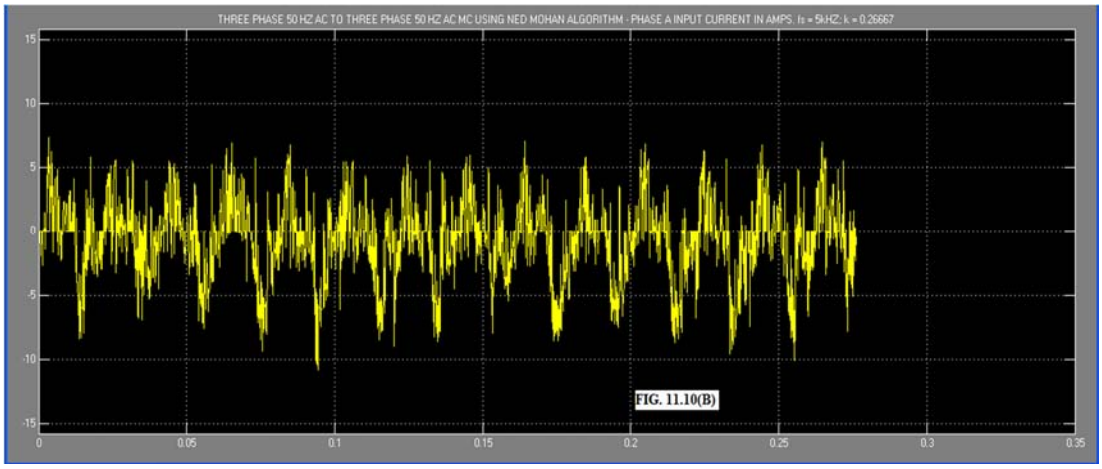
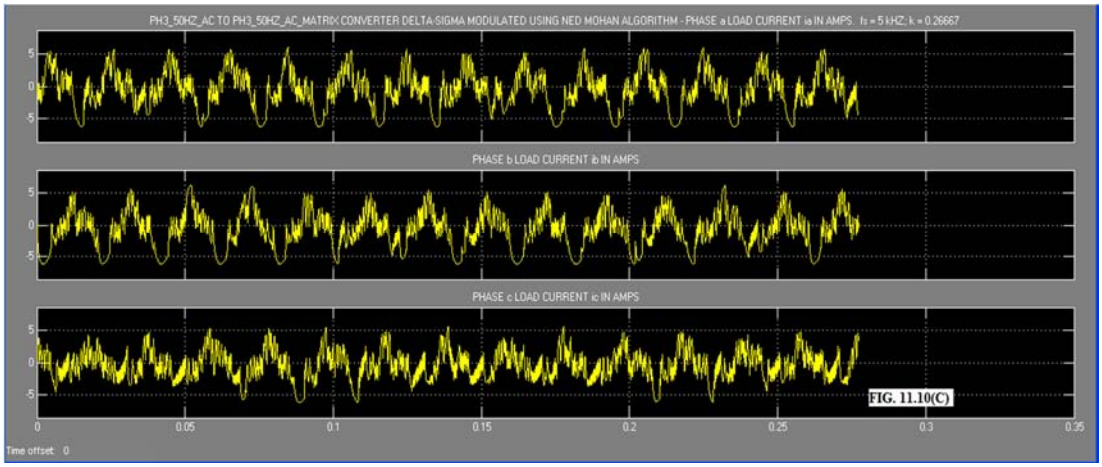
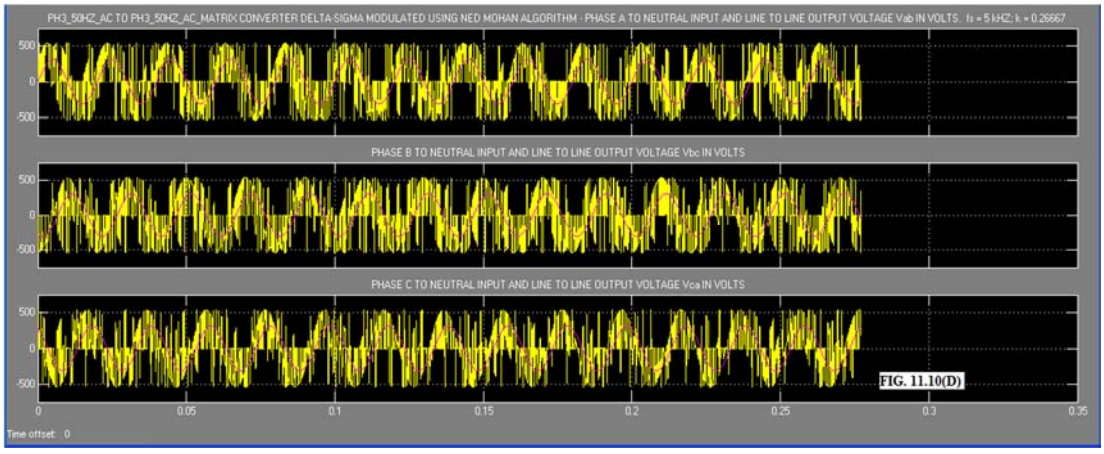


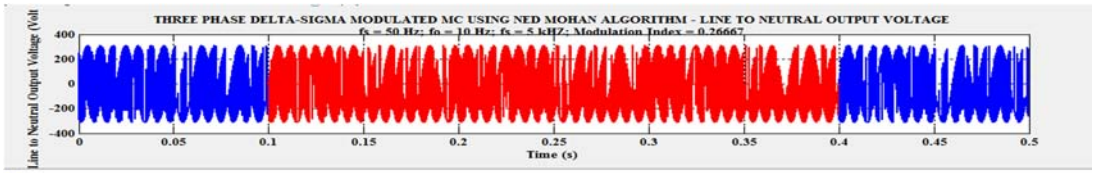
FIG.11.9(D) ADVANCED MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM


PH3_50HZ_AC TO PH3_50HZ_AC_MATRIX CONVERTER DELTA-SIGMA MODULATED USING NED MOHAN ALGORITHM - PHASE A TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Van IN VOLTS. fs = 5 kHZ; k = 0.26667
PHASE B TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vbn IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vcn IN VOLTS
FIG. 11.10(A)


THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MC USING NED MOHAN ALGORITHM - PHASE A INPUT CURRENT IN AMPS. fs = 5kHZ; k = 0.26667
FIG. 11.10(B)


PH3_50HZ_AC TO PH3_50HZ_AC_MATRIX CONVERTER DELTA-SIGMA MODULATED USING NED MOHAN ALGORITHM - PHASE a LOAD CURRENT ia IN AMPS. fs = 5 kHZ; k = 0.26667
PHASE b LOAD CURRENT ib IN AMPS
PHASE c LOAD CURRENT ic IN AMPS
FIG. 11.10(C)
Time offset: 0


PH3_50HZ_AC TO PH3_50HZ_AC_MATRIX CONVERTER DELTA-SIGMA MODULATED USING NED MOHAN ALGORITHM - PHASE A TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vab IN VOLTS. fs = 5 kHZ; k = 0.26667
PHASE B TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vbc IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vca IN VOLTS
FIG. 11.10(D)
Time offset: 0



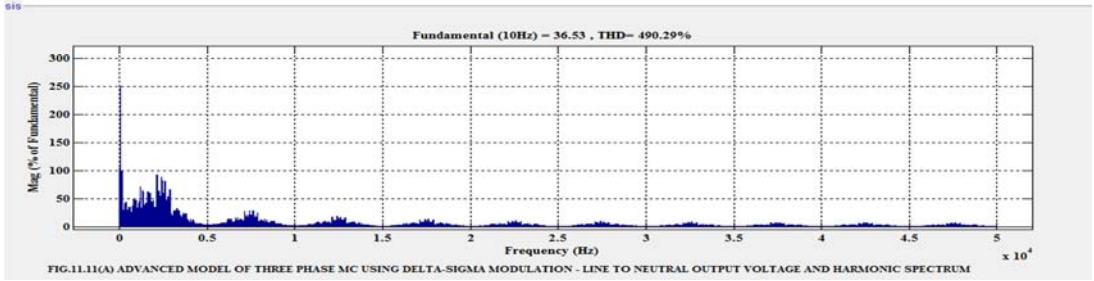
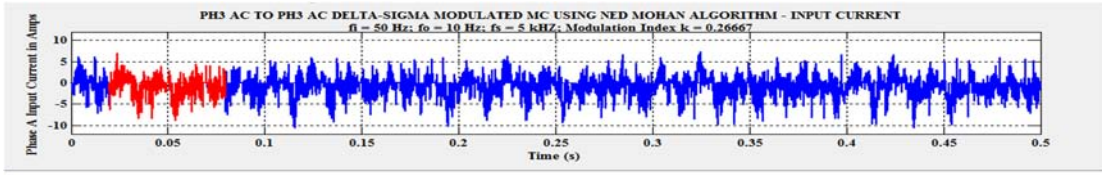


FIG.11.11(A) ADVANCED MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - LINE TO NEUTRAL OUTPUT VOLTAGE AND HARMONIC SPECTRUM



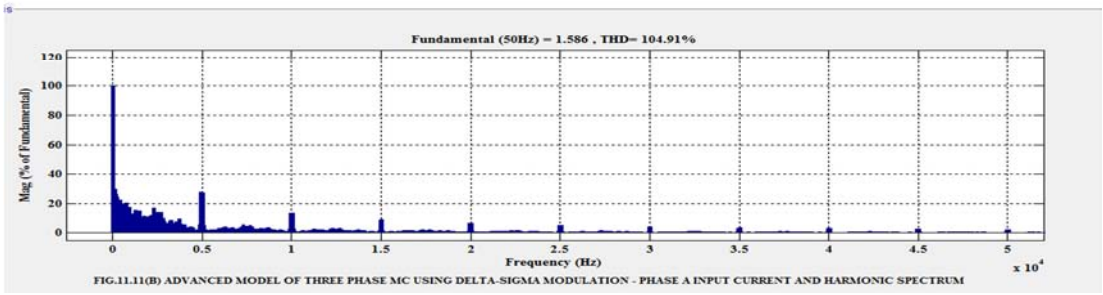
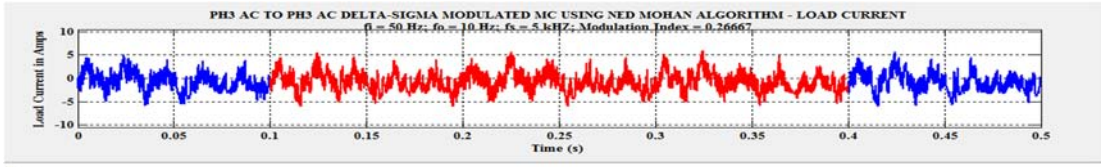


FIG.11.11(B) ADVANCED MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - PHASE A INPUT CURRENT AND HARMONIC SPECTRUM



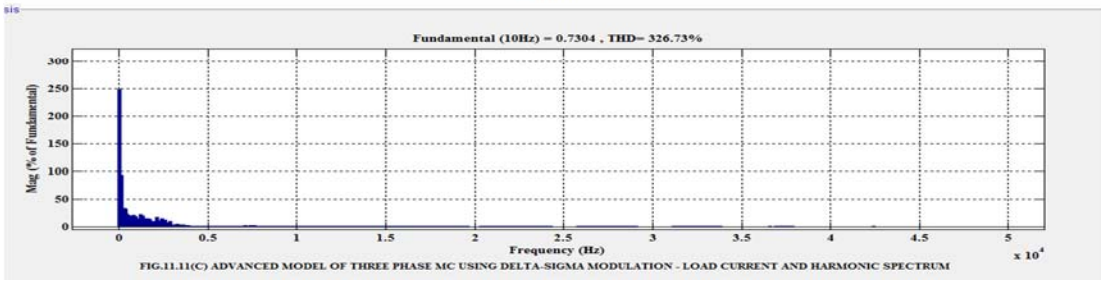
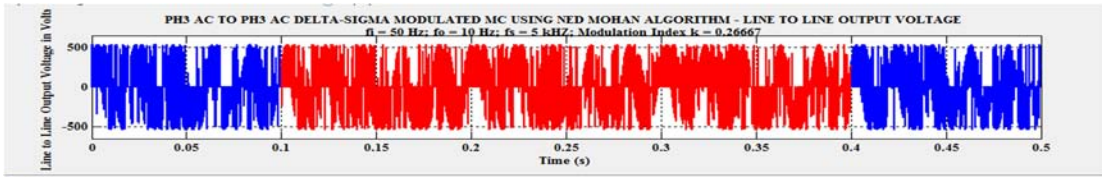


FIG.11.11(C) ADVANCED MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - LOAD CURRENT AND HARMONIC SPECTRUM



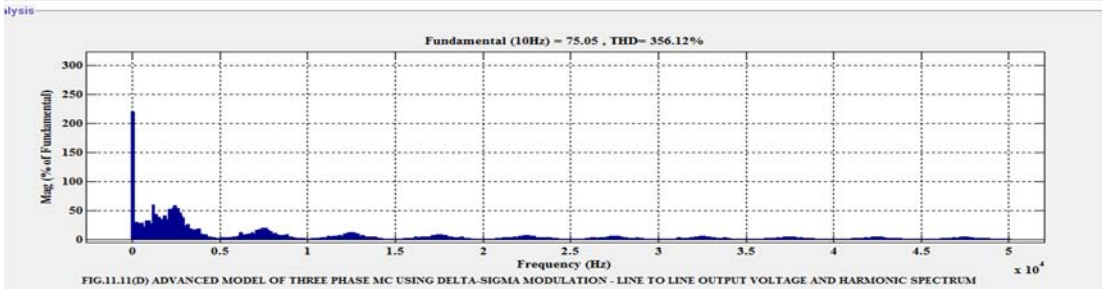
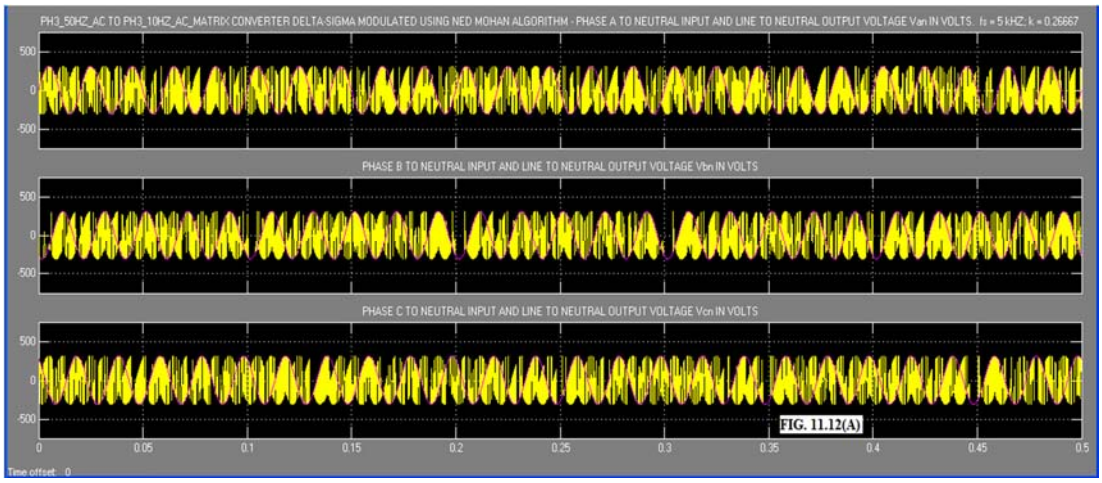
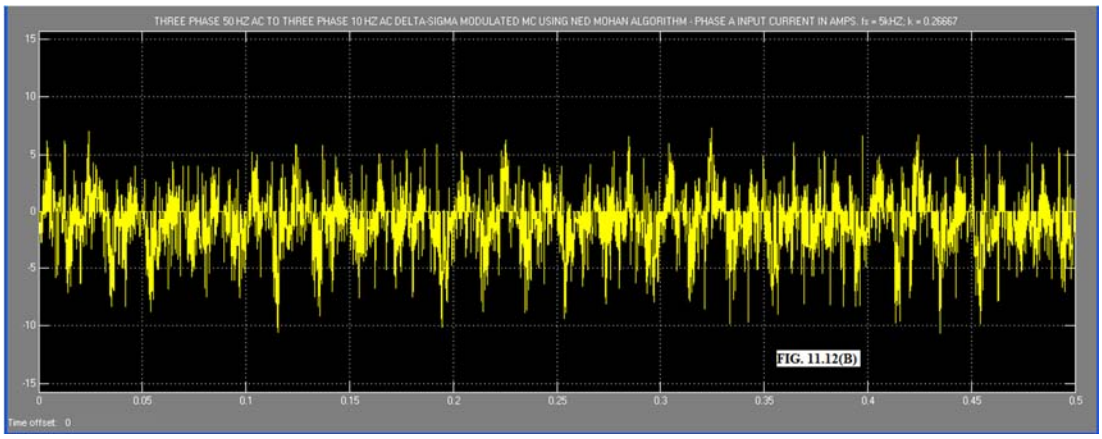
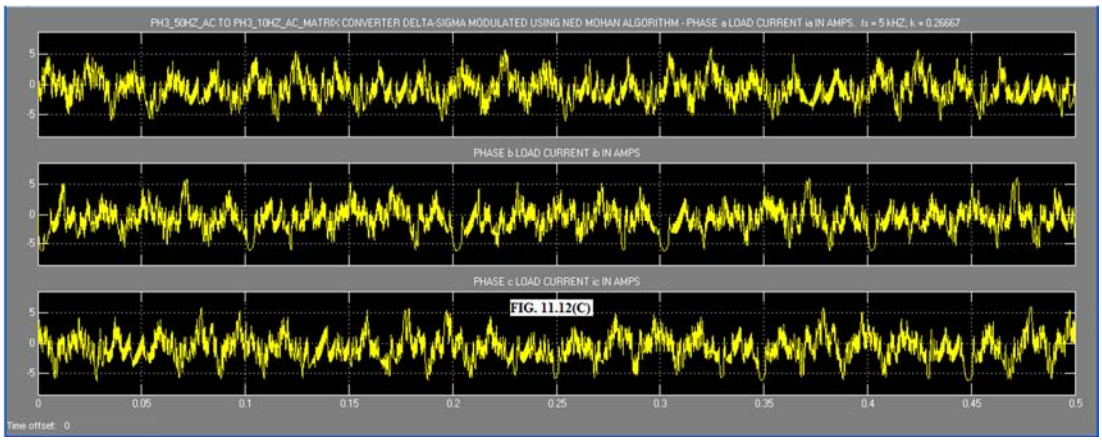
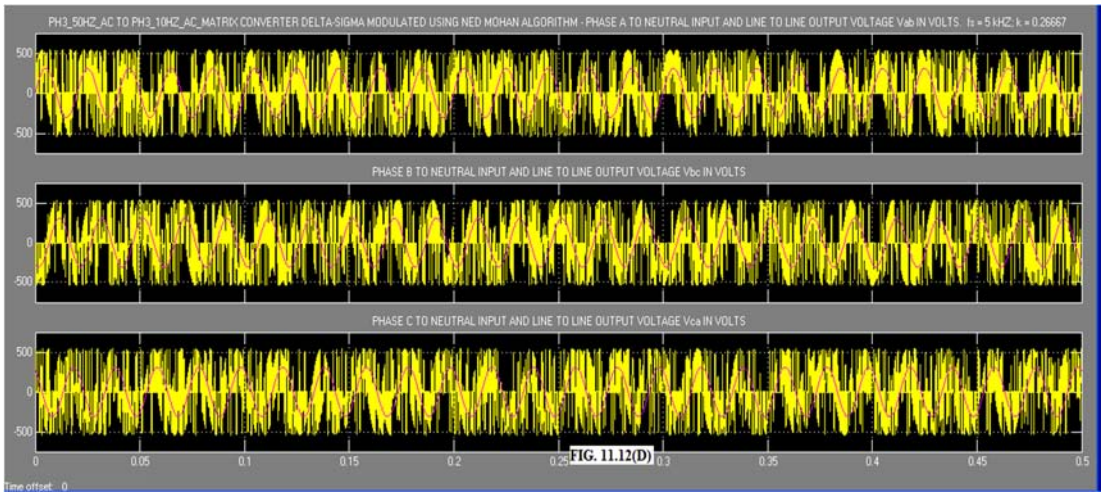


FIG.11.11(D) ADVANCED MODEL OF THREE PHASE MC USING DELTA-SIGMA MODULATION - LINE TO LINE OUTPUT VOLTAGE AND HARMONIC SPECTRUM


PH3_50HZ_AC TO PH3_10HZ_AC_MATRIX CONVERTER DELTA-SIGMA MODULATED USING NED MOHAN ALGORITHM - PHASE A TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Van IN VOLTS. fs = 5 kHZ; k = 0.26667
PHASE B TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vbn IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO NEUTRAL OUTPUT VOLTAGE Vcn IN VOLTS
FIG. 11.12(A)
Time offset: 0


THREE PHASE 50 HZ AC TO THREE PHASE 10 HZ AC DELTA-SIGMA MODULATED MC USING NED MOHAN ALGORITHM - PHASE A INPUT CURRENT IN AMPS. fs = 5kHZ; k = 0.26667
FIG. 11.12(B)
Time offset: 0


PH3_50HZ_AC TO PH3_10HZ_AC_MATRIX CONVERTER DELTA-SIGMA MODULATED USING NED MOHAN ALGORITHM - PHASE a LOAD CURRENT ia IN AMPS. fs = 5 kHZ; k = 0.26667
PHASE b LOAD CURRENT ib IN AMPS
PHASE c LOAD CURRENT ic IN AMPS
FIG. 11.12(C)
Time offset: 0


PH3_50HZ_AC TO PH3_10HZ_AC_MATRIX CONVERTER DELTA-SIGMA MODULATED USING NED MOHAN ALGORITHM - PHASE A TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vab IN VOLTS. fs = 5 kHZ; k = 0.26667
PHASE B TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vbc IN VOLTS
PHASE C TO NEUTRAL INPUT AND LINE TO LINE OUTPUT VOLTAGE Vca IN VOLTS
FIG. 11.12(D)
Time offset: 0

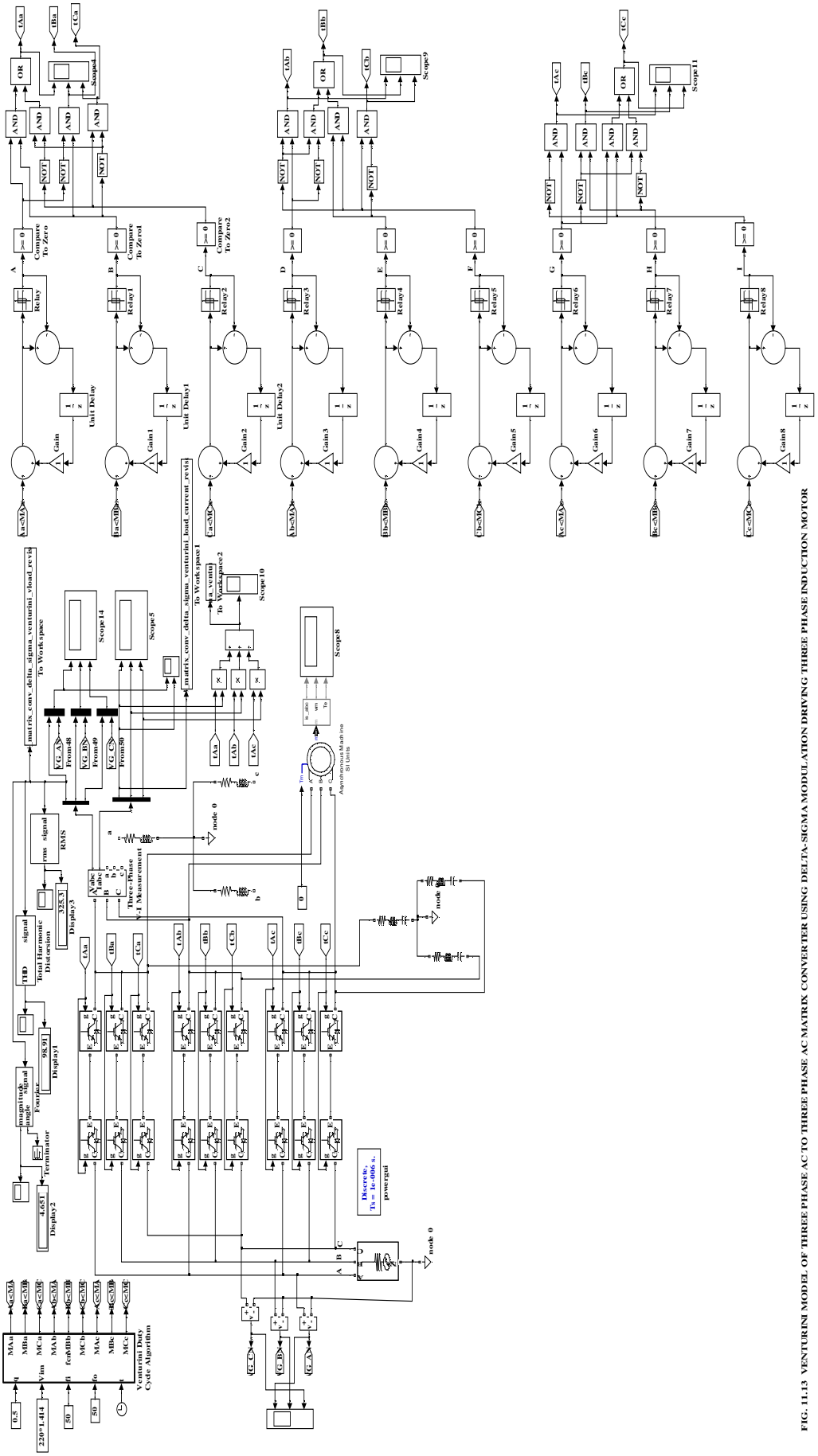
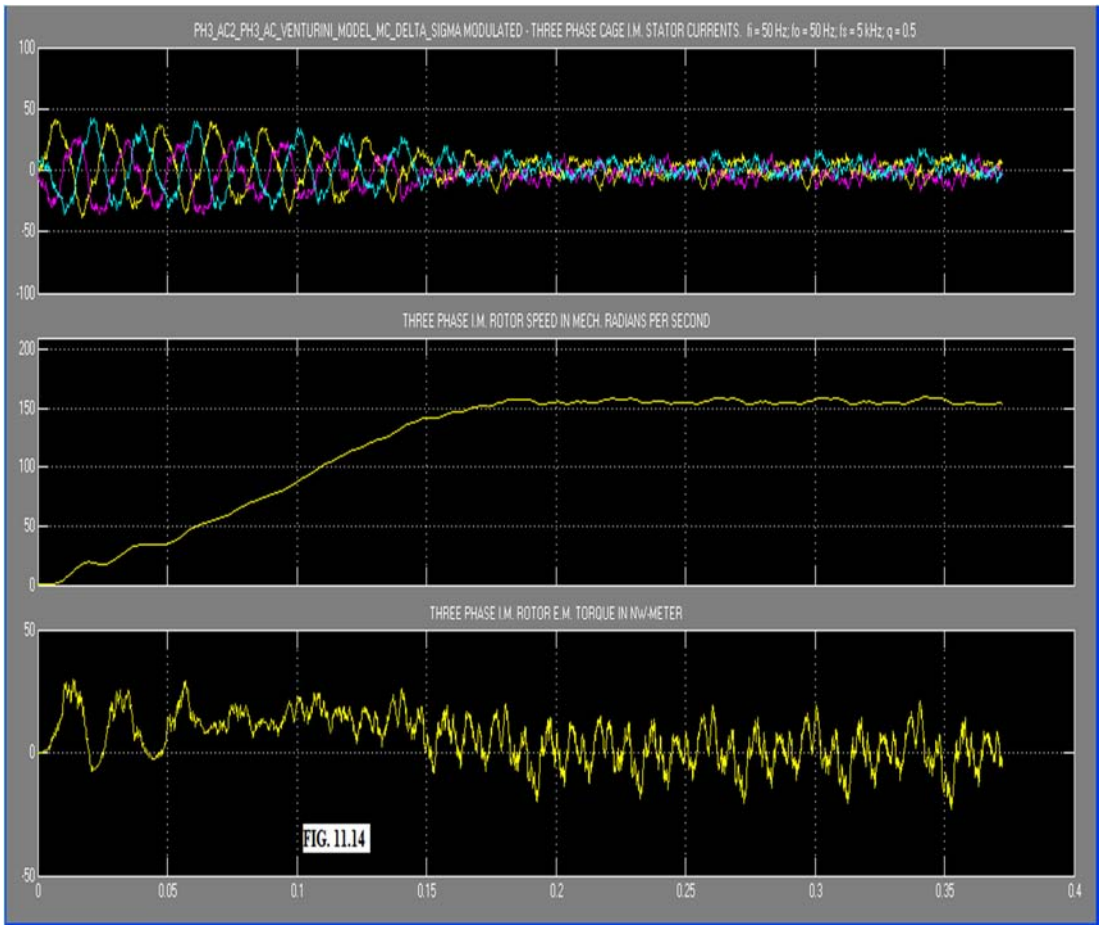
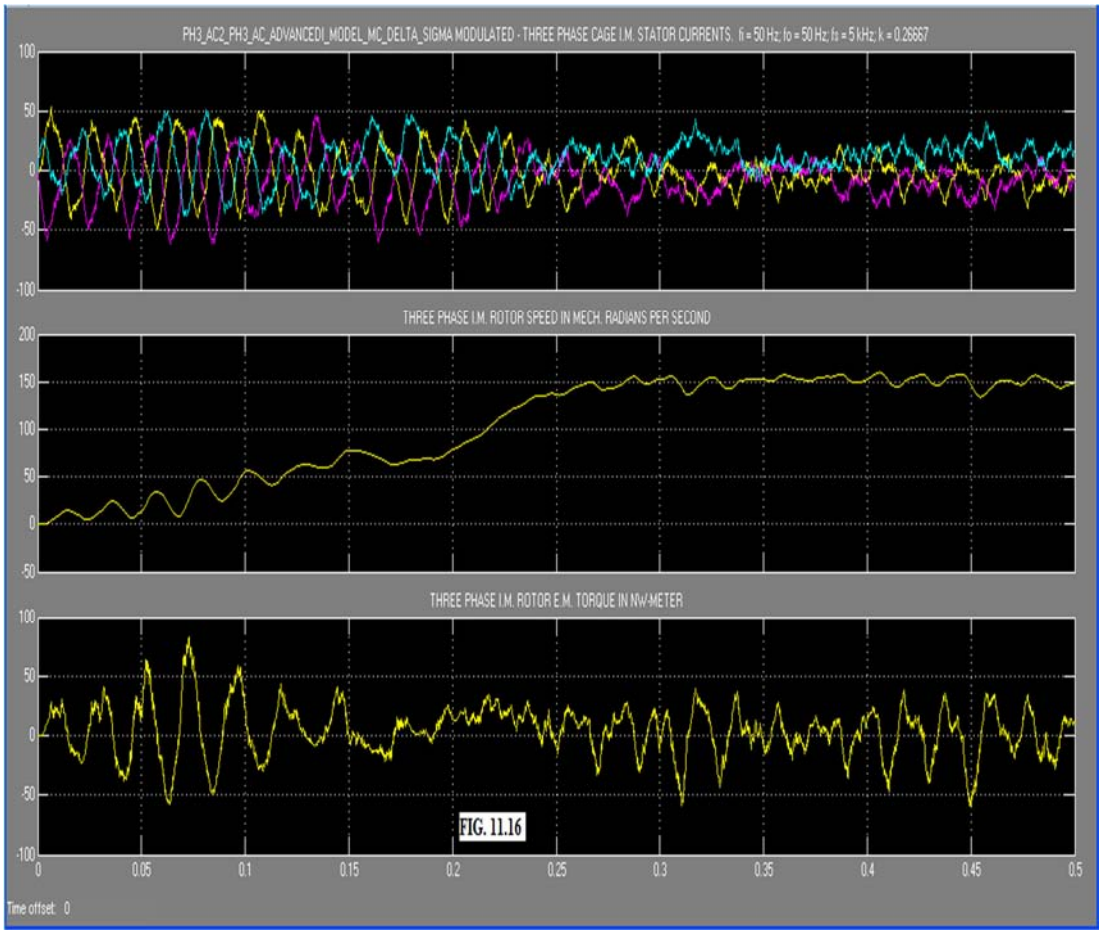


FIG. 11.13 VENTURINI MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING DELTA-SIGMA MODULATION DRIVING THREE PHASE INDUCTION MOTOR


PH3_AC2_PH3_AC_VENTURINI_MODEL_MC_DELTA_SIGMA MODULATED - THREE PHASE CAGE I.M. STATOR CURRENTS. fi = 50 Hz; fo = 50 Hz; fs = 5 kHz; q = 0.5
THREE PHASE I.M. ROTOR SPEED IN MECH. RADIANS PER SECOND
THREE PHASE I.M. ROTOR E.M. TORQUE IN NW-METER
FIG. 11.14


PH3_AC2_PH3_AC_ADVANCEDI_MODEL_MC_DELTA_SIGMA MODULATED - THREE PHASE CAGE I.M. STATOR CURRENTS. fi = 50 Hz; fo = 50 Hz; fs = 5 kHz; k = 0.26667
THREE PHASE I.M. ROTOR SPEED IN MECH. RADIANS PER SECOND
THREE PHASE I.M. ROTOR E.M. TORQUE IN NW-METER
FIG. 11.16
Time offset: 0

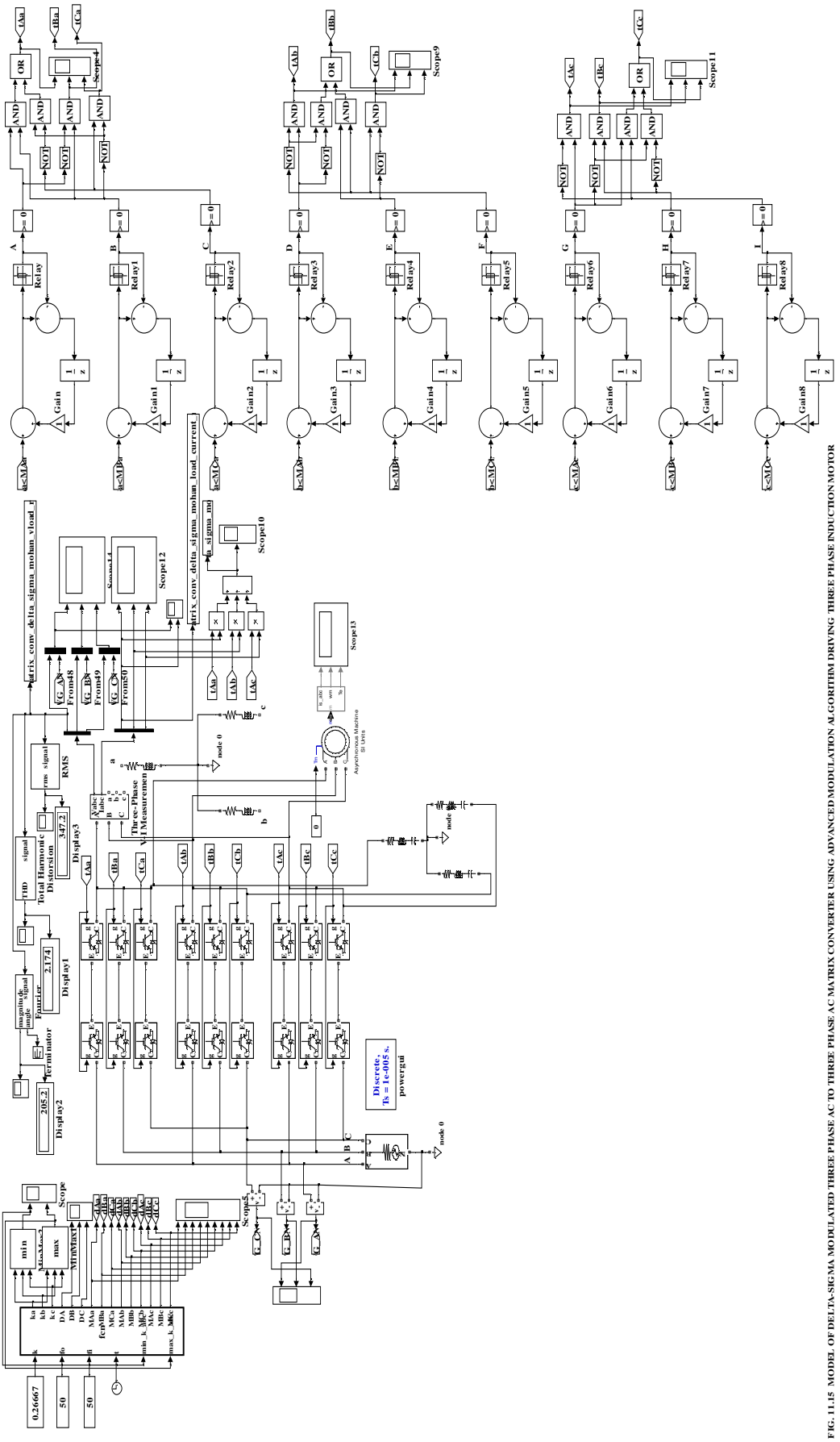


FIG. 11.15 MODEL OF DELTA-SIGMA MODULATED THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING ADVANCED MODULATION ALGORITHM DRIVING THREE PHASE INDUCTION MOTOR

TABLE 11.6: PH3 IM Parameters

Sl.No.	Parameter	Value	Unit	Sl.No.	Parameter	Value	Unit
1)	Stator Resistance Rs	1.405	Ohms	5)	Mutual Inductance Llm	0.1722	H
2)	Rotor Resistance Rr'	1.395	Ohms	6)	Rotor Inertia	0.0131	Kg-m^2
3)	Stator Leakage Inductance Lls	0.005839	H	7)	Damping constant	0.002985	N.m.s
4)	Rotor Leakage Inductance Llr'	0.005839	H	8)	No. of Poles	4	---

The Advanced model of the Delta-Sigma modulated MC driving the three phase IM is shown Fig. 11.15. The R-L load in the model shown in Fig. 11.8 is disconnected and a three phase cage IM whose parameters are in Table 11.6 is connected as load. The simulation results of stator currents, rotor speed and e.m. torque of the three phase IM as load is shown in Fig. 11.16 for zero external mechanical load.

11.7 DISCUSSION OF RESULTS: Comparison of the simulation results for the harmonic spectrum of line to neutral and line output voltages as well as for input and load currents for the venturini model of MC using delta-sigma modulation with that of carrier based modulation given in Chapter III indicates the absence harmonic voltage components at integral multiples of sampling frequency. Similar comparison of the harmonic spectrum for the above values for advanced model of MC using delta-sigma modulation with that of carrier based modulation given in chapter IV indicates the absence of harmonic voltage components at integral multiples of sampling frequency. The proposed method suppress noise peaks in the output voltage and is found to be suitable for clearing noise regulation. As for the simulation results of three phase IM, it is seen that in both cases the stator starting current is high and finally settles to the no load value. Similarly the e.m. torque in both cases are initially high and finally settles to zero corresponding to the externally applied mechanical load. As for the rotor speed, it is seen that in both cases the rotor reaches close to the no load speed of 1430 r.p.m. which is 149.6 mech.rad per second. However the rate of rise of rotor speed is slow for the advanced model as compared to the Venturini model.

11.8 CONCLUSIONS: A method of modeling MC using delta-sigma modulation technique is presented. Comparison of the THD of line to neutral and line output voltages indicates that for a 50 Hz output frequency, the advanced model has low THD compared to Venturini model both with delta-sigma modulation. However with 10 Hz output frequency, the above results are just reversed. The absence of harmonic components of voltages at integral multiples of sampling frequency responsible for noise peak is worth noting. For the input current advanced model gives lower THD compared to Venturini model with delta-sigma modulation. The proposed method suppress noise peaks in the output voltage and is found to be suitable for clearing noise regulation. As for three phase IM performance. It is seen that with both Venturini and advanced model, the rotor reaches rated no load speed with zero external load, the rate of rise of speed being faster for the former as compared to the later model. ----------

Chapter XII

Single Phase AC to Three Phase AC Matrix Converter

12.1 INTRODUCTION: For single phase AC to three phase AC power conversion, three phase indirect method is used where the single phase AC is first rectified to DC and this DC link voltage is inverted to AC using three phase inverter. A control and designing method of the capacitance of the compensation capacitor for a direct single phase AC to three phase AC matrix converters with application to a variable speed induction motor is reported in the literature [50]. The amplitude of the compensation capacitor voltage is controlled to absorb the single phase power fluctuation along with the load power. A method is proposed to decide the input side parameters such as the capacitance of the compensation capacitor, considering the input voltage and the power of the IM [50]. A circuit configuration with a compensation capacitor in the input side is introduced which absorbs the fluctuating power due to the single phase AC power. Here the single phase AC source is connected to an LC filter and compensating capacitor [50]. The two nodes of the LC filter and the compensating capacitor end terminals are connected to nine bidirectional switches [50]. Indirect virtual rectifier-inverter analysis is used. Derivations for modulation ratio and output power flow are presented [50]. A method of designing and selecting the compensating capacitor is given in terms of the output phase voltage, output power flow and input frequency [50]. In this chapter a detailed analysis of the single phase AC to three phase AC MC is presented. A model of this single phase AC to three phase AC MC is developed in SIMULINK [51]. Simulation results of the single phase AC to three phase AC MC is presented for both R-L load and three phase IM load.

12.2 ANALYSIS OF SINGLE PHASE AC TO THREE PHASE AC MATRIX CONVERTER: The single phase AC to three phase AC MC is shown in Fig. 12.1. Here the junction of the input filter

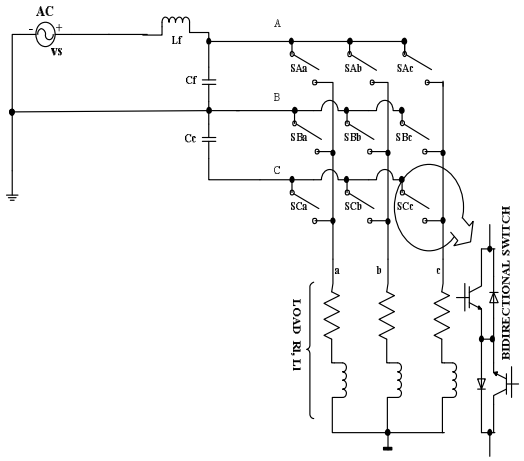


FIG. 12.1: SINGLE PHASE AC TO THREE PHASE AC MATRIX CONVERTER

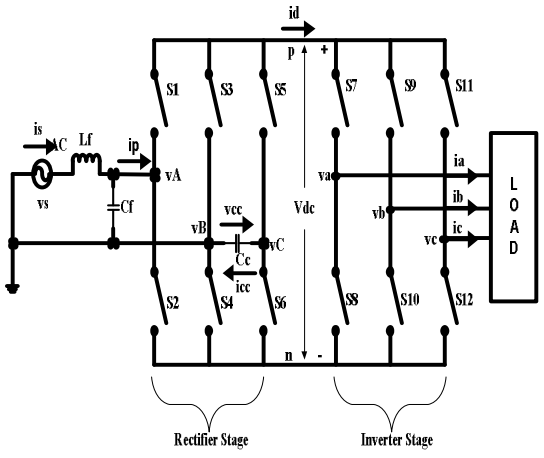


FIG. 12.2: VIRTUAL INDIRECT RECTIFIER-INVERTER CIRCUIT

inductor and capacitor is connected to input phase A, the junction of the input filter capacitor and compensation capacitor is connected to input phase B and the end of the compensation capacitor is connected to input phase C of the 3 X 3 MC consisting of nine bidirectional switches [50]. The

equivalent circuit of Fig. 12.1 is shown in Fig. 12.2 which is a virtual indirect three phase rectifier-inverter circuit [50]. The relationship between switches of Fig. 12.1 and Fig. 12.2 is given by equation 9.1 in chapter IX. The following analysis for the design of compensation capacitor C_C is based on reference 50.

12.2.1 CONTROL OF VIRTUAL RECTIFIER: The rectifier stage in Fig. 12.2 is a Current Source Converter (CSC). Referring to Fig. 12.2, the input voltage is expressed below:

$$v_S = \sqrt{2} * V_S * \sin(\omega_i . t) \quad (12.1)$$

$$V_S = RMS \quad value \quad of \quad input \quad voltage$$

Assuming unity input power factor, the reference input current i_S^* is given below:

$$i_S^* = \sqrt{2} * I_S * \sin(\omega_i . t) \quad (12.2)$$

$$I_S = RMS \quad value \quad of \quad input \quad current$$

Modulation signal m_S for the switch S1 and S2 in Fig. 12.2 is given below:

$$m_S = M_S * \sin(\omega_i . t) \quad (12.3)$$

$$M_S = Modulation \quad ratio \quad of \quad modulation \quad signal \quad m_S$$

The fundamental component of the current i_{pf} of current i_p in Fig. 12.2 is given below:

$$i_{pf} = M_S * i_d * \sin(\omega_i . t) \quad (12.4)$$

$$i_d = DC \quad Link \quad Current$$

When the current $i_{pf} = i_S^*$, we have the following equation by equating equation 12.2 and 12.3:

$$I_S = \frac{M_S * i_d}{\sqrt{2}} \quad (12.5)$$

Input power p_i is obtained by multiplying equations 12.1 and 12.2 which is given below:

$$p_i = 2 * V_S * I_S * \sin^2(\omega_i . t)$$

$$= V_S * I_S - V_S * I_S * COS\ (2 * \omega_i . t) \quad (12.6)$$

Compensating capacitor current reference i_{CC}^* is gen below:

$$i_{CC}^* = \sqrt{2} * I_{CC} * \sin\left(\omega_i . t + \frac{\pi}{4}\right) \quad (12.7)$$

$$I_{CC} = RMS \quad value \quad of \quad compensating \quad capacitor \quad current$$

A modulation signal m_C for switches S5 and S6 in Fig. 12.2 to control i_{CC} is given below:

$$m_C = M_C * \sin\left(\omega_i . t + \frac{\pi}{4}\right) \quad (12.8)$$

$$M_C = Modulation \quad ratio \quad of \quad modulation \quad signal \quad m_C$$

Fundamental frequency component of compensation capacitor current i_{CCf} is given below:

$$i_{CCf} = M_C * i_d * \sin\left(\omega_i.t + \frac{\pi}{4}\right) \qquad (12.9)$$

$$i_d = \quad DC \quad Link \quad Current$$

Compensation capacitor voltage v_{CC} is given below:

$$v_{CC} = \frac{1}{C_C} * \left(\int i_{CCf} * dt\right) = -\frac{M_C * i_d}{\omega_i * C_C} * \cos\left(\omega_i.t + \frac{\pi}{4}\right) \qquad (12.10)$$

$$i_d = \quad DC \quad Link \quad Current$$

Power input to compensating capacitor is obtained by multiplying equation 12.9 with 12.10 which is given below:

$$p_C = \quad -\frac{M_C^2 * i_d^2}{\omega_i * C_C} * \sin\left(\omega_i.t + \frac{\pi}{4}\right) * \cos\left(\omega_i.t + \frac{\pi}{4}\right)$$

$$= \quad -\frac{M_C^2 * i_d^2}{2 * \omega_i * C_C} * \cos\left(2 * \omega_i.t\right) \qquad (12.11)$$

When the fluctuating power is compensated, then the second term on the R.H.S. of equation 12.6 equal to equation 12.11. Thus equating second term of equation 12.6 with equation 12.11 and using equation 12.5 for the value of I_S, we have the following equation for M_C:

$$V_S * I_S * COS\ \left(2 * \omega_i.t\right) = \frac{M_C^2 * i_d^2}{2 * \omega_i * C_C} * \cos\left(2 * \omega_i.t\right)$$

$$V_S * I_S = \frac{M_C^2 * i_d^2}{2 * \omega_i * C_C}$$

$$\frac{V_S * M_S * i_d}{\sqrt{2}} = \frac{M_C^2 * i_d^2}{2 * \omega_i * C_C}$$

$$M_C = \sqrt{\frac{\sqrt{2} * \omega_i * C_C * M_S * V_S}{i_d}} \qquad (12.12)$$

12.2.2 CONTROL OF VIRTUAL INVERTER: Referring to Fig. 12.2, when any one of switch S1, S3 and S5 of the virtual rectifier is ON, the p rail of DC link is $+V_{Tmax}$ and when any one of switch S2, S4 and S6 is ON, the n rail of DC link is $-V_{Tmax}$ where V_T is the RMS value of the output phase voltage of the virtual inverter in Fig. 12.2. Assume that the neutral of the load connected to the virtual inverter is grounded (NOT shown in Fig. 12.2). Then assuming that the modulation ratio of the switches of the virtual inverter is M_T, with reference the neutral ground of the load connected to the virtual inverter, inverter output phase voltage can be expressed as follows:

$$\left[+V_{Tmax} - \left(-V_{Tmax}\right)\right] = V_{dc} * M_T$$

$$V_{Trms} = \quad V_T = \frac{V_{dc} * M_T}{2 * \sqrt{2}} \qquad (12.13)$$

12.2.3 CALCULATION OF MODULATION RATIO: Balancing the input power and output power is required for the proper operation of the single phase AC to three phase AC MC. The virtual DC link voltage is obtained from equation 12.13, as given below:

$$V_{dc} = \frac{2*\sqrt{2}*V_T}{M_T} \qquad (12.14)$$

The sum of the constant and fluctuating component of the virtual DC link voltage V_{dc} is given by multiplying equation 12.1 with equation 12.3, as given below:

$$V_{dcf} = \sqrt{2}*V_S*M_S*\sin^2(\omega_i.t)$$

$$= \left(\frac{V_S*M_S}{\sqrt{2}}\right) - \left(\frac{V_S*M_S*\cos(2*\omega_i.t)}{\sqrt{2}}\right) \qquad (12.15)$$

When the fluctuating component of DC link voltage V_{dcf} is compensated fully, the second term on the R.H.S. of equation 12.15 is zero and under this circumstances, equating the first term of equation 12.15 with equation 12.14, the modulation ratio M_S of the switches S1 and S2 can be expressed as follows:

$$\frac{V_S*M_S}{\sqrt{2}} = \frac{2*\sqrt{2}*V_T}{M_T}$$

$$M_S = \frac{4*V_T}{V_S*M_T} \qquad (12.16)$$

If the single phase fluctuating input power is compensated, then the output power P_O is a constant and is equal to the virtual DC link voltage V_{dc} multiplied by the DC link current i_d of the rectifier. This is given below:

$$P_O = V_{dc}*i_d = \frac{2*\sqrt{2}*V_T}{M_T}*i_d$$

$$i_d = \frac{P_O*M_T}{2*\sqrt{2}*V_T} \qquad (12.17)$$

Using equations 12.16 and 12.17 in equation 12.12, the modulation ratio M_C can be expressed as follows:

$$M_C = \sqrt{\frac{\sqrt{2}*\omega_i*C_C*4*V_T*V_S*2*\sqrt{2}*V_T}{P_O*M_T*V_S*M_T}}$$

$$= \sqrt{\frac{16*\omega_i*C_C*V_T^2}{P_O*M_T^2}} \qquad (12.18)$$

The modulation ratio M_C of the switches S5 and S6 is a function of output power P_O and the virtual inverter output phase voltage V_T. The DC link voltage $V_{dc}$is proportional to the ratio of V_T to M_T.

The RMS compensation capacitor voltage V_{CC} is is dependent on output power P_O. By designating RMS output phase voltage of the virtual inverter as V_T^*, the three phase reference output voltage of the inverter for an output frequency of ω_O can be expressed as follows:

$$\left.\begin{aligned} v_a^* &= \sqrt{2} * V_T^* * \sin(\omega_O.t) \\ v_b^* &= \sqrt{2} * V_T^* * \sin\left(\omega_O.t - \frac{2\pi}{3}\right) \\ v_c^* &= \sqrt{2} * V_T^* * \sin\left(\omega_O.t - \frac{4\pi}{3}\right) \end{aligned}\right] \quad (12.19)$$

The output power P_O is calculated as follows:

$$P_O = v_a^* * i_a + v_b^* * i_b + v_c^* * i_c \quad (12.20)$$

The modulation function M_S is calculated by substituting V_T^* to V_T in equation 12.16 and M_C is calculated by using equations 12.18 and substituting P_O from equation 12.20. All modulation ratios M_S, M_C and M_T lie in the range 0 to 1.

12.3 DESIGN OF COMPENSATION CAPACITOR: The capacitance of the compensating capacitor C_C is an important factor for the proper operation of single phase AC to three phase AC MC. The compensating power in the compensation capacitor is dependent on output power and the output voltage of MC is restricted by the compensation capacitor voltage. The compensation capacitor C_C decides the characteristics of the output power versus output phase voltage in a single phase to three phase MC. The compensation capacitor C_C is designed based on the relation between output power P_O and the output phase voltage V_T of the single phase to three phase MC with IM load to drive inertial load at constant acceleration. The maximum value of input phase voltage for the IM V_{Tmax} is decided by the maximum values of modulation ratios M_C and M_T given by equation 12.18. Output power P_O is determined by motor torque T_{em} and rotor angular speed ω_{re}. Using IM parameters and the IM RMS input phase voltage reference V_T^*, the IM torque T_{em} can be calculated. Using this T_{em} and rotor inertia J and damping constant B, the theoretical rotor speed ω_{ret} can be calculated.

Using RMS input voltage reference to the IM, the compensation capacitor C_C can be calculated using equation 12.18, where M_C and M_T are given the maximum value unity. Thus C_C and V_T^* and V_{Tmax} are related as follows:

$$V_T^* \le V_{Tmax} = \frac{1}{4} * \sqrt{\frac{P_O}{\omega_i * C_C}} \quad (12.21)$$

$$C_C \le \frac{P_O}{16 * V_T^{*2} * \omega_i} \quad (12.22)$$

Using equations 12.10, 12.17 and 12.21 and for the maximum value of M_C and M_T, the RMS value of the compensation capacitor voltage V_{CC} can be expressed as follows:

$$V_{CC} = \sqrt{\frac{P_O}{\omega_i * C_C}} \qquad (12.23)$$

From equation 12.23 and 12.21, it is clear that the RMS value of the compensation capacitor voltage V_{CC} is four times greater than the maximum output phase voltage V_{Tmax}.

12.4 MODEL DEVELOPMENT: The model of the Single phase AC to three phase AC MC fed IM drive was developed in SIMULINK [51]. The parameter of the three phase IM rated 4 kW, 400 V, 50 Hz, 4 poles, 1430 rpm is shown in Table 12.1.

TABLE 12.1: PH3 IM Parameters

Sl.No.	Parameter	Value	Unit
1	Stator Resistance Rs	1.405	Ohms
2	Rotor Resistance Rr'	1.395	Ohms
3	Stator Leakage Inductance Lls	0.005839	H
4	Rotor Leakage Inductance Llr'	0.005839	H
5	Mutual Inductance Llm	0.1722	H
6	Rotor Inertia	0.0131	Kg-m^2
7	Damping constant	0.002985	N.m.s

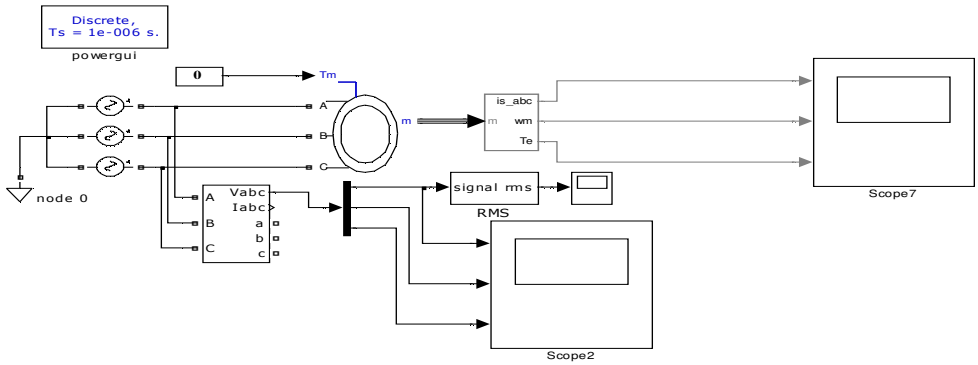


FIG. 12.3 THREE PHASE INDUCTION MOTOR UNDER NO LOAD TEST

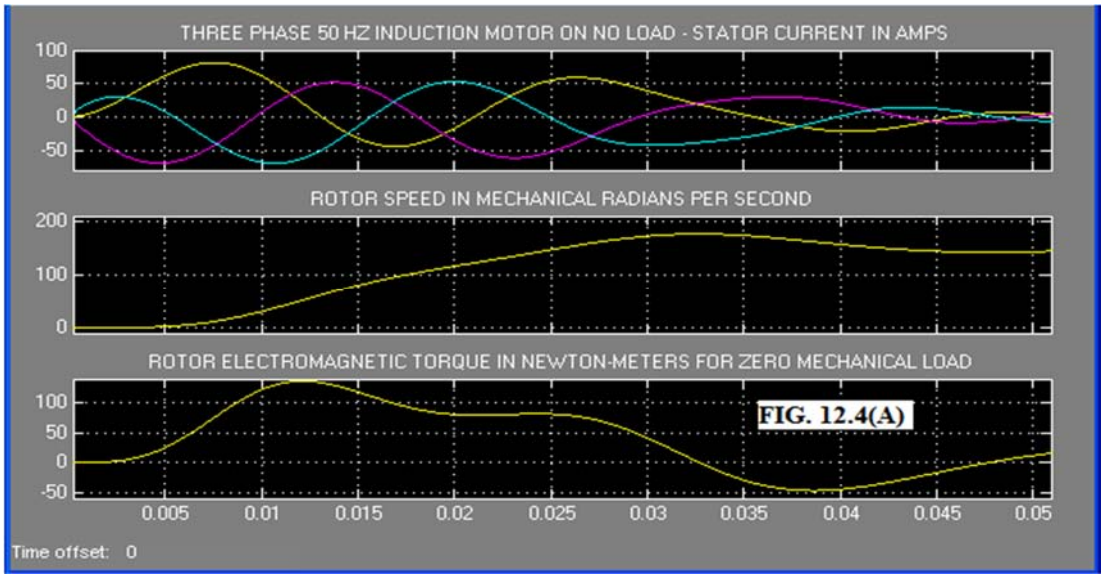
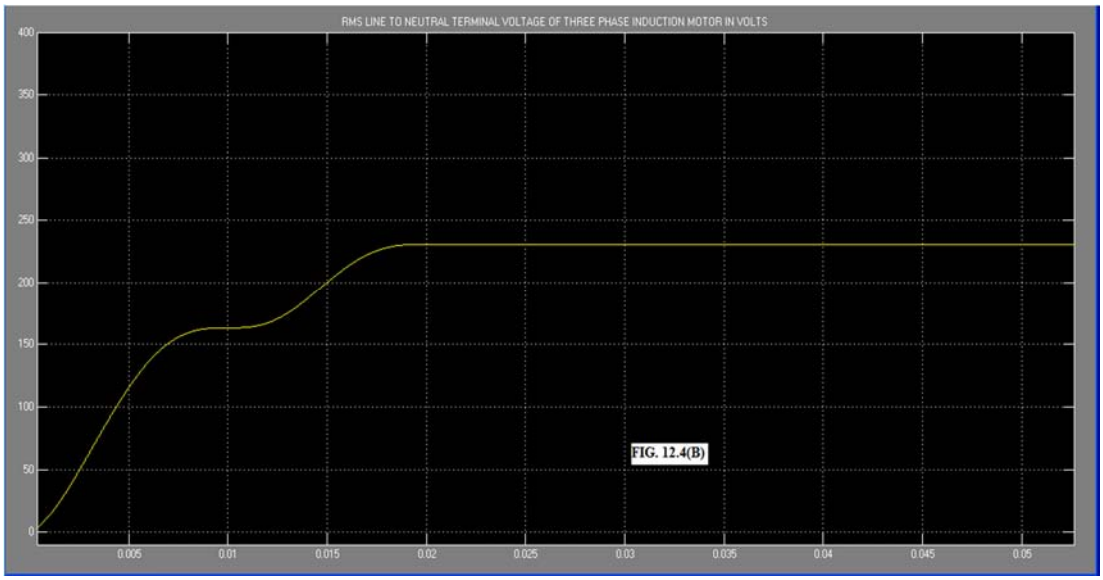


FIG. 12.4(A)



To design the compensating capacitor value, the three phase IM was first driven on no load at rated input voltage**.** The model of the three phase IM and its no load characteristics are shown in Fig. 12.3 and Fig. 12.4(A) and (B) respectively. From Fig. 12.4(A) it is seen that the time taken by the three phase IM to reach a no load speed of 149.67 mech.rad. per second which corresponds to a frequency slightly less than 50 Hz is 25 milliseconds. For this time of 25 milliseconds it is seen that from Fig. 12.4 (B) the RMS value of terminal voltage per phase rises to 230 Volts. Thus a V_T^* of 230 Volts is assumed and the given output power P_O is 1333.33 Watts. Using equation 12.22, the value of the Compensating capacitor C_C is found to be 5.017E-6 Farads. The input filter inductor L_f and filter capacitor C_f are taken to be 1E-3 H and 8E-6 Farads respectively.

12.4.1 MODEL OF SINGLE PHASE AC TO THREE PHASE AC MATRIX CONVERTER FED INDUCTION MOTOR DRIVE: The model of the single phase AC to three phase AC MC driving the IM is shown in Fig. 12.5. Here the gate pulses for the nine bidirectional switches are generated using Venturini modulation algorithm assuming unity input phase displacement factor given by equation 3.17 in section 3.3 of chapter III. This algorithm is also proved to be valid for three phase sine wave input voltages as given in A3.3 Appendix of Chapter III. In this model a saw-tooth carrier frequency of 10 kHz is used. The single phase AC input voltage source has an RMS value of 231 Volts and frequency 50 Hz. Two Embedded MATLAB Function blocks are used to generate the gate pulses. The method of generating this gate pulses and the source code used are already explained in Section 3.4.1 of Chapter III. The gate pulses drive the nine bidirectional switches of the MC.

12.4.2 SIMULATION RESULTS: The simulation of the single phase AC to three phase AC MC driving the IM is carried out in SIMULINK [51]. The ode15s(stiff/NDF) solver is used. The simulation parameters are given in Table 12.2 below. An output R-L-C filter to resonate at 10 kHz carrier switching frequency is used. The simulation results for the three phase 50 Hz line to line output voltage is shown in Fig. 12.6(A) and the stator current, rotor speed and electromagnetic torque of the three phase IM are shown in Fig. 12.6(B), for zero externally applied mechanical load.

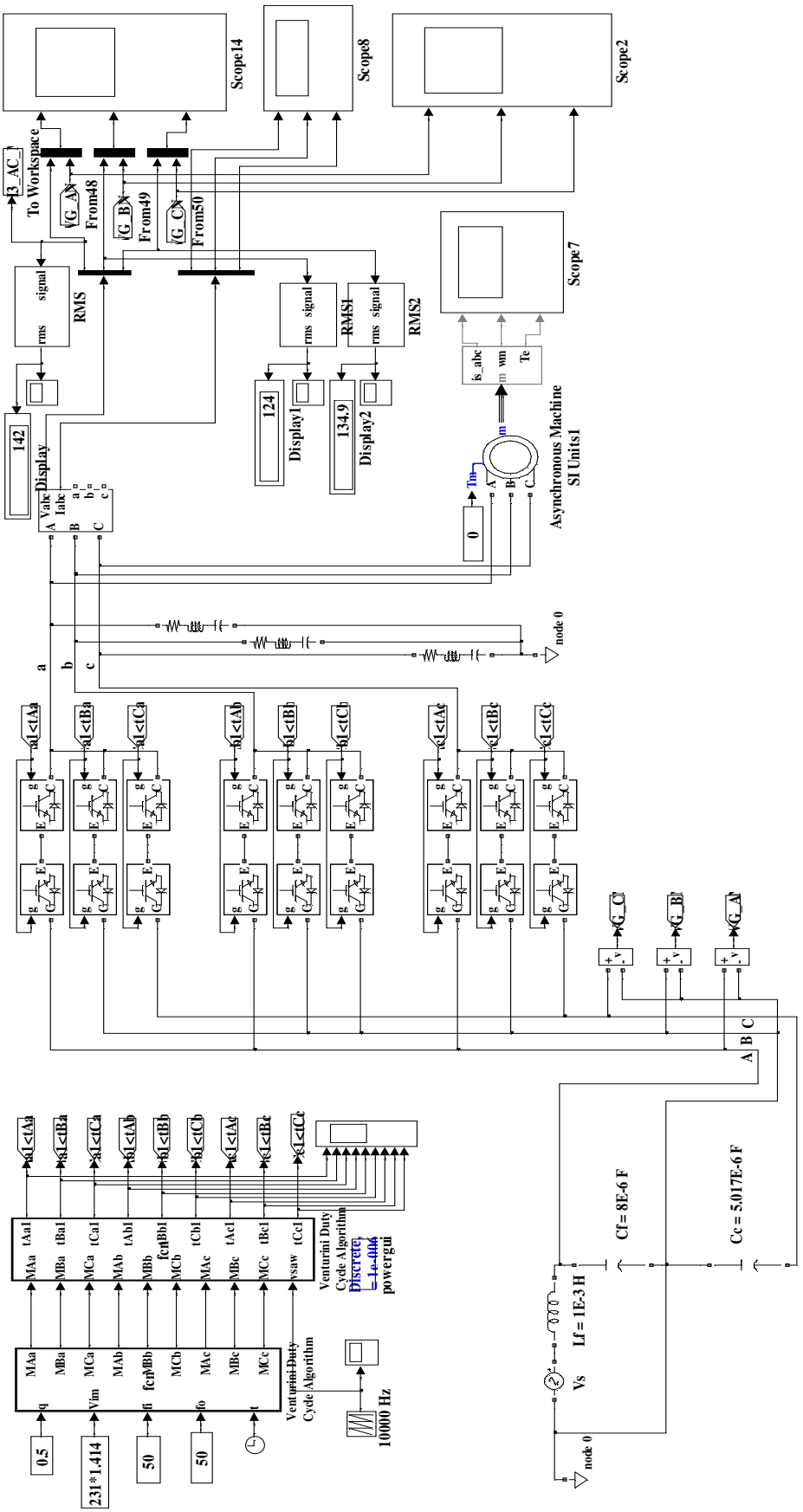
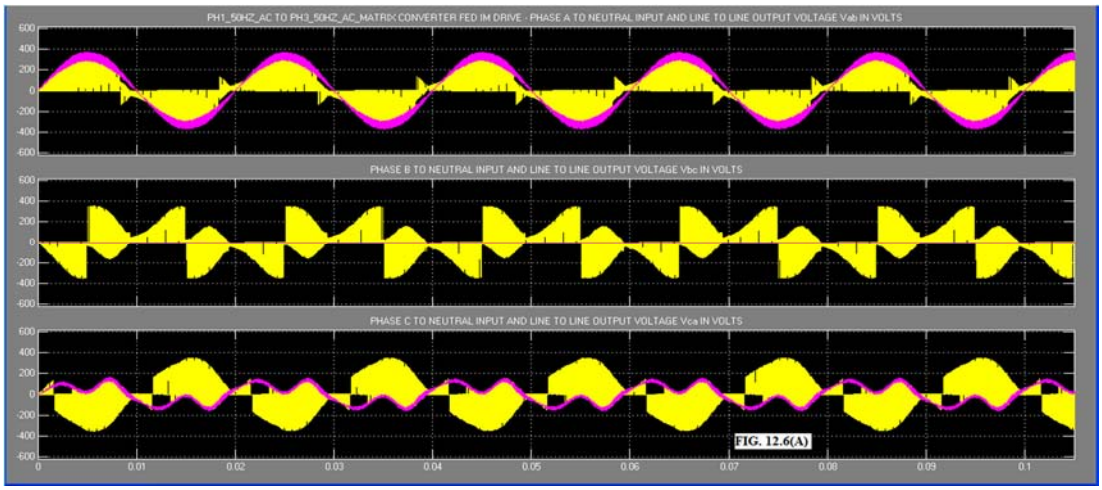


FIG. 12.5: MODEL OF SINGLE PHASE AC TO MATRIX CONVERTER FED I.M. DRIVE



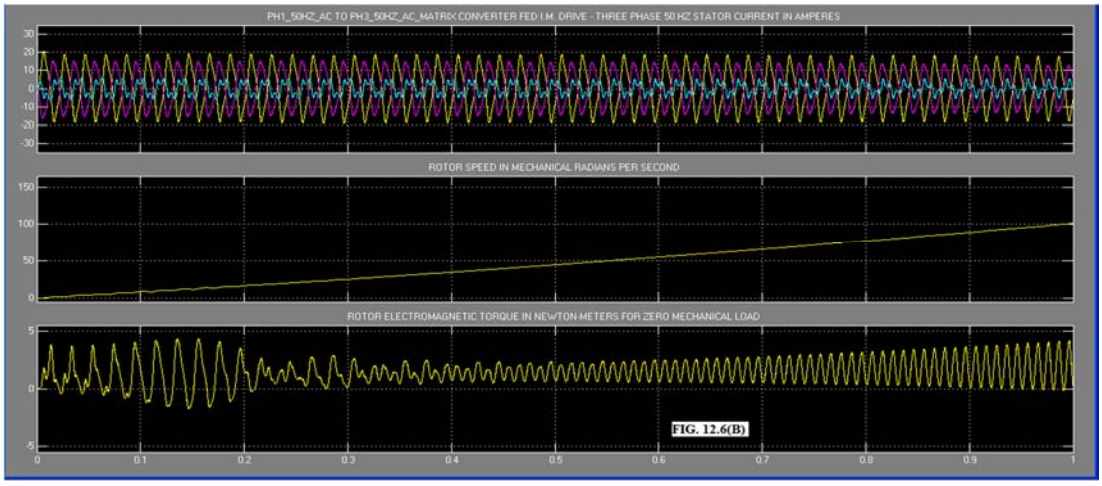


TABLE 12.2: PH1 AC to PH3 AC MC Model Parameters

Sl .No	Parameter	Value	Unit	Sl.No.	Parameter	Value	Unit
1	Single Phase RMS Line to Ground Input Voltage Vs	231	V	5	Modulation Index	0.5	--
2	Input Frequency fi	50	Hz	6	Compensation capacitor	5.017E-6	F
3	Output Frequency fo	50	Hz	7	Input Filter Inductor	1E-3	H
4	Saw-tooth Carrier Freqency fsw	10	kHz	8	Input Filter Capacitor	8E-6	F

12.4.3 MODEL OF SINGLE PHASE AC TO THREE PHASE AC MATRIX CONVERTER: The model of the single phase AC to three phase AC MC connected to an R-L load is shown in Fig. 12.7. The model is already explained under section 12.4.1 above.

12.4.4 SIMULATION RESULTS: The simulation of the single phase AC to three phase AC MC

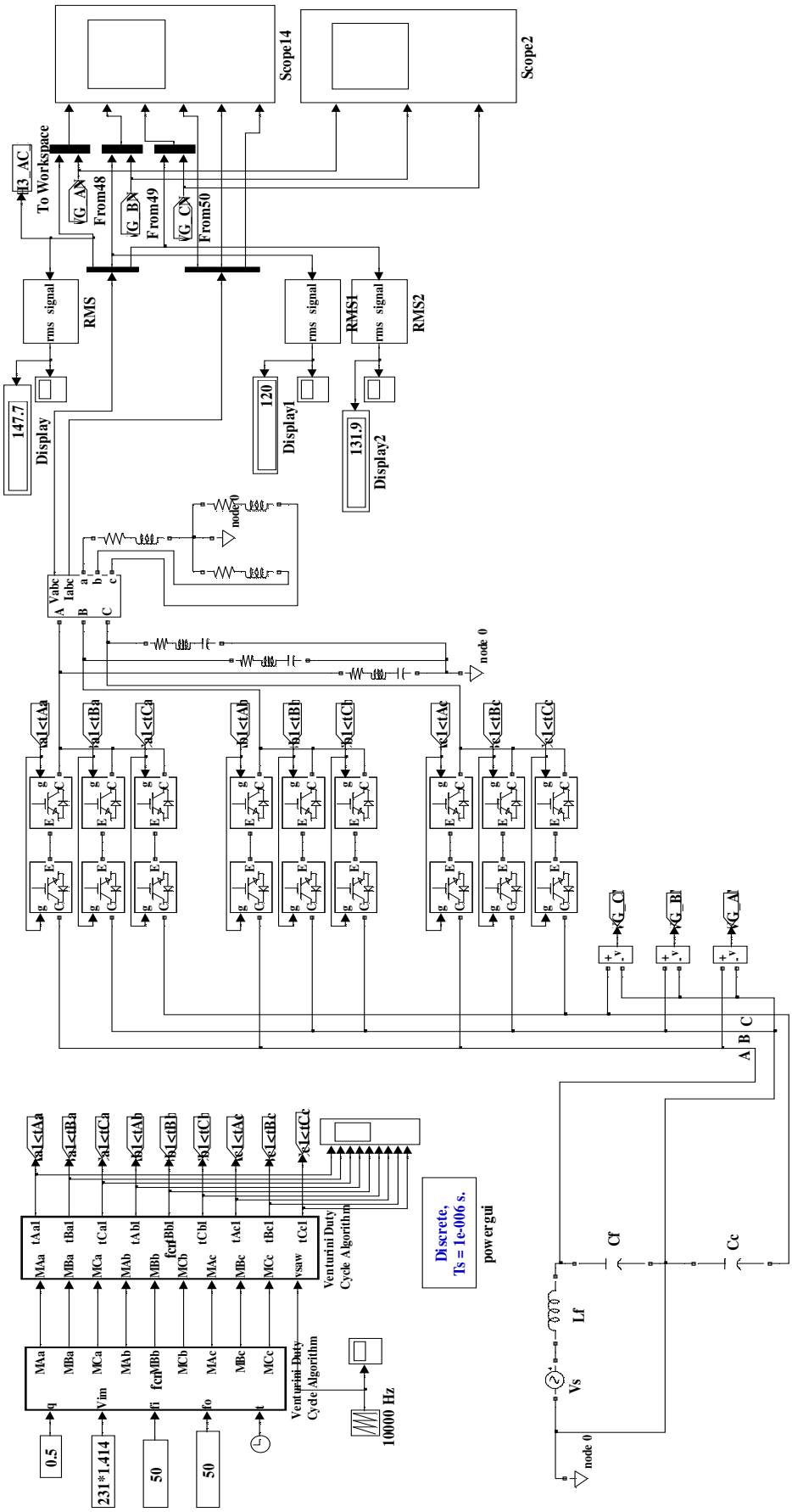
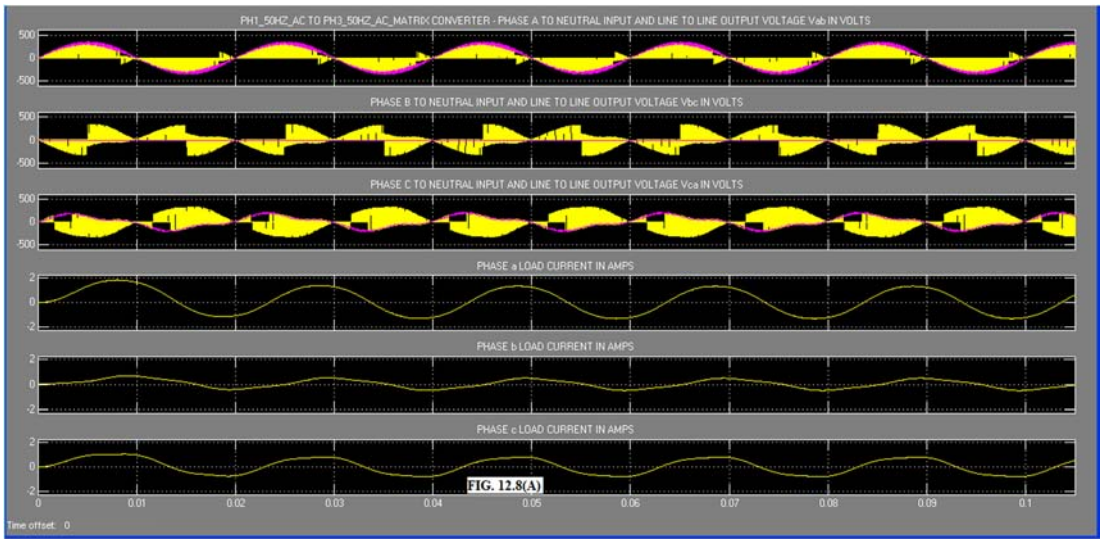
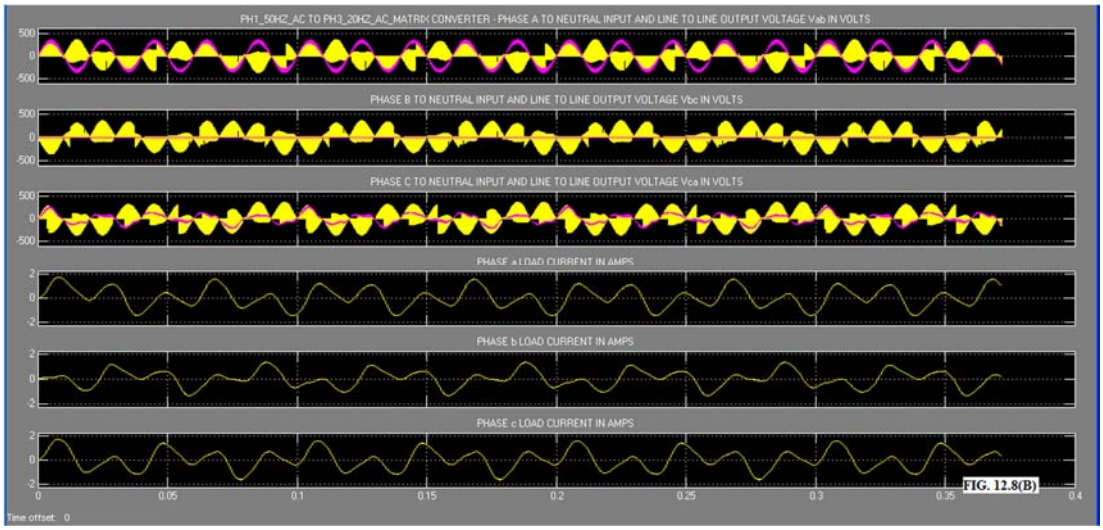


FIG. 12.7: MODEL OF SINGLE PHASE AC TO THREE PHASE AC TO MATRIX CONVERTER FED I.M. DRIVE





connected to the R-L load is carried out in SIMULINK [51]. The ode15s(stiff/NDF) solver is used. The simulation parameters used are the same as in Table 12.2 above. The R-L load used is 50 Ω and 0.5 Henries. An output R-L-C filter to resonate at 10 kHz carrier switching frequency is used. The simulation results for the three phase line to line output voltage and load current for 50 Hz and 20 Hz output frequencies are shown in Fig. 12.8(A) and Fig. 12.8(B) respectively.

12.5 DISCUSSION OF RESULTS: The simulation results for the case of three phase I.M. load shows unbalanced output voltage and load current. The speed pick up for the I.M. is very slow. As for static R-L load also unbalanced output voltages and load current are observed.

12.6 CONCLUSIONS: The model of a new technique for single phase AC to three phase AC MC is presented. Simulation results for three phase IM as well as for static R-L load shows conversion of single phase AC voltage to three phase AC voltage at the same frequency as the input or a different frequency. However the three phase output voltages and load current are found to be unbalanced by model simulation.

Chapter XIII

A Novel AC To AC Converter Using A DC Link

13.1 INTRODUCTION: A novel method of generating a Pulse Width Modulated single phase and three phase variable frequency, variable voltage AC from the normal 220 Volts/440 Volts, single phase/three phase 50 Hz AC supply mains using a step down transformer and an intermediate DC link is presented here.

13.2 SINGLE PHASE AC TO SINGLE PHASE AC CONVERTER USING A DC LINK: The block diagram of the single phase AC to single phase AC converter is shown in Fig. 13.1. The block

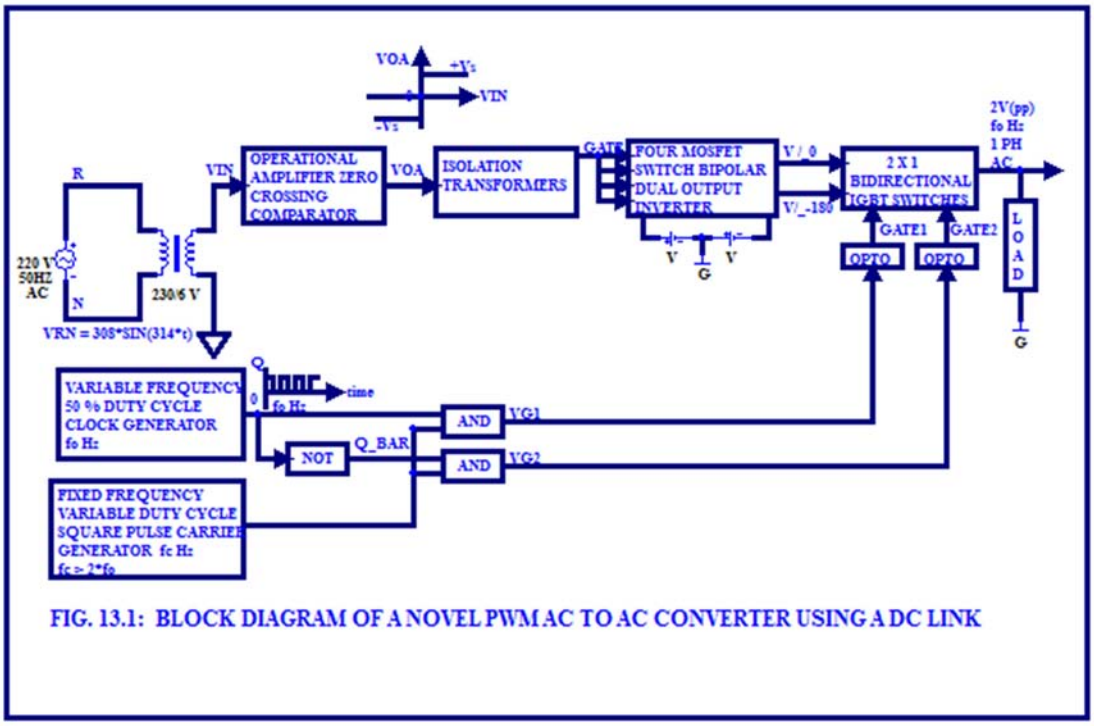


FIG. 13.1: BLOCK DIAGRAM OF A NOVEL PWM AC TO AC CONVERTER USING A DC LINK

diagram is explained below:

- The supply mains is a 220 Volts, 50 Hz AC.
- The step down transformer 230/6 V is connected to the supply mains.
- The secondary 6 V is connected to the op.amplifier zero crossing comparator.
- The output of the zero crossing comparator forms the gate drive input to all the four MOSFET switches forming the bipolar dual output inverter.
- The bipolar dual output inverter consists of two legs. Each leg is a pair of N and P type MOSFETs connected in series. The two parallel legs of the inverter are connected to the DC source which forms the DC link. The two outputs of this inverter are V/_0 and V/_-180 with a frequency of 50 Hz, where 2V is the DC link voltage. These two outputs are fed to the two IGBT bidirectional switches.

- The four gates of the two IGBT bidirectional switches are cross connected. This is different from the mode of connection used in conventional matrix converter. The output of this bidirectional switches is connected to the load.
- The clock generator output is a square pulse having a frequency of fo Hz with 50 % duty cycle. This frequency fo Hz is variable.
- The carrier generator output is a square pulse having a pre-calculated fixed frequency of fc Hz with a variable duty-cycle. The carrier frequency fc Hz must be at least two times greater than the desired output frequency of fo Hz.
- The load voltage Vo is a Pulse Width Modulated square wave AC with a peak to peak value of 2V Volts and frequency fo Hz.
- By varying the duty-cycle of the square pulse carrier generator, the magnitude of the output voltage Vo can be controlled.

13.3 MODEL OF A PWM SINGLE PHASE AC TO SINGLE PHASE AC CONVERTER: The schematic of the novel PWM Single phase AC to single phase AC converter is shown in Fig. 13.2.

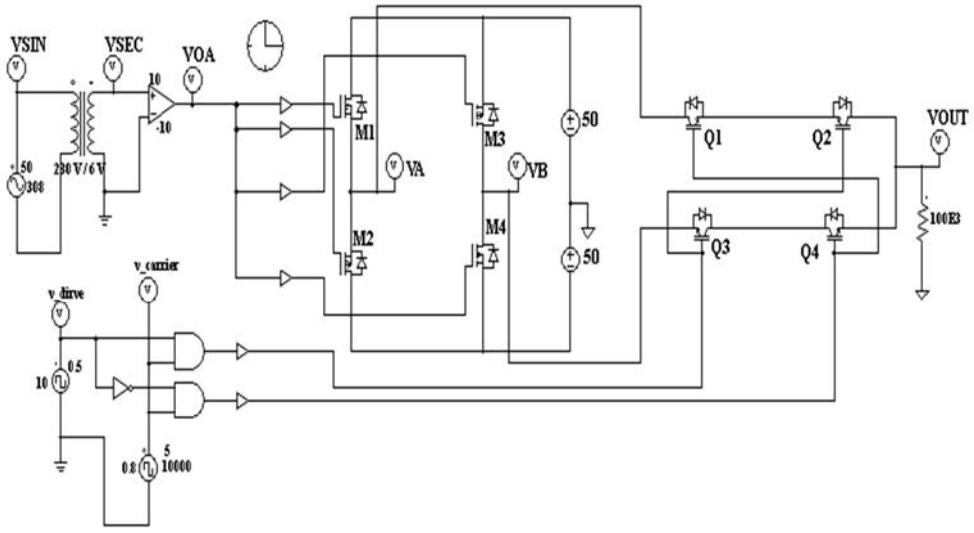


FIG. 13.2 A NOVEL PWM SINGLE PHASE AC SINGLE PHASE AC CONVERTER

The 230 Volts, 50 Hz single phase AC supply is stepped down to 6 Volts and given as input to the non-inverting input of op.amp. zero crossing comparator. The MOSFETs M1 and M2 are N and P MOSFET pair and so is the case with M3 and M4. This zero crossing comparator drives the four MOSFET switches M1 to M4 to produce bipolar dual output voltages which are given as inputs to four IGBT switches Q1 to Q4. The opto isolation circuit is NOT shown in Fig.13.2 due to simulation difficulty in PSIM9. The 10Hz (fo Hz) square pulse with 50 % duty-cycle and its inverted output pulse are ANDed using a 10 kHz (fc Hz) modulating square wave voltage signal with variable duty-cycle which drives the four bidirectional IGBT switches Q1 to Q4 as shown in Fig. 13.2, whose variable voltage output having frequency fo Hz is given to the load. By changing the frequency fo of the square pulse generator the frequency of output voltage can be controlled. The modulating signal frequency fc Hz must be at least twice greater than the desired output frequency fo Hz. The detailed principle of operation of the above converter is shown in Appendix A13.1

13.4 RMS OUTPUT VOLTAGE: A typical output voltage waveform of the above converter is shown in Fig.13.3 below. This is uniform pulse width modulation. Let D_C be the duty cycle of the square pulse carrier and $T_C = 1/f_C$ be its period. Let $T_0 = 1/f_O$ be the period of the output voltage waveform. Let V be the peak value of the output PWM voltage waveform. The following derivation for RMS output voltage waveform holds good:

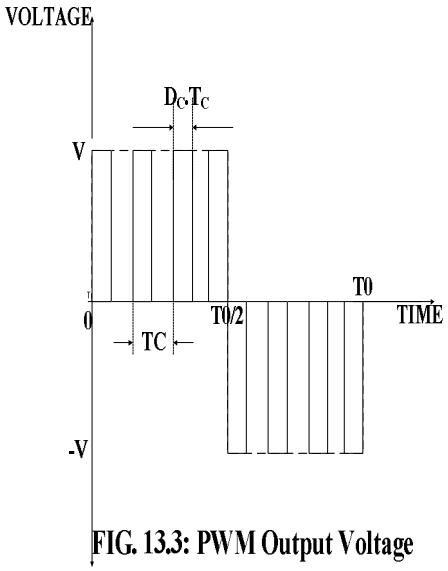


FIG. 13.3: PWM Output Voltage

Number of PWM square pulses for one half cycle of the PWM output voltage $n_p = \frac{T_O}{2T_C}$ (13.1)

Let V_{rms} be the RMS value of the output voltage and T_1 be the time of starting of the first pulse measured from the origin.

$$V_{rms}^2 = \frac{2 * n_p}{T_O} * \left[\int_{T_1}^{T_1 + D_C.T_C} V^2.dt \right] \quad (13.2)$$

$$= \frac{2.V^2.n_p.D_C.T_C}{T_O} \quad (13.3)$$

$$V_{rms} = V * \sqrt{\frac{2.n_p.D_C.T_C}{T_O}} \quad (13.4)$$

$$= V * \sqrt{2.n_p.D_C.T_C.f_O} \quad (13.5)$$

Equations 13.4 and 13.5 gives the RMS value of the PWM output voltage waveform.

13.5 SIMULATION RESULTS: To verify the performance of the proposed single phase PWM AC to single phase AC converter, a model of this was developed in PSIM9, as shown in Fig. 13.2. The DC link voltage is 100 Volts. The carrier frequency is 10 kHz. The clock generator frequency is 1 kHz with 50 % duty cycle. The duty cycle for the carrier generator was initially set to 0.8. The simulation results are shown in Fig. 13.4(A) to (G). The duty cycle of the carrier generator was then set to 0.5 and the simulation results are shown in Fig. 13.5(A) to Fig. 13.5(G). The simulation results with the duty cycle of the carrier generator set to 0.2 are shown in Fig. 13.6(A) to Fig. 13.6(G). To study the output frequency variation capability, the simulation of the above converter was carried out for a fo value of 10 Hz. The clock frequency was set to 10 Hz with a duty cycle of 50 %. The carrier frequency was chosen to be 1 kHz. The duty cycles of the carrier generator used for simulation were 0.8, 0.5 and 0.2 respectively. The simulation results for these three values of duty cycles are shown above in Fig. 13.7(A) to Fig. 13.7(G), Fig. 13.8(A) to Fig. 13.8(G) and Fig. 13.9(A) to Fig. 13.9(G) respectively.

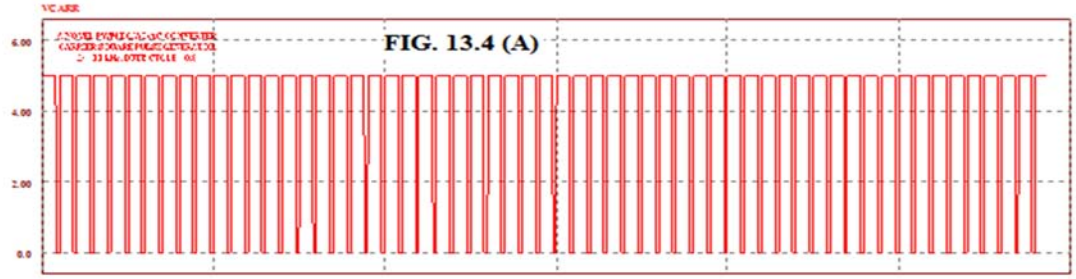


FIG. 13.4 (A)

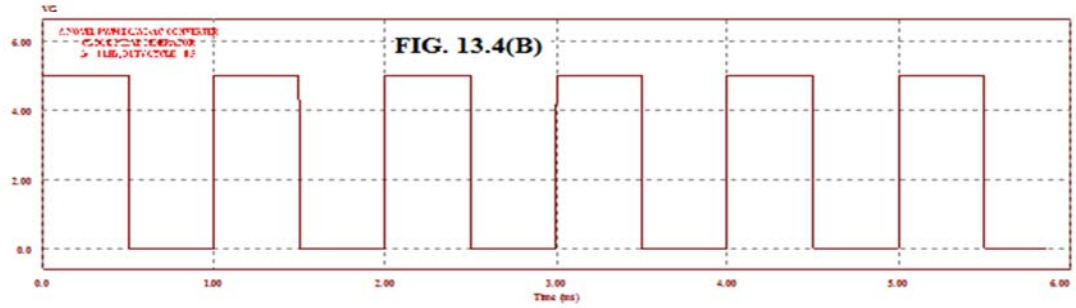


FIG. 13.4(B)

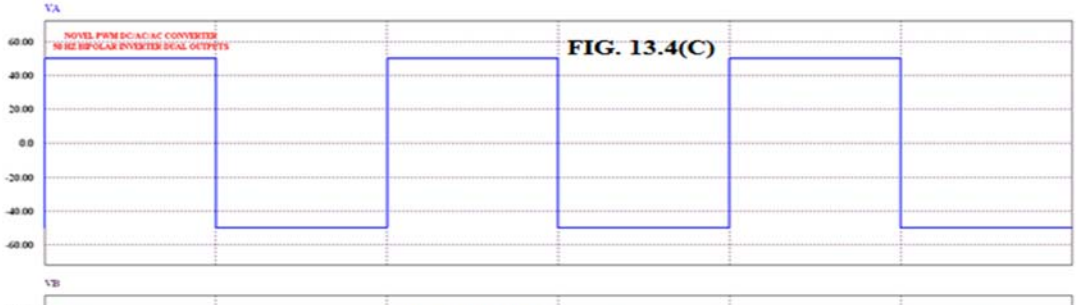


FIG. 13.4(C)

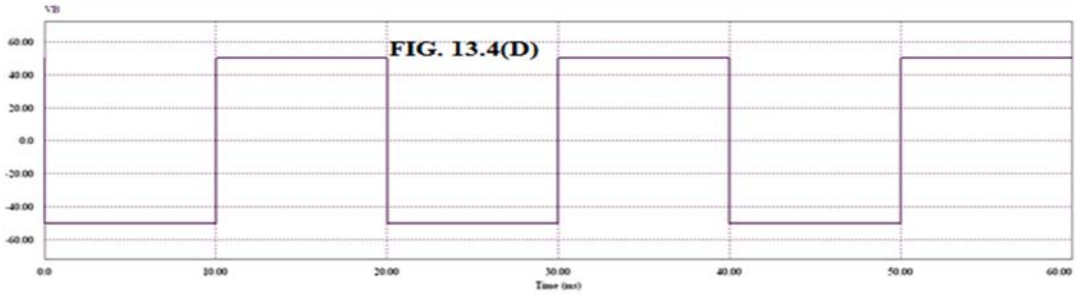


FIG. 13.4(D)

FIG. 13.4(E)

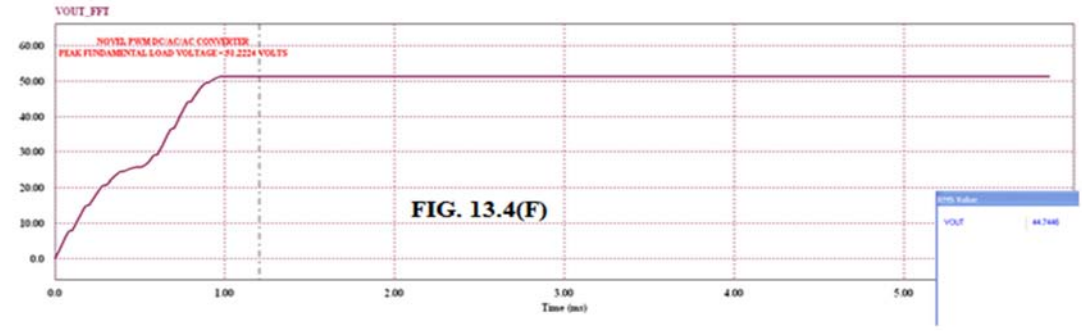


FIG. 13.4(F)

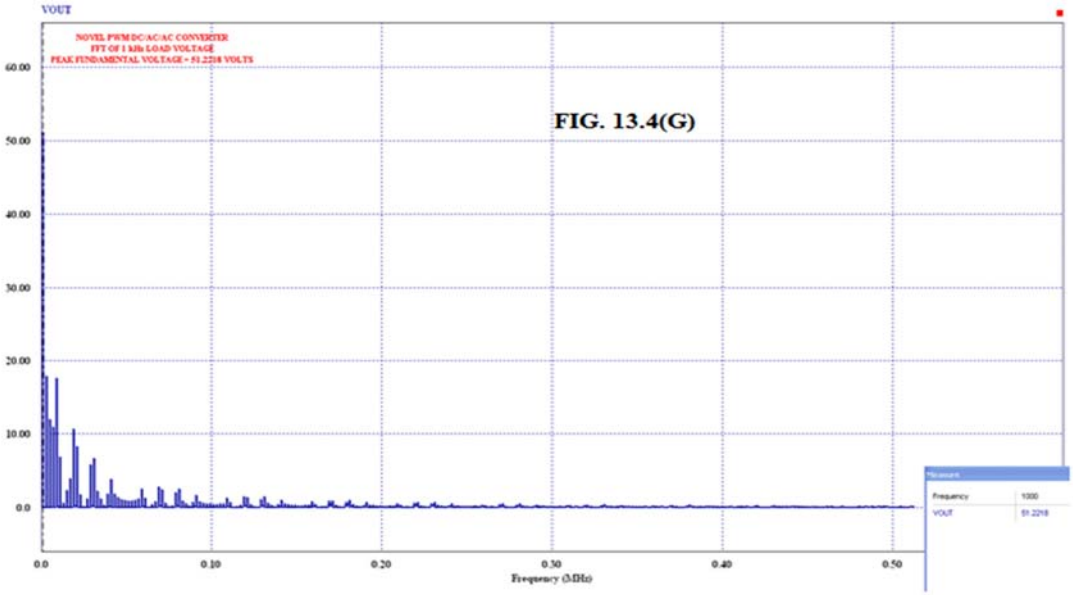


FIG. 13.4(G)

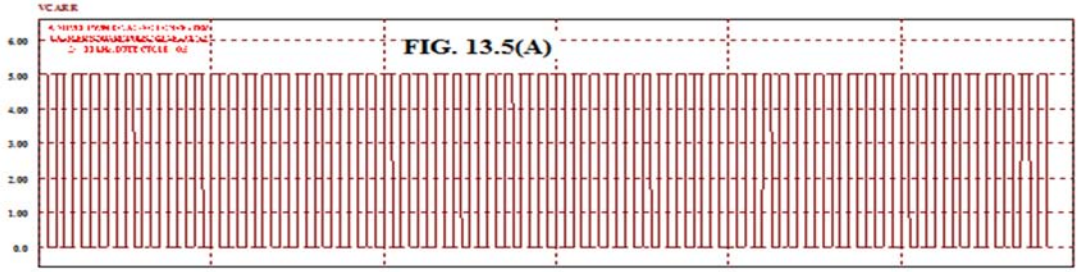


FIG. 13.5(A)

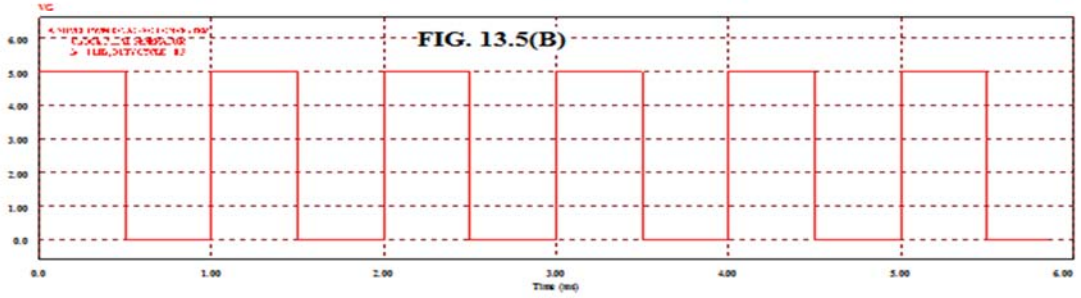


FIG. 13.5(B)

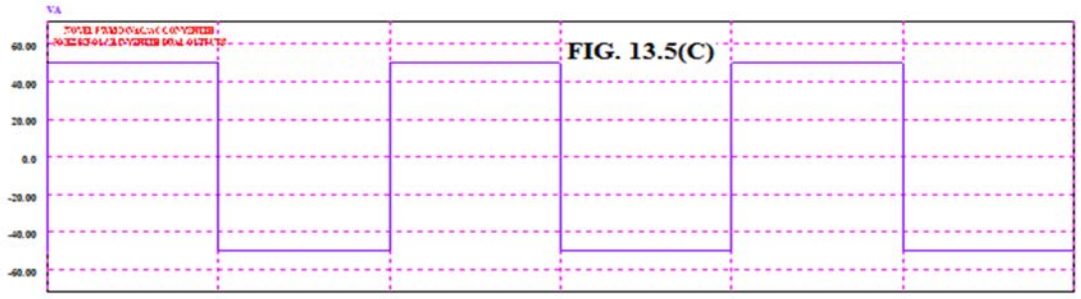


FIG. 13.5(C)

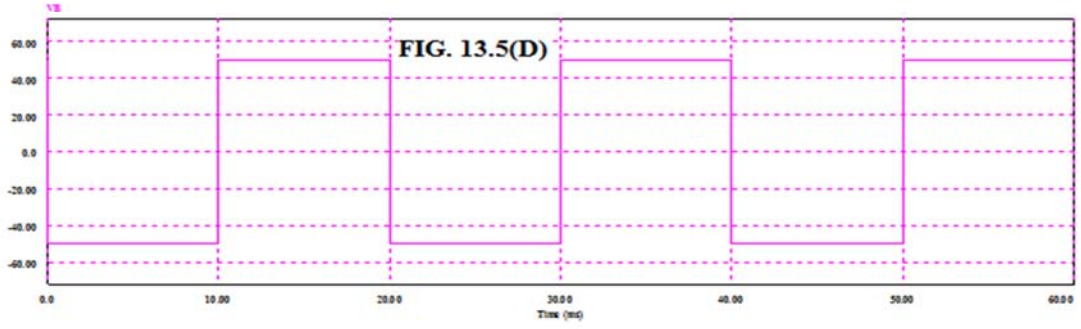


FIG. 13.5(D)

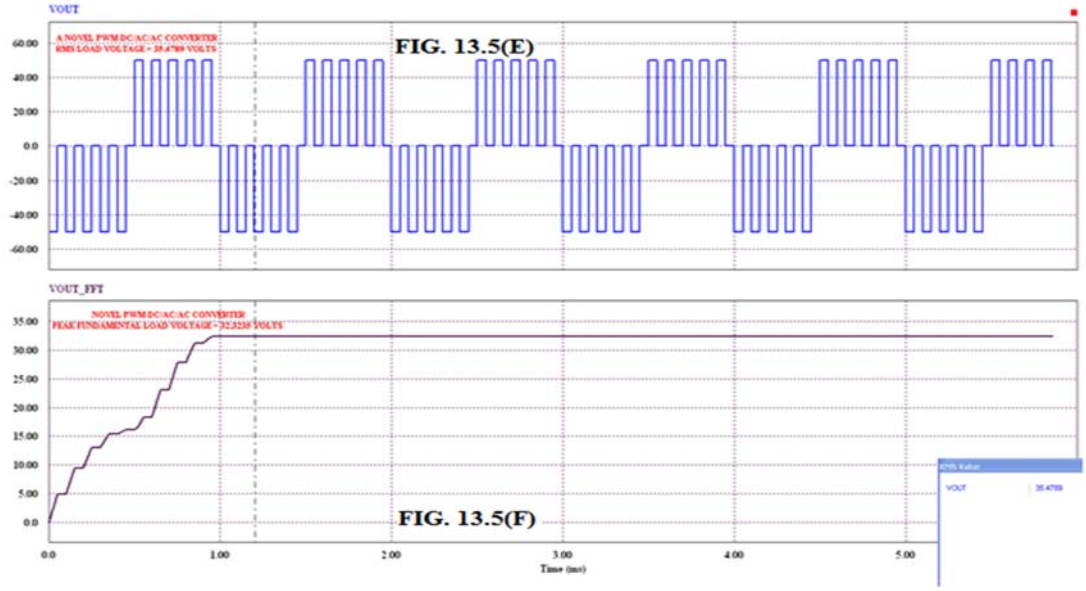


FIG. 13.5(E)

FIG. 13.5(F)

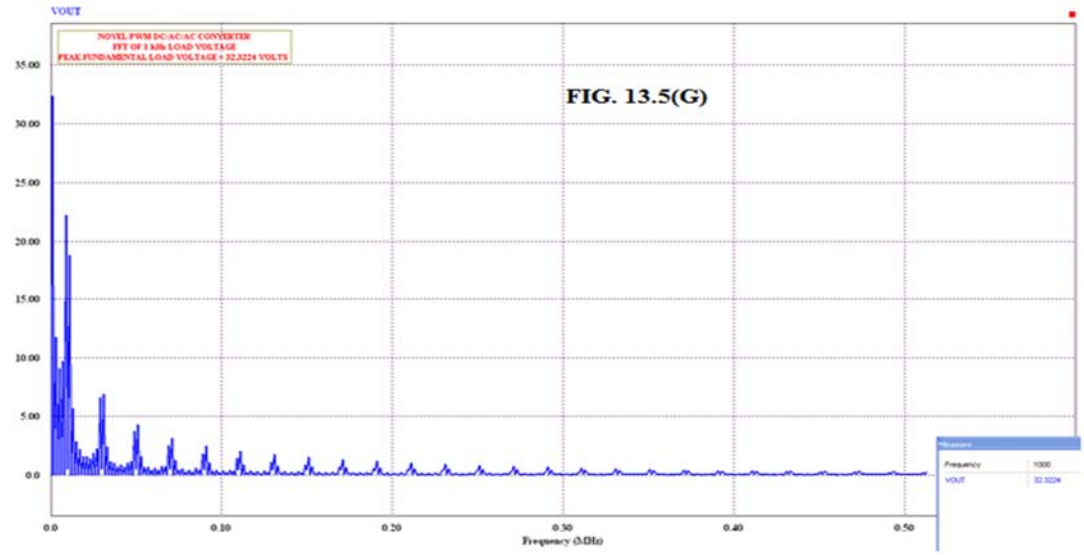


FIG. 13.5(G)

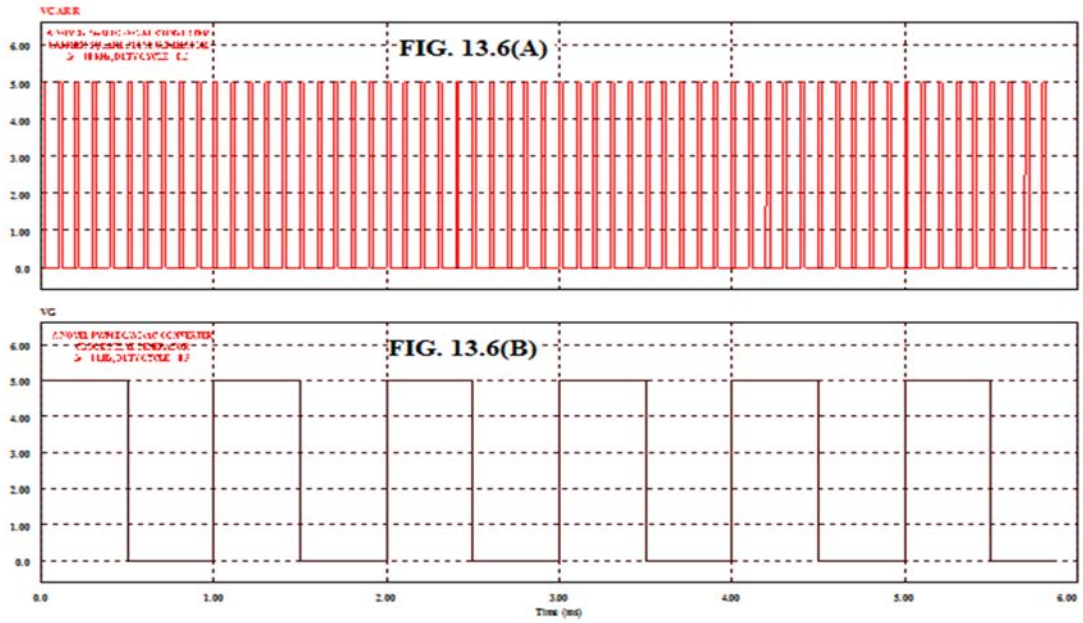


FIG. 13.6(A)

FIG. 13.6(B)

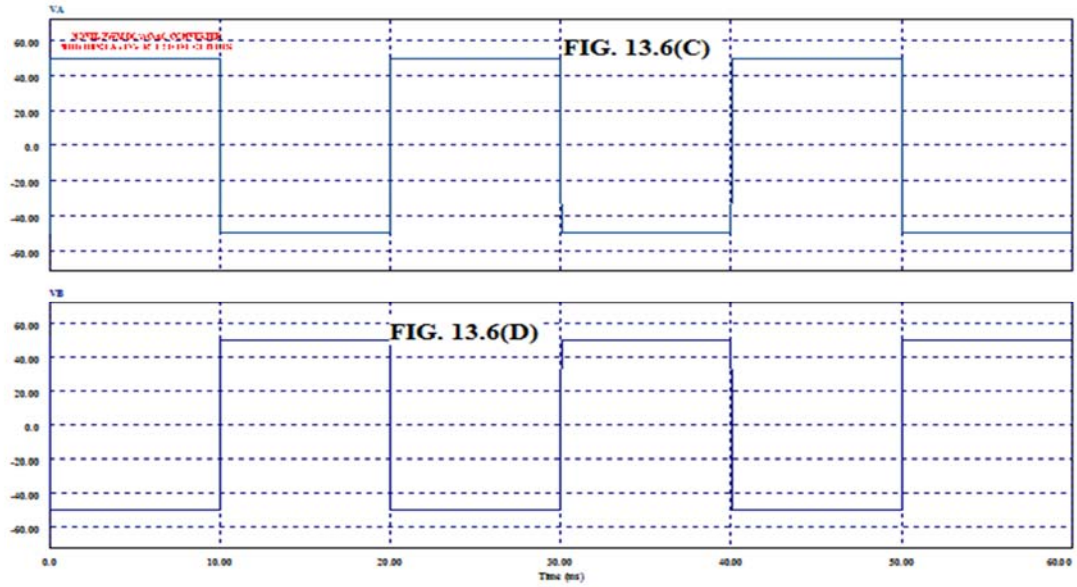


FIG. 13.6(C)

FIG. 13.6(D)

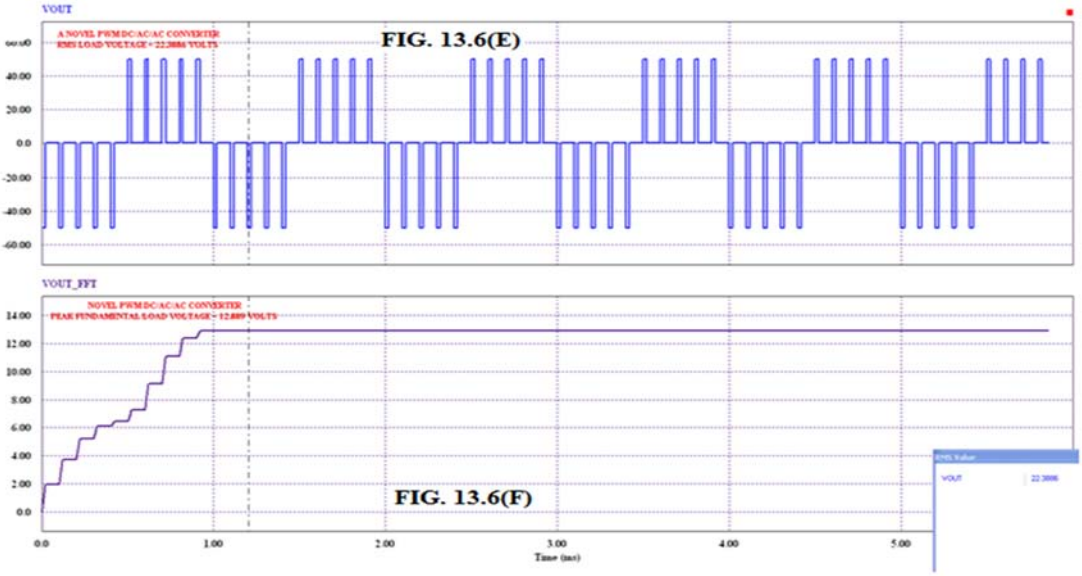


FIG. 13.6(E)

FIG. 13.6(F)

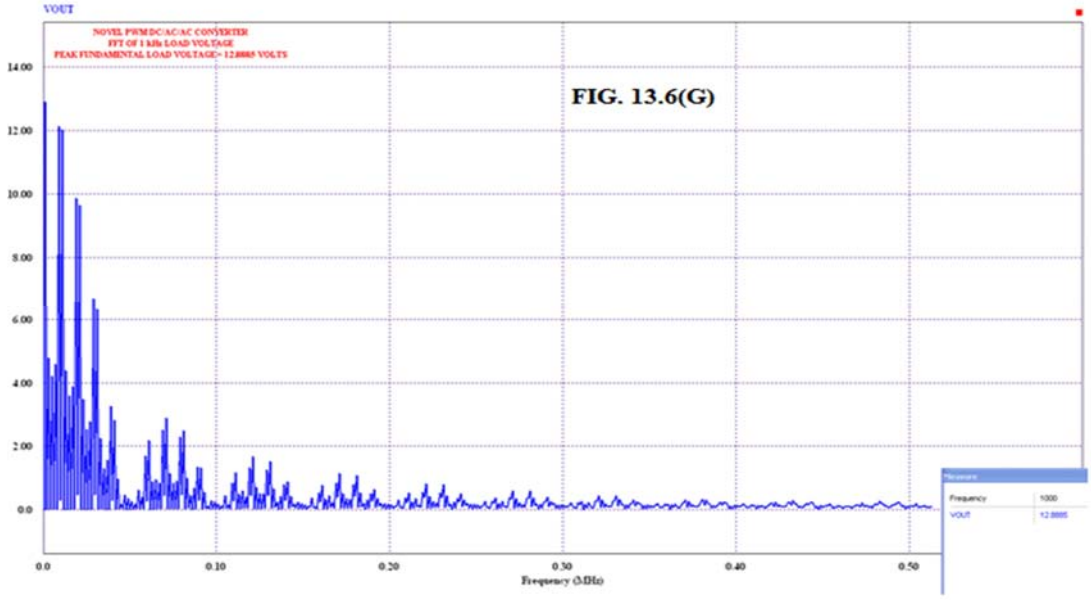


FIG. 13.6(G)

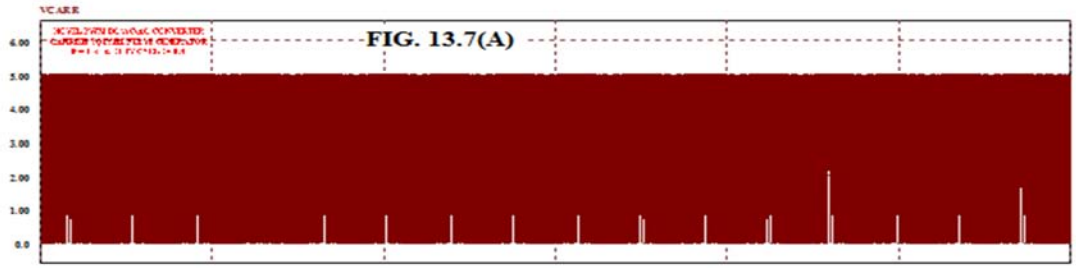


FIG. 13.7(A)

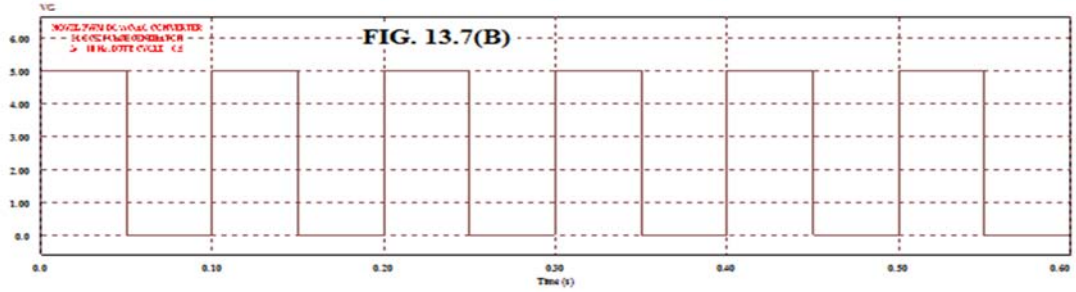


FIG. 13.7(B)

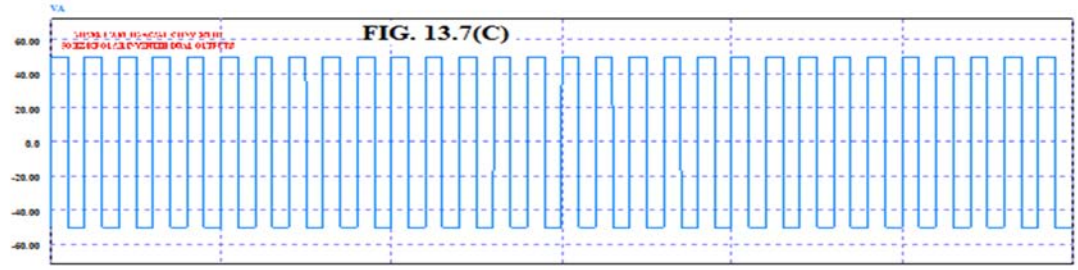


FIG. 13.7(C)

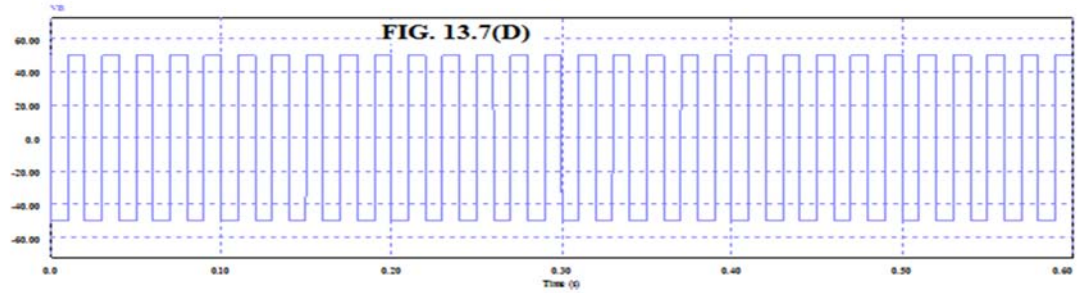


FIG. 13.7(D)

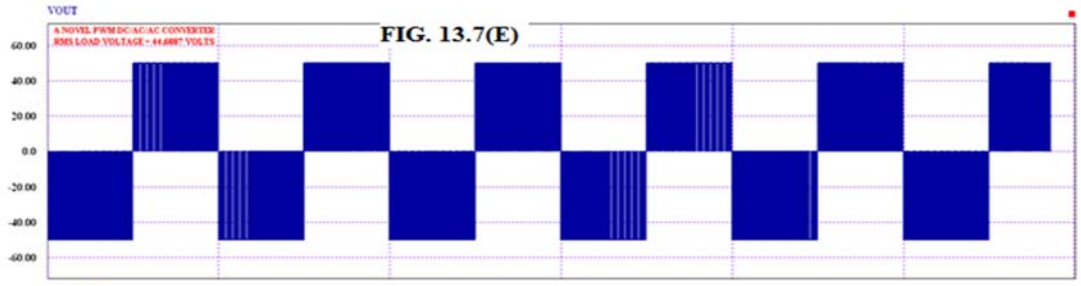


FIG. 13.7(E)

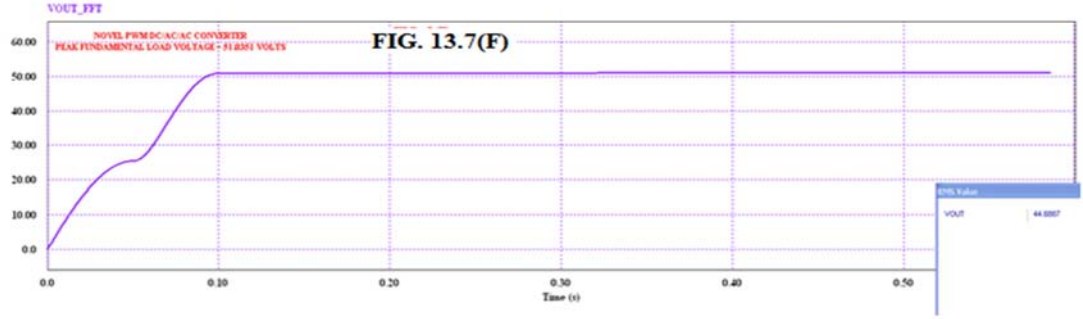


FIG. 13.7(F)

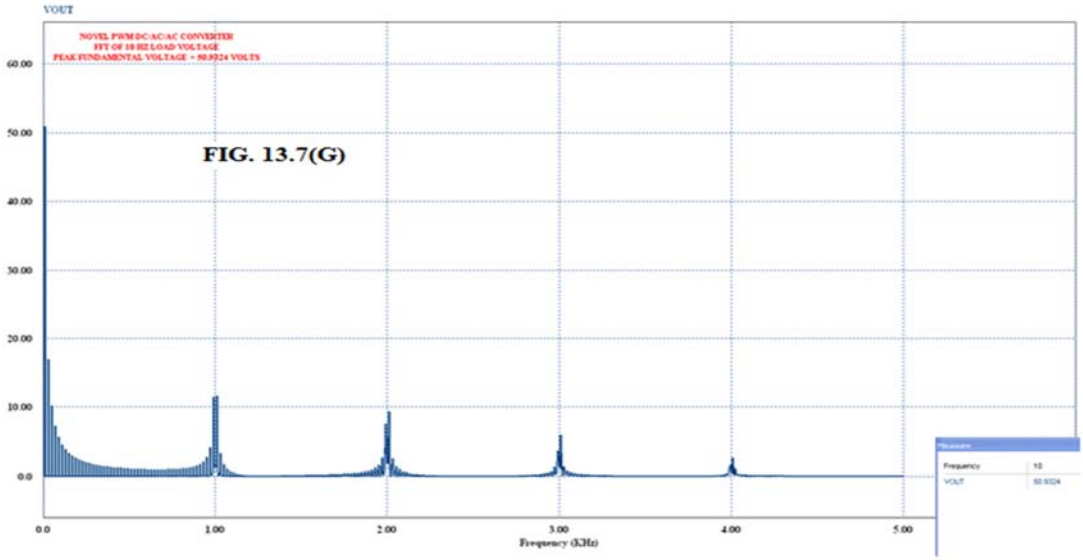


FIG. 13.7(G)

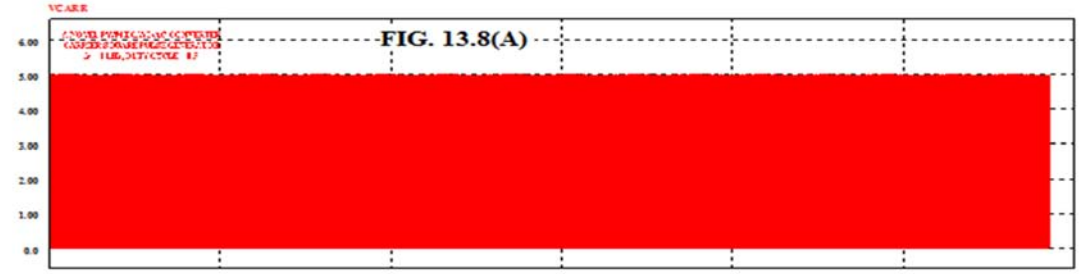


FIG. 13.8(A)

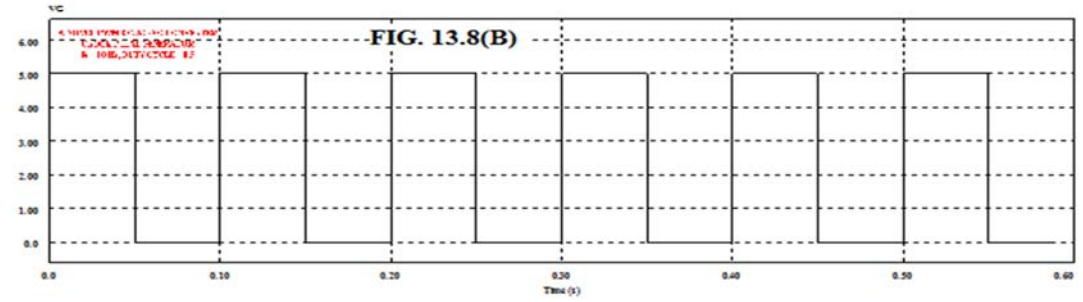


FIG. 13.8(B)

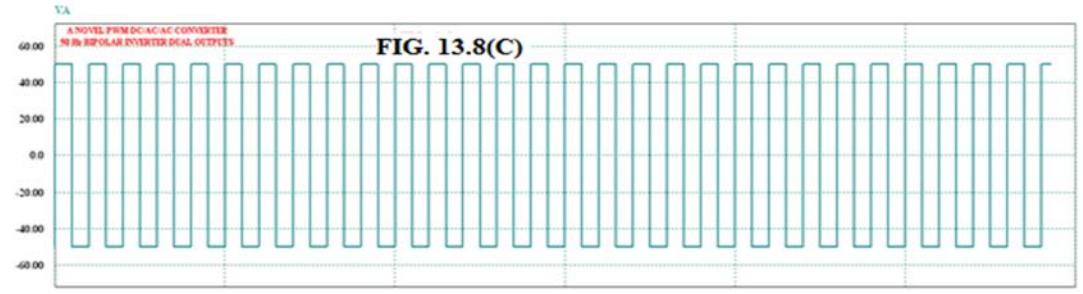


FIG. 13.8(C)

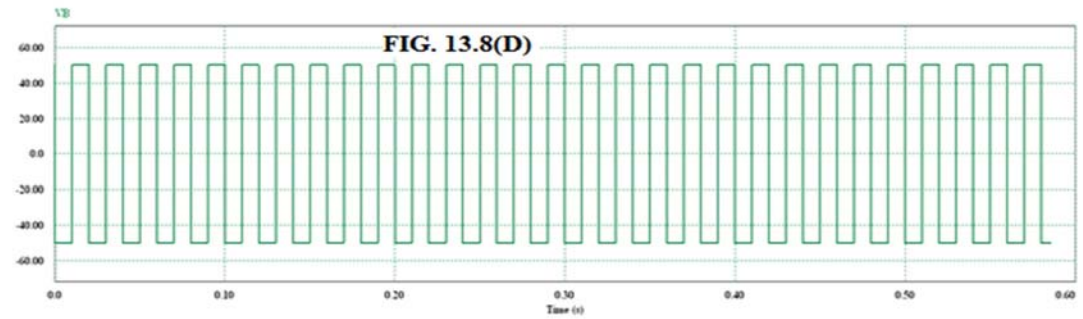


FIG. 13.8(D)

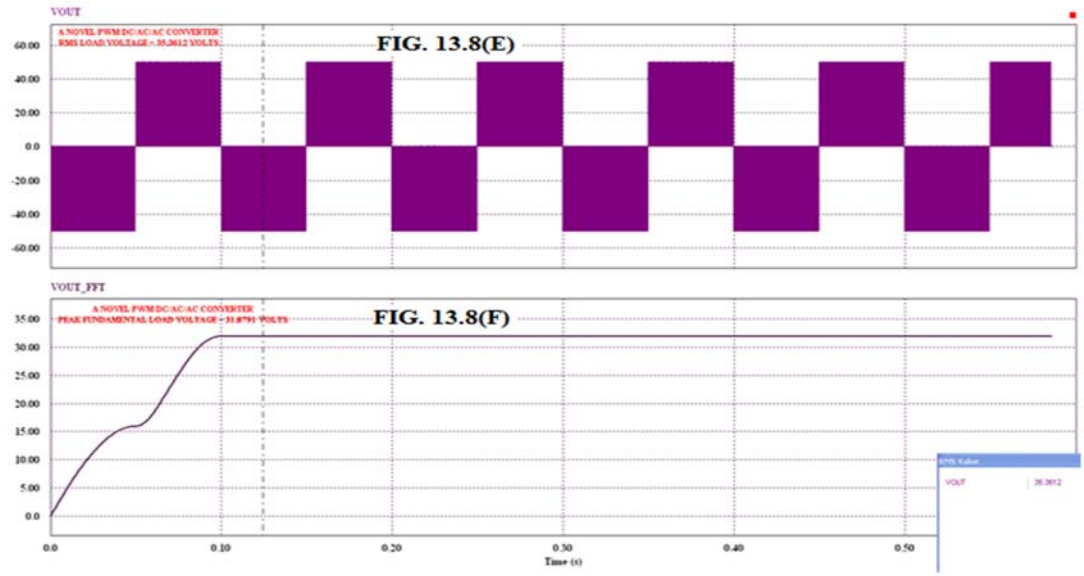


FIG. 13.8(E)

FIG. 13.8(F)

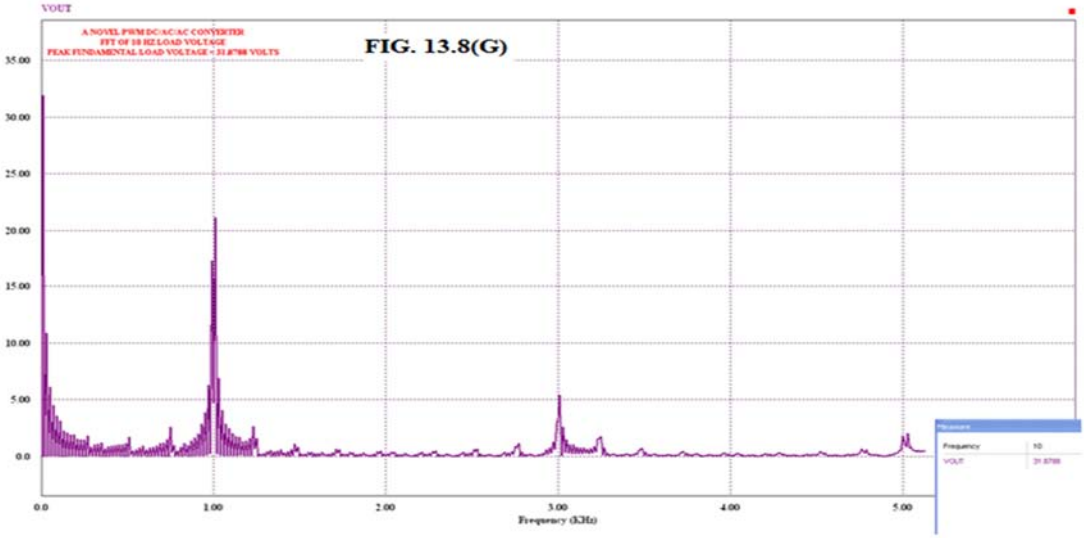


FIG. 13.8(G)

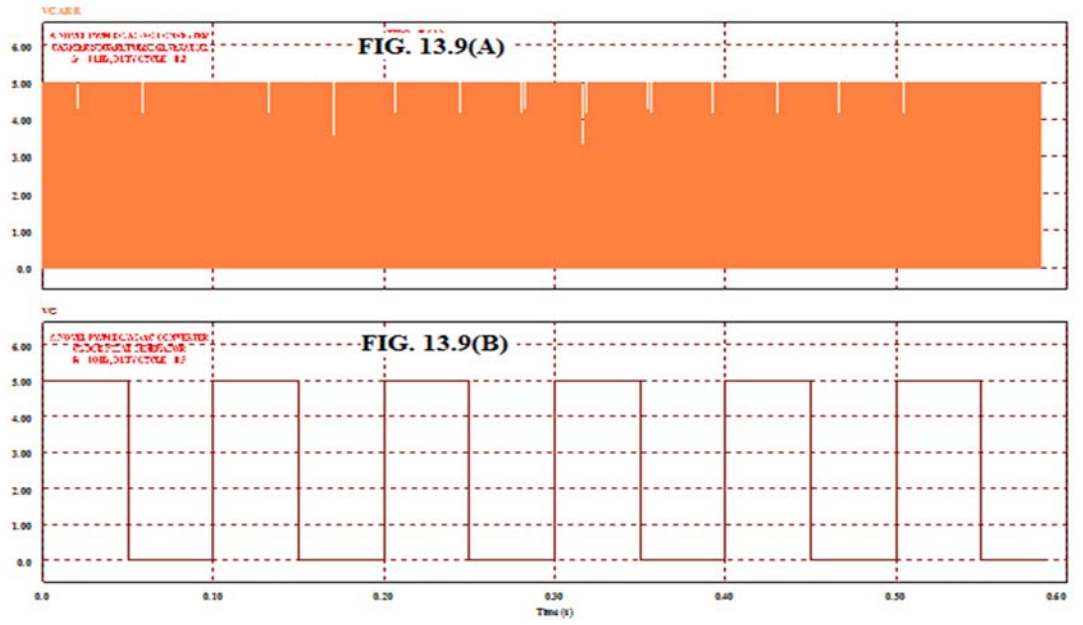
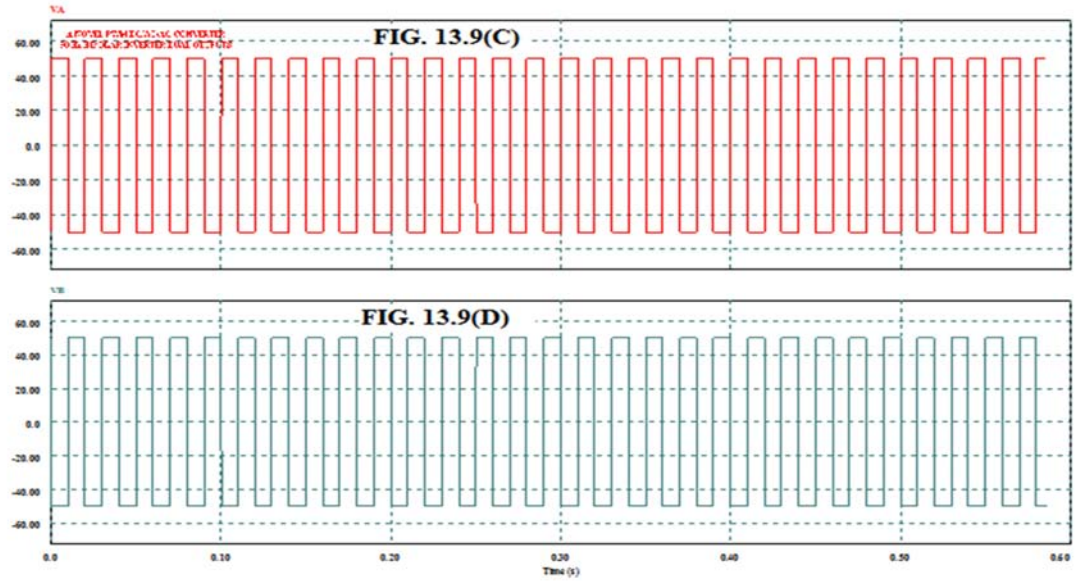
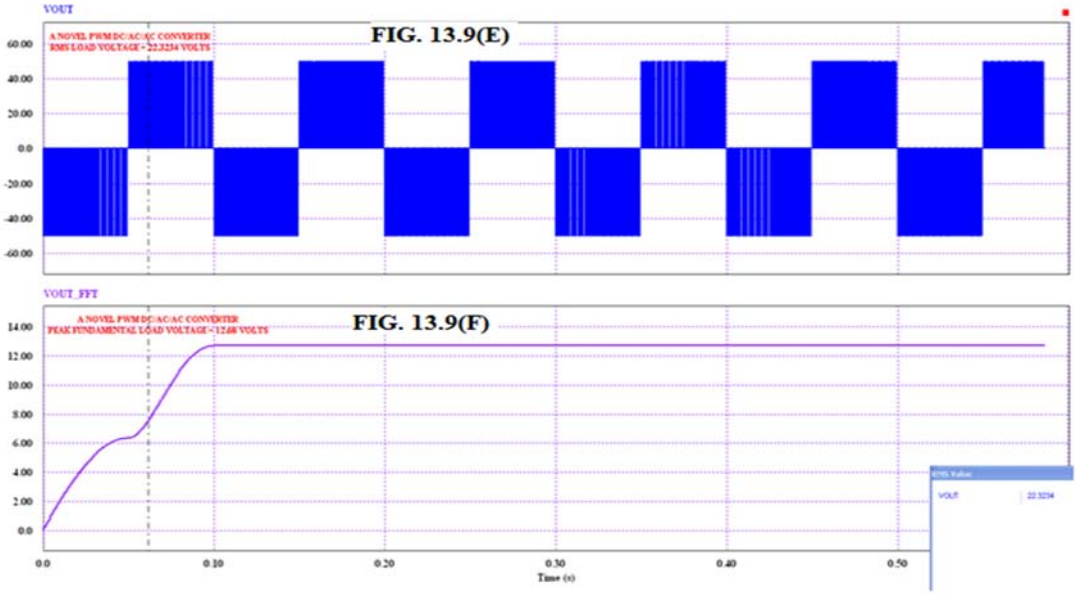
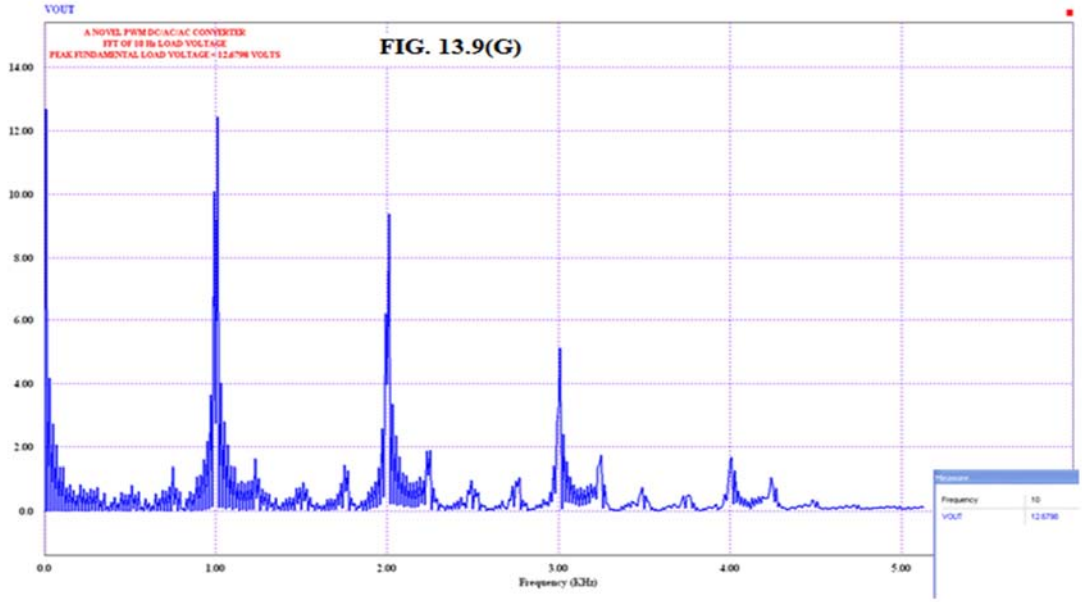


FIG. 13.9(A)

FIG. 13.9(B)


VA
FIG. 13.9(C)
VB
FIG. 13.9(D)
Time (s)


VOUT
FIG. 13.9(E)
VOUT_FFT
FIG. 13.9(F)
Time (s)


VOUT
FIG. 13.9(G)
Frequency (KHz)

13.6 DISCUSSION OF RESULTS: From the simulation results it is seen that a variable frequency Pulse Width Modulated variable voltage output is obtained at the load terminal from a constant 50 Hz frequency AC input voltage. The variable frequency at the load terminal is obtained by selecting the appropriate clock frequency to drive the IGBT bidirectional switches. The variable voltage magnitude at the load terminal is obtained by varying the duty-cycle of the carrier switching frequency.

13.7 THREE PHASE AC TO THREE PHASE AC CONVERTER USING A DC LINK: The block diagram of the Three Phase fixed supply frequency AC to Three Phase variable frequency AC converter using an intermediate DC link is shown in Fig.13.10. The block diagram is explained below:

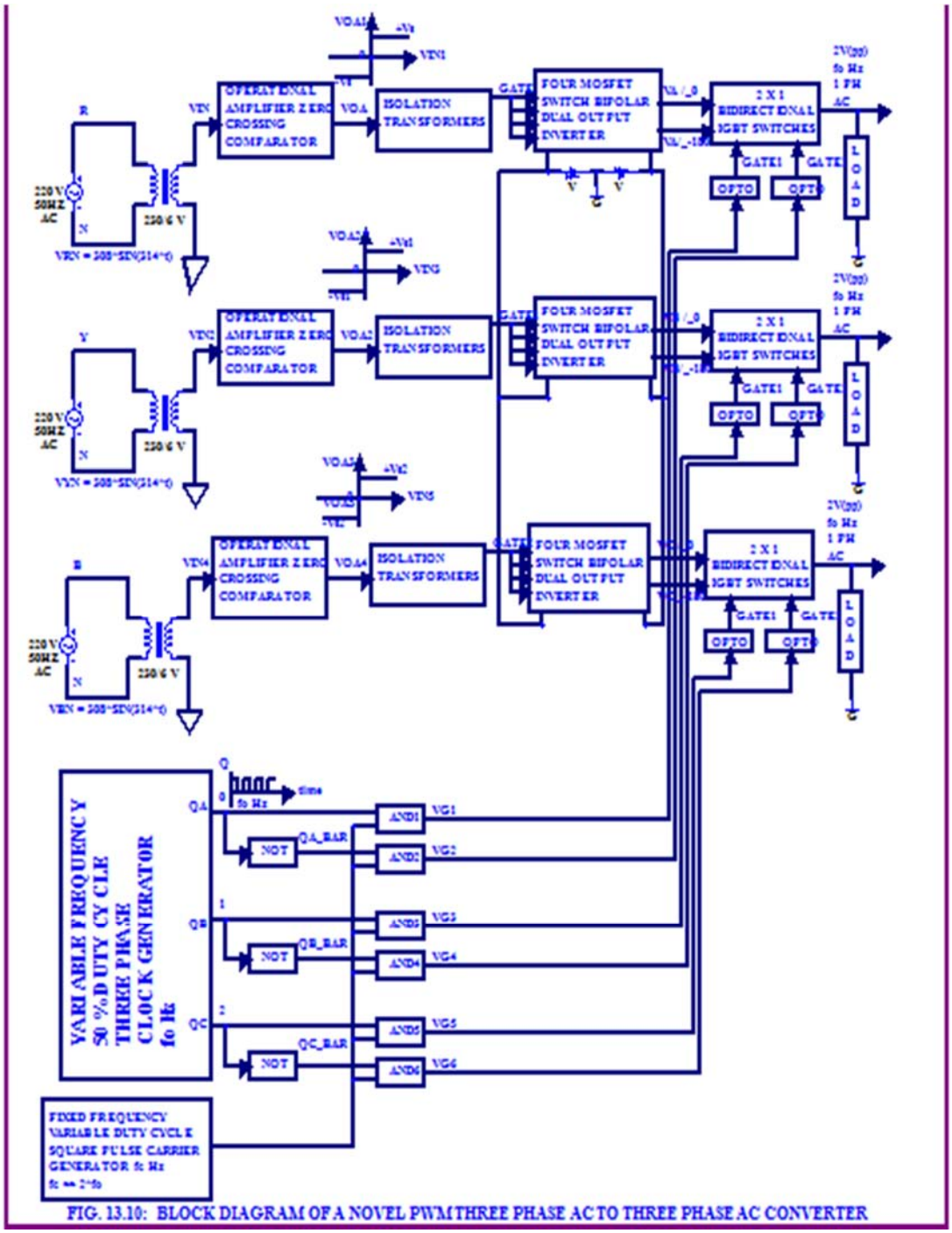


FIG. 13.10: BLOCK DIAGRAM OF A NOVEL PWM THREE PHASE AC TO THREE PHASE AC CONVERTER

- The supply mains is a 220 Volts (Line to Neutral), 50 Hz Three Phase AC.
- The step down transformer 230/6 V is connected to each phase of the supply mains.
- The secondary 6 V of each phase is connected to op. amplifier zero crossing comparator.
- The output of the zero crossing comparator forms the gate drive input to all the four MOSFET switches forming the bipolar dual output inverter in each phase.
- The bipolar dual output inverter in each phase consists of two legs. Each leg is a pair of N and P type MOSFETs connected in series. The two parallel legs of the inverter are connected to the DC source which forms the DC link. The two outputs of this inverter in each phase are VA=V/_0, VA=V/_-180, VB=V/_-120, VB=V/_-300 and VC=V/-240, VC=V/_-420 with a frequency of 50 Hz, where 2V is the DC link voltage. These two outputs of inverter in each phase are fed to the IGBT bidirectional switches corresponding to each output phase.
- There are two IGBT bidirectional switches in each output phase. The four gates of the two IGBT bidirectional switches in each output phase are cross connected. This is different from the mode of connection used in conventional matrix converter. The output of this bidirectional switches is connected to the three phase load.
- The three phase clock generator output is a square pulse for each phase having a frequency of fo Hz with 50 % duty cycle. The clock QA, QB and QC corresponding to each output phase are separated from each other by a phase difference of To/3 seconds, where To = 1/fo. This frequency fo Hz is variable.
- The carrier generator output is a square pulse having a pre-calculated fixed frequency of fc Hz with a variable duty-cycle. The carrier frequency fc Hz must be at least two times more greater than the desired output frequency of fo Hz.
- The load voltage Vo is a Pulse Width Modulated square wave AC with a peak to peak value of 2V Volts and frequency fo Hz.
- By varying the duty-cycle of the square pulse carrier generator, the magnitude of the output voltage Vo can be controlled.

13.8 MODEL OF A PWM THREE PHASE AC TO THREE PHASE AC CONVERTER: The model schematic of the novel PWM Three Phase AC to three phase AC converter is shown in Fig. 13.11. One op.amp. zero crossing comparator (ZCC) for each input phase drives the four MOSFET switches corresponding to each input phase to produce bipolar dual output voltages which are respectively given to four IGBTs forming two bidirectional switches connected to each output phase. In Fig. 13.11, MOSFETs M1 and M2 and N and P type respectively. Similar is the case with M3-M4, M5-M6, M7-M8, M9-M10 and M11-M12 pair of MOSFETs. In Fig.13.11, the isolation transformers are not shown next to op.amp. ZCC due to simulation difficulty in PSIM9. The three phase square clock pulse with 50 % duty-cycle and frequency fo Hz is modulated using a variable duty-cycle square pulse carrier signal generator. Three phase clock and its inverted pulse are ANDed with square pulse carrier wave and these pair of gate pulses drive the two pairs of bidirectional IGBT switches corresponding to each output phase whose variable frequency variable three phase voltage output is given to the load. The gates of the IGBTs Q1-Q4, Q5-Q8 and Q9-Q12 are cross connected.

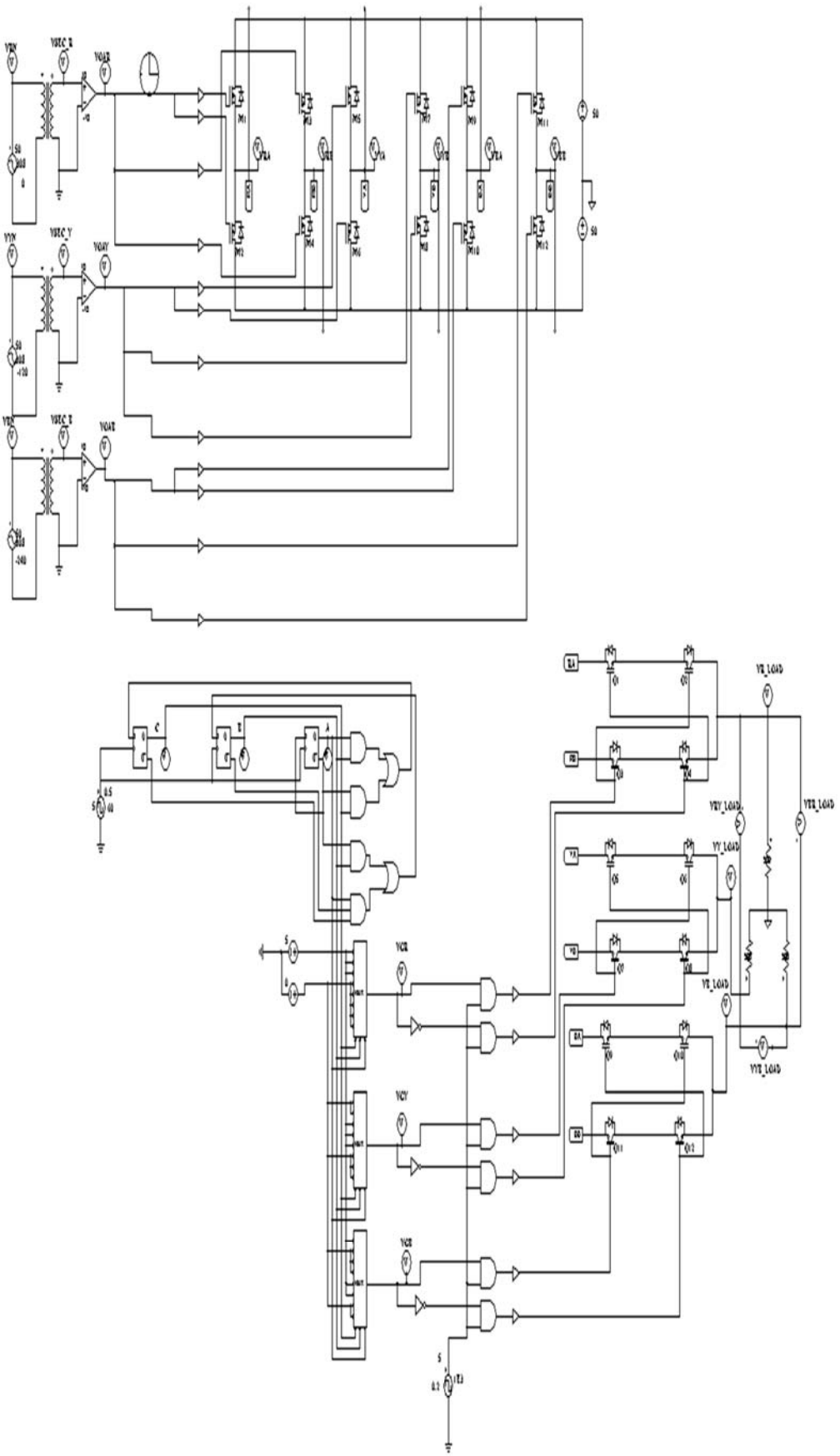


FIG. 13.11: A NOVEL PWM THREE PHASE AC TO THREE PHASE AC CONVERTER

The three phase clock of frequency fo Hz is developed here as given below:

A modulo six counter which counts from 0 to 5 in the continuous up sequence is developed using D filp-flop. The truth table for designing the modulo six counter using D flip-flops is shown in Table 13.1. For D flip-flops the next state is mapped to find the three control logic for the D input of C, B

TABLE 13.1
D-Flip-flop Truth Table

Sl.No.	Present state			Next state		
	C	B	A	C	B	A
1	0	0	0	0	0	1
2	0	0	1	0	1	0
3	0	1	0	0	1	1
4	0	1	1	1	0	0
5	1	0	0	1	0	1
6	1	0	1	0	0	0

C BA	0 0	0 1	1 1	1 0
0	1	0	0	1
1	1	0	X	X

A input map. $D_A = /A$ (A)

C BA	0 0	0 1	1 1	1 0
0	0	1	0	1
1	0	0	X	X

B input map. $D_B = /C./B.A + B./A$ (B)

C BA	0 0	0 1	1 1	1 0
0	0	0	1	0
1	1	0	X	X

C input map. $D_C = C./A + B.A$ (C)

FIG. 13.12: K_Map for Modulo Six Counter

and A. The control logic for the D input of flip-flops A, B and C are derived using K-maps as shown in Fig. 13.12(a), (b) and (c). The clock input to this counter has a frequency of 6*fo, where fo Hz is the desired output frequency. The three bit output of the counter is decoded using three 8 line to 1 line Multiplexer. Each of these multiplexers give a logic HIGH output corresponding to the minimum terms Σm(0,1,2), Σm(2,3,4), Σm(4,5,0). The output of these MUX and their corresponding inverted output drives the four bidirectional switches in each of the three output phase. Another method of switching the gates of IGBTs Q1-Q12 using PIC16F84A microcontroller is given in Appendix I.

13.9 SIMULATION RESULTS: To verify the performance of the proposed PWM three phase AC to three phase AC converter, a model of this was developed in PSIM9, as shown in Fig. 13.11. The DC link voltage is 100 Volts. The carrier frequency is 10 kHz. The clock frequency was set to 6 kHz so that frequency of the square pulse used for driving the bidirectional switches is 1 kHz with 50% duty-cycle. The output frequency is 1 kHz. The duty cycle for the carrier generator was initially set to 0.2. The simulation results are shown in Fig. 13.13(A) to (C) and Fig. 13.14(A) to (C) for the three phase line to neutral and line to line output voltages respectively. The duty cycle of the carrier generator was then set to 0.8 and the simulation results in the above order are shown in Fig. 13.15(A) to (C) and Fig. 13.16(A) to (C). To study the output frequency variation capability, the simulation of the above converter was carried out for an output frequency value of 10 Hz. The clock frequency was set to 60 Hz, so that the frequency of the square pulse driving the bidirectional switches is 10 Hz with 50% duty-cycle. The carrier frequency was chosen to be 1 kHz with variable duty-cycle. The duty cycles of the carrier generator used for simulation were 0.2 and 0.8 respectively. The simulation

results for these two values of duty cycles in the above order are shown above in Fig. 13.17(A) to (C), Fig. 13.18(A) to (C) Fig. 13.19(A) to (C) and Fig. 13.20(A) to (C) respectively.

13.10 DISCUSSION OF RESULTS: From the simulation results it is seen that a variable frequency Pulse Width Modulated Three Phase variable voltage output is obtained at the load terminal from a constant 50 Hz frequency Three Phase AC input. The variable frequency at the load terminal is obtained by selecting the appropriate clock frequency to drive the IGBT bidirectional switches. The variable voltage magnitude at the load terminal is obtained by varying the duty-cycle of the carrier square wave switching pulse.

Both the single phase AC to single phase AC and the three phase AC to three phase AC converter presented above converts the fixed supply frequency AC voltage to variable frequency AC output voltage. This is a new method in the sense the topology of connecting the IGBT bidirectional switches and its gate connections are much different from the conventional matrix converter. The above topology presents a new method of obtaining variable frequency AC output voltage from a supply frequency input voltage. The gate drive can be easily implemented using analog and digital ICs or microcontrollers whereas gate drive for conventional matrix converters require algorithms to be implemented in dSPACE or using Digital Signal Processors.

13.11 CONCLUSIONS: A novel method of generating a variable frequency variable single phase and variable Three Phase AC output voltage across the load from a single phase and three phase 50 Hz AC input voltage is presented. The PWM scheme used is well known. The topology of the DC to 50 Hz AC single phase and three phase dual inverter using N and P MOSFETs with 180 degree phase difference in the output voltage and the topology of the IGBT bidirectional switches and their gate connection of the single phase AC to single phase AC and Three Phase AC to Three Phase AC converter are new.

A13.1 APPENDIX: Referring to Fig. 13.2, the working of the dual MOSFET inverter using N and P MOSFETs in series is explained below:

The 220 Volts single phase 50 Hz sine wave AC input voltage and the 6V transformer secondary output voltage are shown in Fig. A13.1. During the positive half cycle of the transformer secondary input voltage, the output OA of the Op.Amplifier zero crossing comparator (ZCC) is driven to positive saturation and it is +10 V and during the negative half cycle of this input voltage, the ZCC output OA is driven to negative saturation and it is -10V. This is shown in Fig.A13.1. During the positive half cycle of the ZCC output OA, N MOSFETs M1 and M4 conducts, the output VA and VB with respect to DC link ground are respectively +Vdc/2 (+50 V) and –Vdc/2 (-50 V) respectively, where Vdc is the DC link voltage. Similarly during the negative half cycle of the ZCC output OA, P MOSFETs M2 and M3 conducts, the output VA and VB with respect to DC link ground are respectively -Vdc/2 (-50 V) and +Vdc/2 (+50 V) respectively. This is shown in Fig. A13.1.

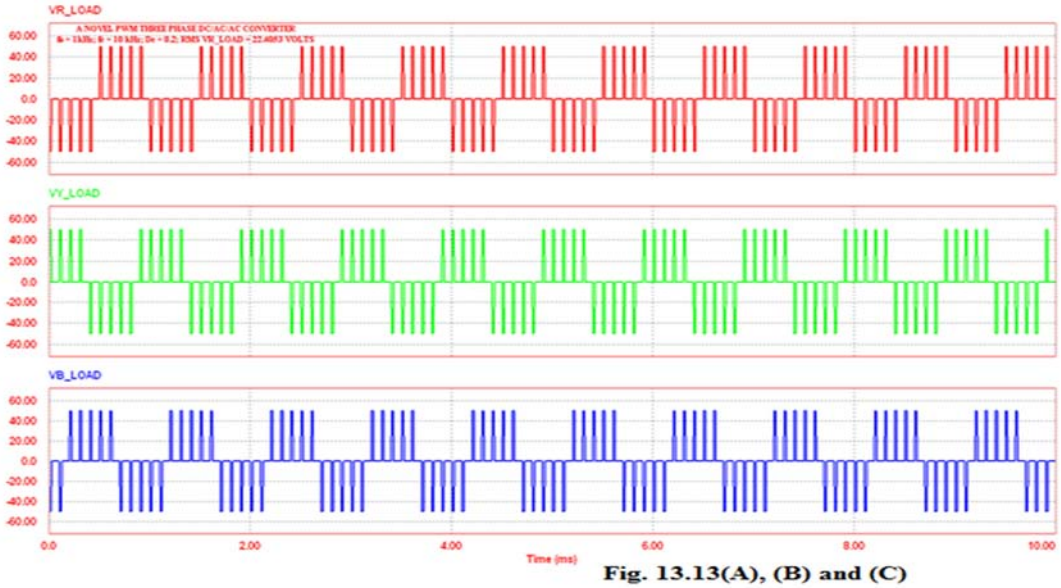


Fig. 13.13(A), (B) and (C)

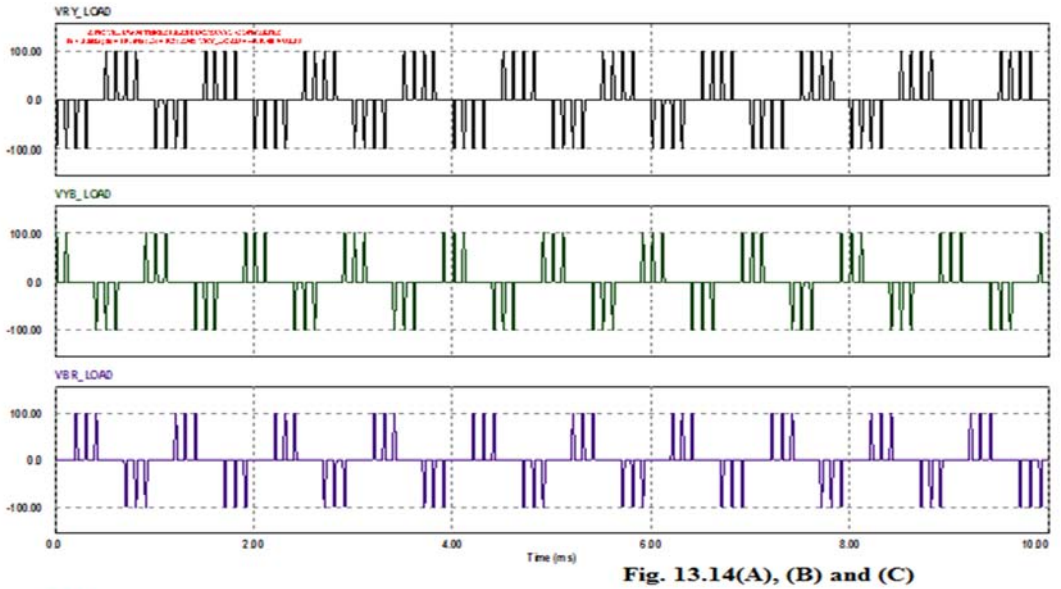


Fig. 13.14(A), (B) and (C)

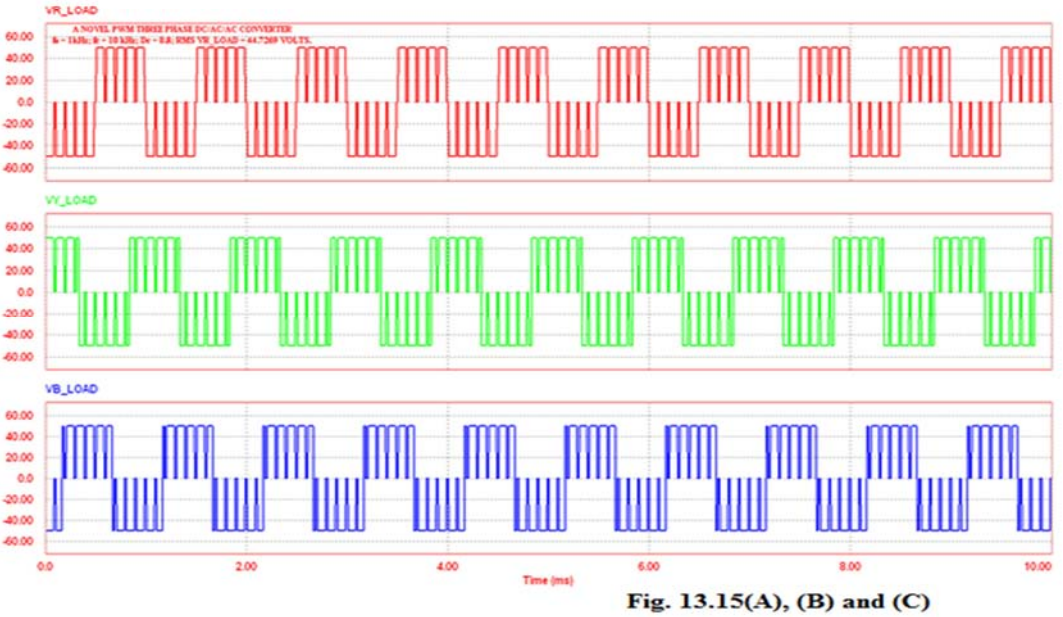


Fig. 13.15(A), (B) and (C)

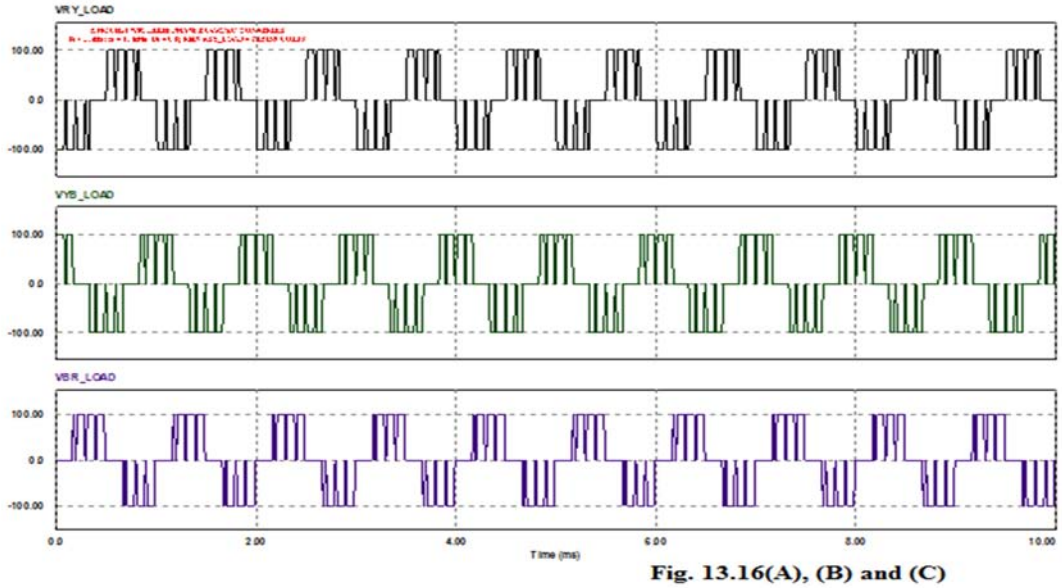


Fig. 13.16(A), (B) and (C)

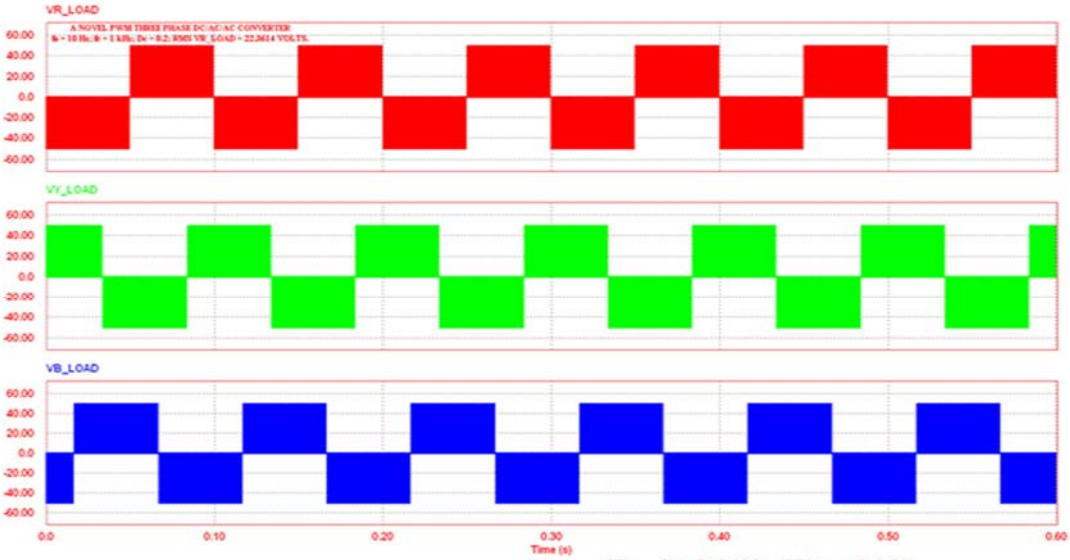


Fig. 13.17(A), (B) and (C)

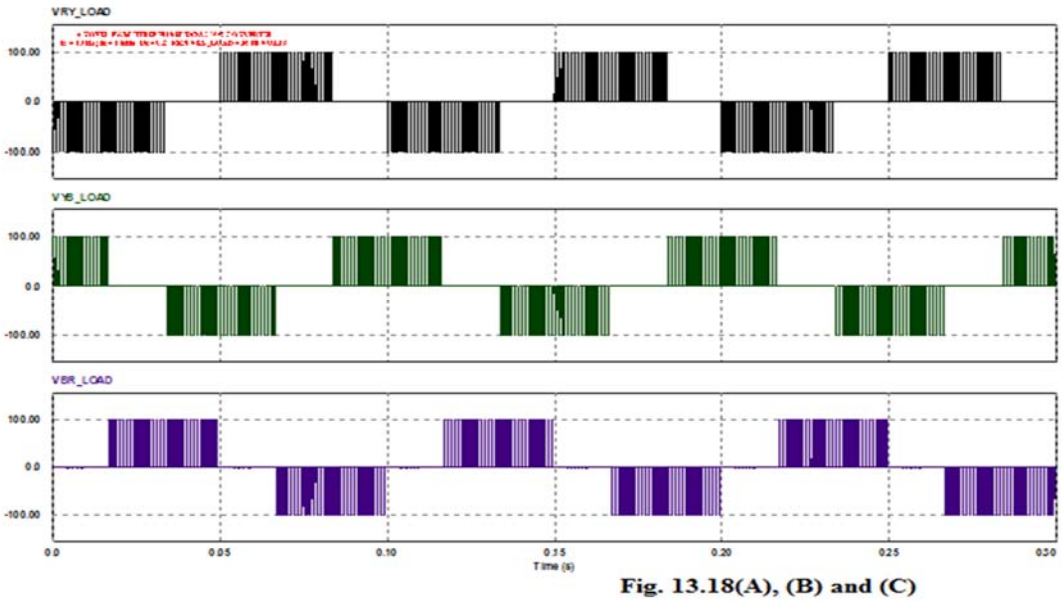


Fig. 13.18(A), (B) and (C)

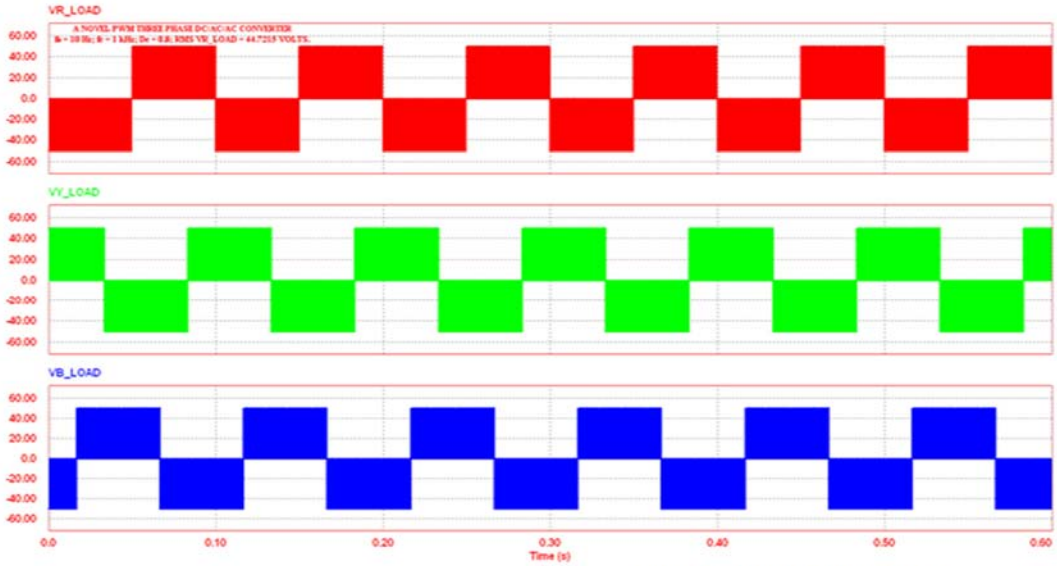


Fig. 13.19(A), (B) and (C)

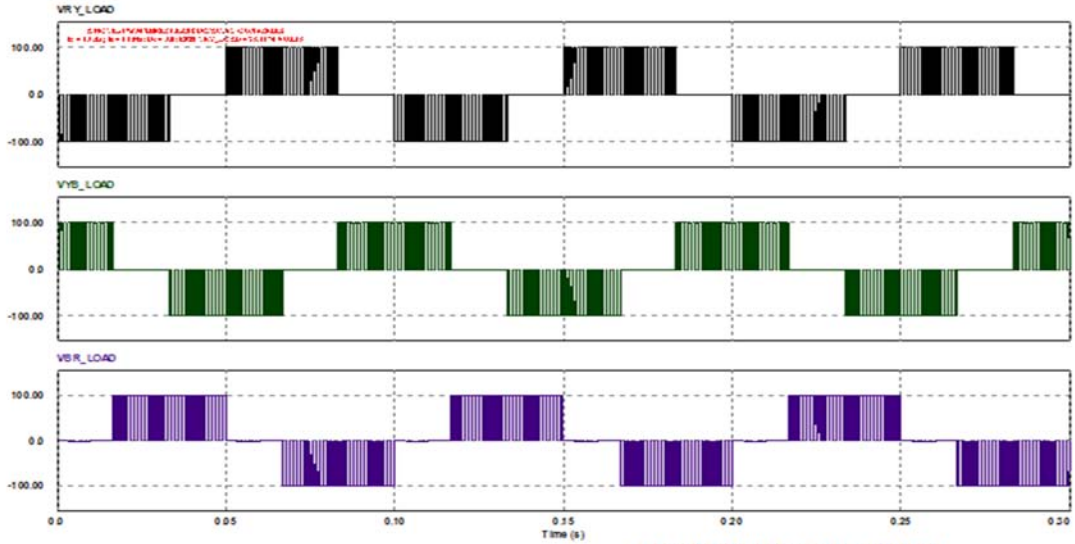
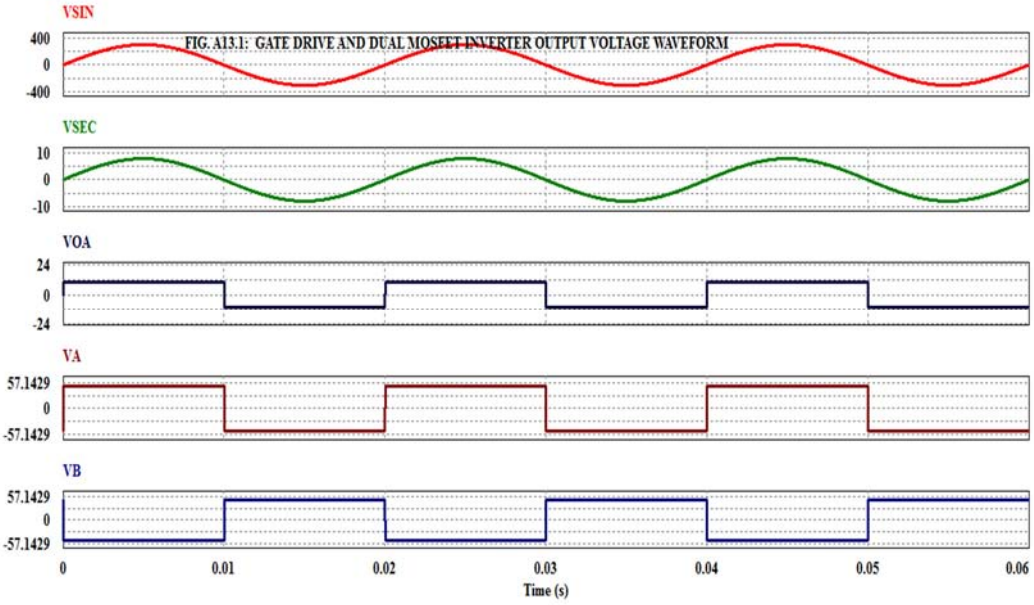


Fig. 13.20(A), (B) and (C)



Referring to Fig. 13.2, the working principle of the IGBT bidirectional switch inverter is given below:

Now consider that the period of the input voltage VA and VB is T and that of the clock switching the IGBT bidirectional switches is To with 50% duty-cycle. Assume that there is no carrier modulation involved. Referring to Fig. 13.2, the following analysis hold good:

Case A: Let T >> To. Consider interval 0 < t <= To/2 . Gate pulse for Q1 and Q4 are HIGH and that for Q2 and Q3 are LOW. Then the following argument is valid:

- Input voltage VA is +Vdc/2 (+50 V) Volts and VB is –Vdc/2 (-50 V) Volts.
- IGBT Q1 is ON and Q2, Q3 and Q4 are OFF.
- IGBT Q1 and the diode across Q2 conducts.
- Output voltage VOUT is +Vdc/2 (+50 V) Volts.

Case B: Let T >> To. Consider interval To/2 < t <= To. Gate pulse for Q2 and Q3 are HIGH and that for Q1 and Q4 are LOW. Then the following argument is valid:

- Input voltage VA is +Vdc/2 (+50 V) Volts and VB is –Vdc/2 (-50 V) Volts.
- IGBT Q3 is ON and Q1, Q2 and Q4 are OFF.
- IGBT Q3 and the diode across Q4 conducts.
- Output voltage VOUT is -Vdc/2 (-50 V) Volts.

Case C: Let T >> To. Consider interval 0 < t <= To/2. Gate pulse for Q1 and Q4 are HIGH and that for Q2 and Q3 are LOW. Then the following argument is valid:

- Input voltage VA is -Vdc/2 (-50 V) Volts and VB is +Vdc/2 (+50 V) Volts.
- IGBT Q4 is ON and Q1, Q2 and Q3 are OFF.
- IGBT Q4 and the diode across Q3 conducts.
- Output voltage VOUT is +Vdc/2 (+50 V) Volts.

Case D: Let T >> To. Consider interval To/2 < t <= To. Gate pulse for Q2 and Q3 are HIGH and that for Q1 and Q4 are LOW. Then the following argument is valid:

- Input voltage VA is -Vdc/2 (-50 V) Volts and VB is +Vdc/2 (+50 V) Volts.
- IGBT Q2 is ON and Q1, Q3 and Q4 are OFF.
- IGBT Q2 and the diode across Q1 conducts.
- Output voltage VOUT is -Vdc/2 (-50 V) Volts.

Period of output voltage VOUT is To. Case A to D are shown in Fig. A13.2.

Case E: Let T << To. Consider interval 0 < t <= To/2 . Gate pulse for Q1 and Q4 are HIGH and that for Q2 and Q3 are LOW. Then the following argument is valid:

- When VA is +Vdc/2 (+50 V) Volts and VB is –Vdc/2 (-50 V) Volts, IGBT Q1 and the diode across Q2 conducts. Output VOUT is +Vdc/2 (+50 V) Volts.

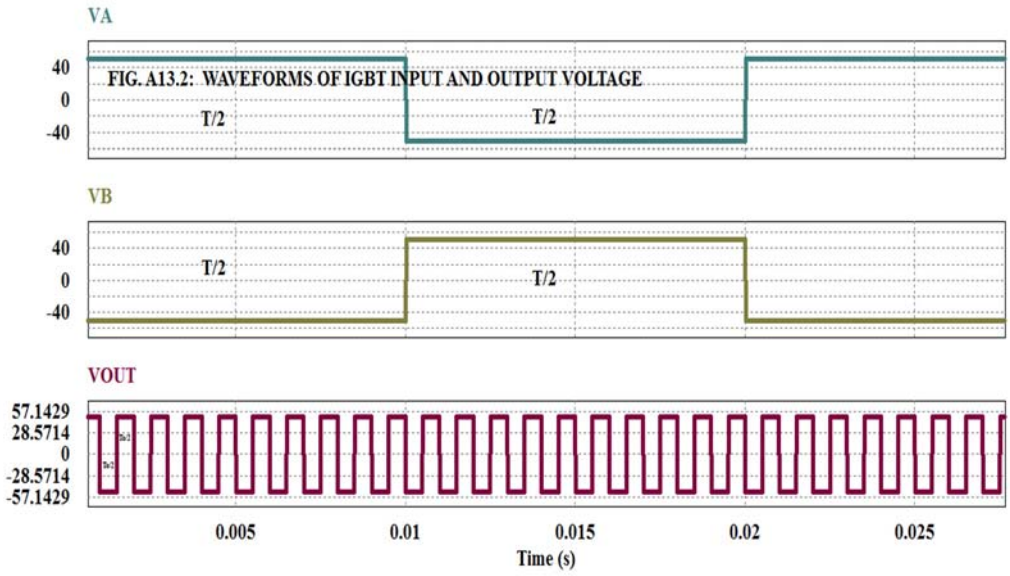


FIG. A13.2: WAVEFORMS OF IGBT INPUT AND OUTPUT VOLTAGE

- When VA is -Vdc/2 (-50 V) Volts and VB is +Vdc/2 (+50 V) Volts, IGBT Q4 and the diode across Q3 conducts. Output VOUT is +Vdc/2 (+50 V) Volts.

Case F: Let T << To. Consider interval To/2 < t <= To. Gate pulse for Q1 and Q4 are LOW and that for Q2 and Q3 are HIGH. Then the following argument is valid:

- When VA is +Vdc/2 (+50 V) Volts and VB is –Vdc/2 (-50 V) Volts, IGBT Q3 and the diode across Q4 conducts. Output VOUT is -Vdc/2 (-50 V) Volts.
- When VA is -Vdc/2 (-50 V) Volts and VB is +Vdc/2 (+50 V) Volts, IGBT Q2 and the diode across Q1 conducts. Output VOUT is -Vdc/2 (-50 V) Volts.

Case G: Let T << To. Consider interval 0 < t <= To/2 . Gate pulse for Q1 and Q4 are LOW and that for Q2 and Q3 are HIGH. Then the following argument is valid:

- When VA is +Vdc/2 (+50 V) Volts and VB is –Vdc/2 (-50 V) Volts, IGBT Q3 and the diode across Q4 conducts. Output VOUT is -Vdc/2 (-50 V) Volts.
- When VA is -Vdc/2 (-50 V) Volts and VB is +Vdc/2 (+50 V) Volts, IGBT Q2 and the diode across Q1 conducts. Output VOUT is -Vdc/2 (-50 V) Volts.

Case H: Let T << To. Consider interval To/2 < t <= To. Gate pulse for Q1 and Q4 are HIGH and that for Q2 and Q3 are LOW. Then the following argument is valid:

- When VA is +Vdc/2 (+50 V) Volts and VB is –Vdc/2 (-50 V) Volts, IGBT Q1 and the diode across Q2 conducts. Output VOUT is +Vdc/2 (+50 V) Volts.
- When VA is -Vdc/2 (-50 V) Volts and VB is +Vdc/2 (+50 V) Volts, IGBT Q4 and the diode across Q3 conducts. Output VOUT is +Vdc/2 (+50 V) Volts.

The period of the output voltage VOUT is To. Case E to H are shown in Fig. A13.3.

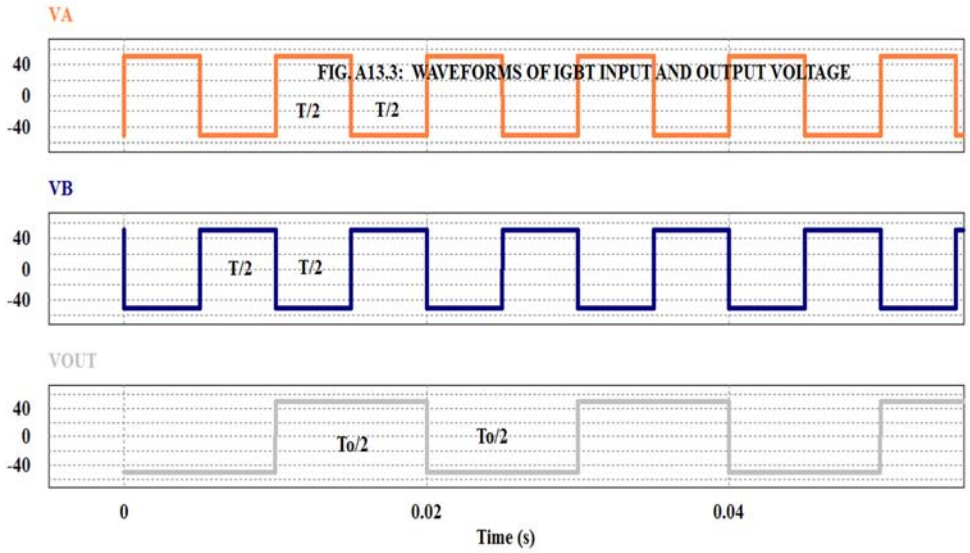


FIG. A13.3: WAVEFORMS OF IGBT INPUT AND OUTPUT VOLTAGE

Also Case A to H described above are diagrammatically shown in Fig. A13.4 (A), (B), (C) and (D).

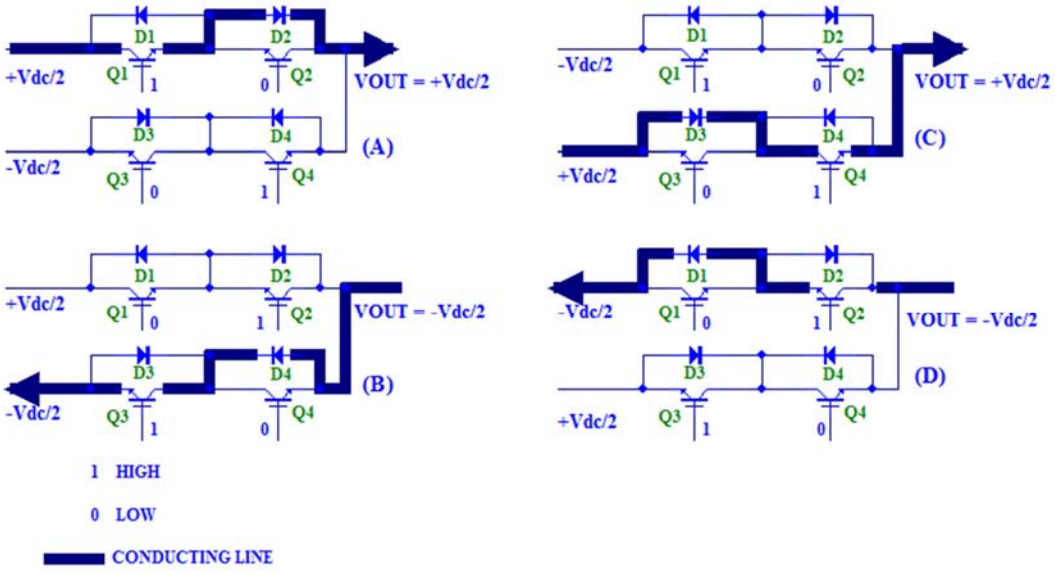


FIG. A13.4: BIDIRECTIONAL IGBT INVERTER CONDUCTING MODES

Fig. A13.4(A), (B), (C) and (D) respectively correspond to cases A, E and H; cases B, F and G; cases C, E and H; and cases D, F and G discussed in Appendix A13.1 above.

The same principle of operation holds good for the three phase AC to three phase AC Converter using a DC link discussed in section 13.7 above.

Chapter XIV

Verification of Models of Three Phase AC To Three Phase AC Matrix Converter

14.1 INTRODUCTION: This chapter provides the verification of models of **selected** three phase AC to three phase AC Matrix Converter (MC) topologies discussed in the previous chapters using either PSIM or PSCAD software [52-53].

14.2 MATRIX CONVERTER MODEL USING VENTURINI MODULATION ALGORITHM: The model of a three phase AC to three phase AC MC using Venturini second method is discussed in Section 3.4.3 of Chapter III. The data given in Table 3.2 of Chapter III is used to solve the above problem using PSCAD [53]. Here equation 3.17 of Chapter III is used to generate the nine modulation functions for the bidirectional switches of the MC. The PSCAD model is shown in Fig. 14.1 and the simulation results are shown in Fig. 14.2. The simulation results are tabulated in Table 14.1.

TABLE 14.1: PH3 MC – PSCAD Simulation Results 1

Sl.No.	Algorithm	THD of Line to Neutral Output Voltage (p.u.)	THD Line to Line Output Voltage (p.u.)	THD of Input Current (p.u.)
1	Venturini Second Method	2.19	1.3896	2.331

14.3 MATRIX CONVERTER MODEL USING SUNTER-CLARE MODULATION ALGORITHM: The Sunter-Clare modulation algorithm is discussed in Section 4.2 of Chapter IV. The data given in Table 3.2 of Chapter III is used to develop the model of the three phase AC to three phase AC MC using Sunter-Clare modulation algorithm in PSCAD. This PSCAD model is shown in Fig. 14.3 and the simulation results are in Fig. 14.4. The simulation results are tabulated in Table 14.2.

TABLE 14.2: PH3 MC – PSCAD Simulation Results 2

Sl.No.	Algorithm	THD of Line to Neutral Output Voltage (p.u.)	THD Line to Line Output Voltage (p.u.)	THD of Input Current (p.u.)
1	Sunter-Clare	2.217	1.101	3.164

14.4 MODEL OF MATRIX CONVERTER USING NED MOHAN MODULATION ALGORITHM: The Ned Mohan modulation algorithm is discussed in Section 4.4 of Chapter IV. The data given in Table 3.2 of Chapter III is used to develop the model of the three phase AC to three phase AC MC using Ned Mohan modulation algorithm in PSCAD. The value of modulation index k is 0.26667. This PSCAD model is shown in Fig. 14.5 and the simulation results are in Fig. 14.6. The simulation results are tabulated in Table 14.3.

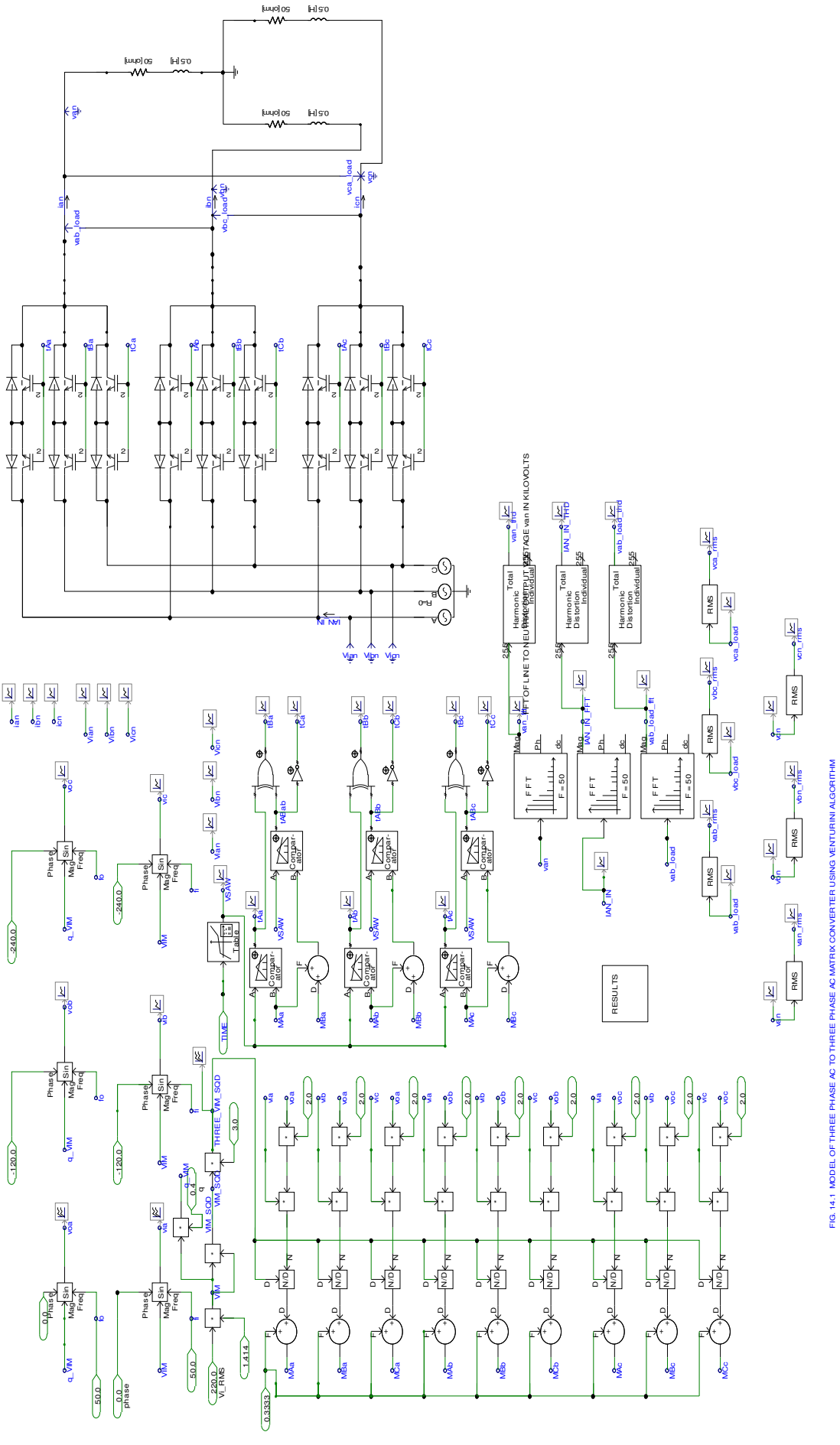


FIG. 14.1 MODEL OF THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER USING VENTURINI ALGORITHM

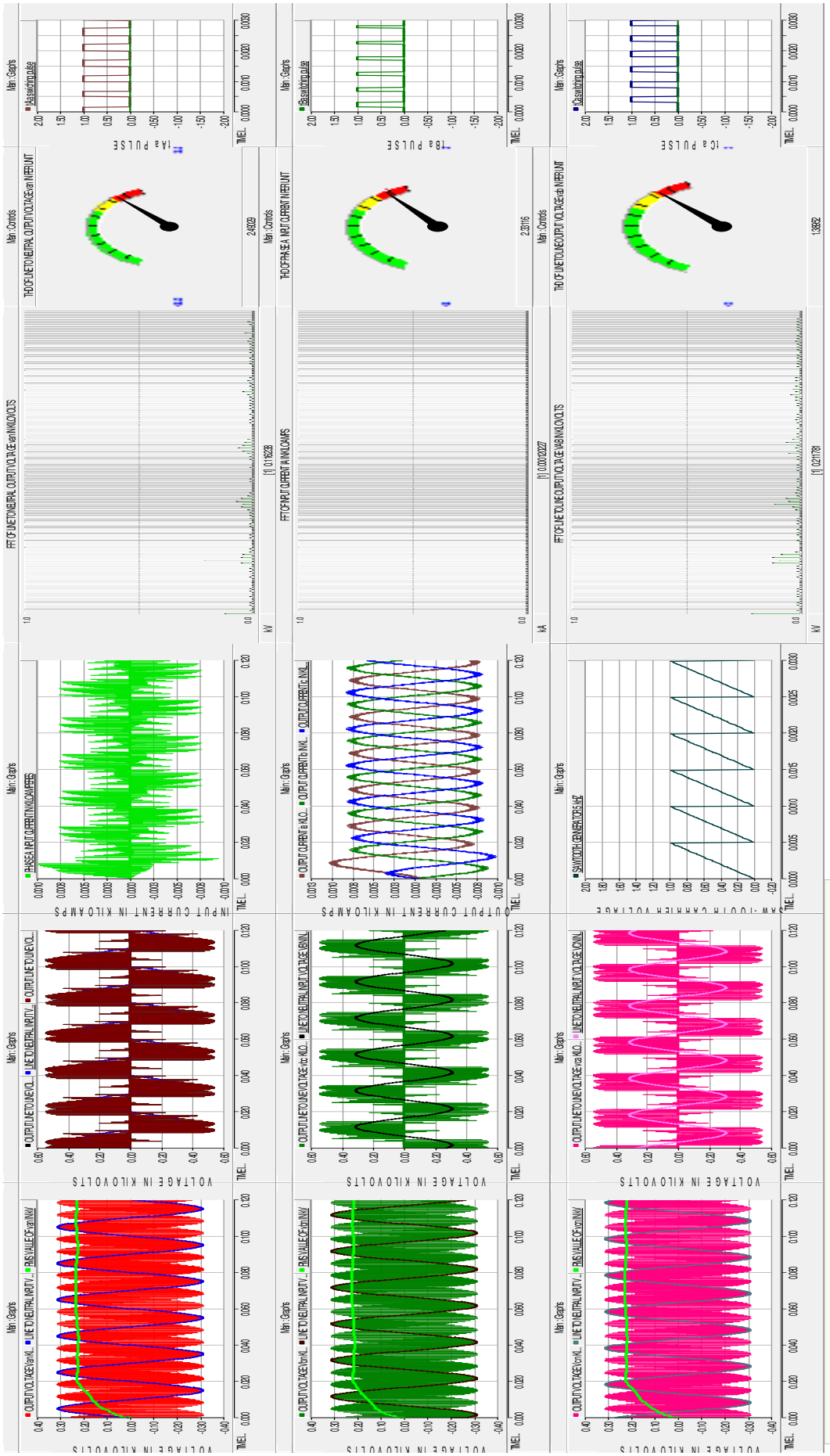


FIG. 14.2 SIMULATION RESULTS FOR THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MC USING VENTURINI ALGORITHM

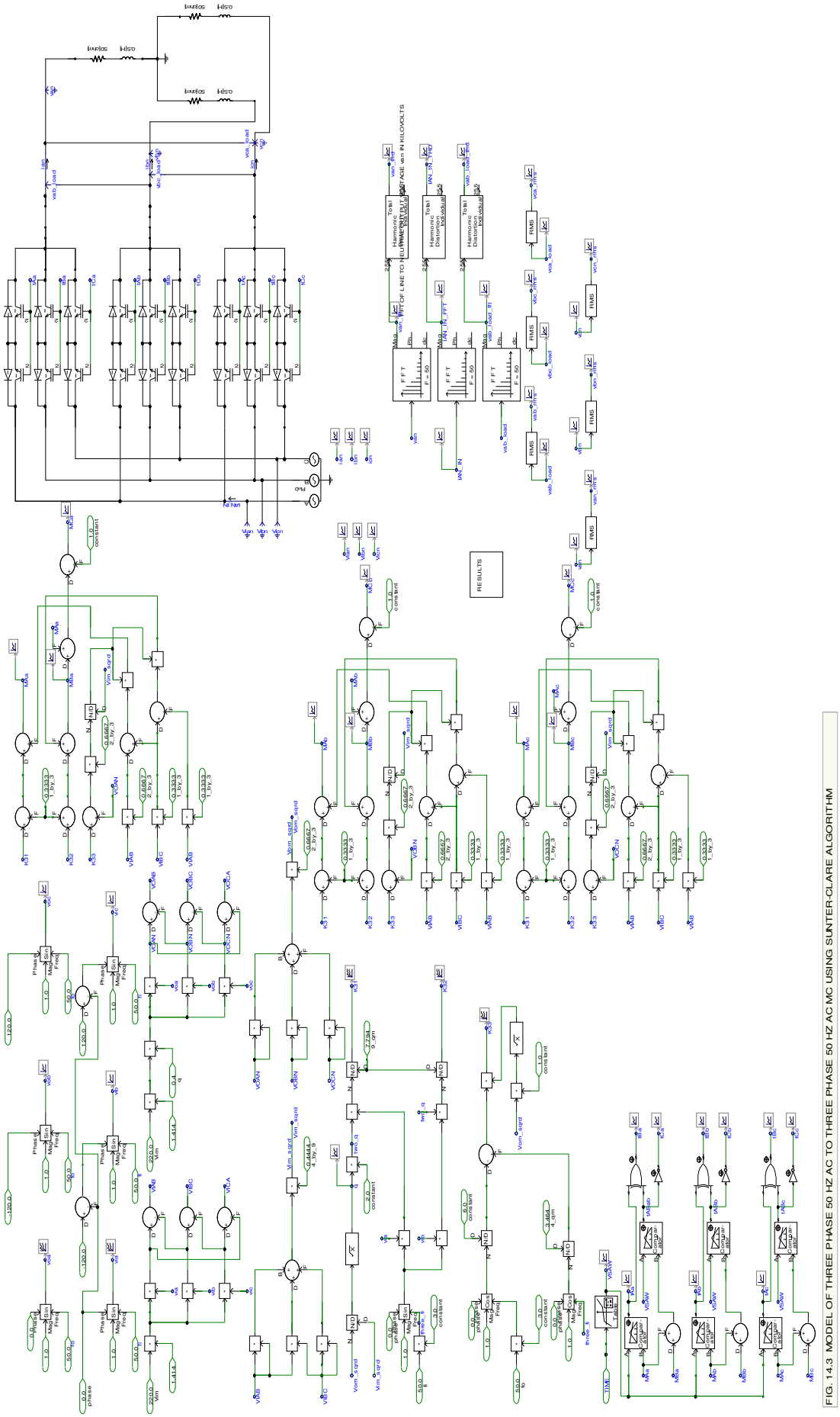


FIG. 14.3 MODEL OF THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MC USING SUNTER-CLARE ALGORITHM

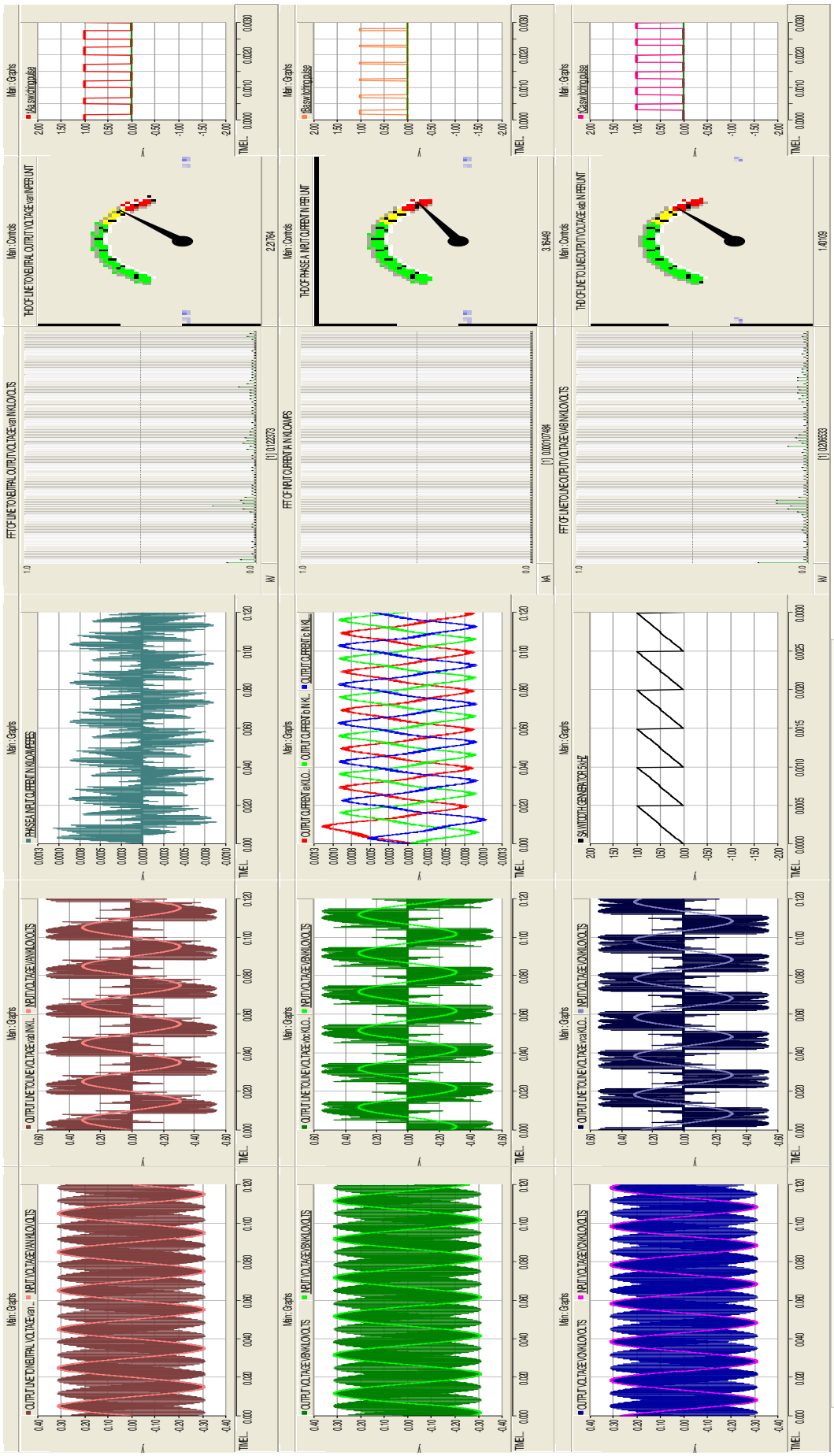


FIG. 14.4 THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MC USING SUNTER-CLARE ALGORITHM - SIMULATION RESULTS

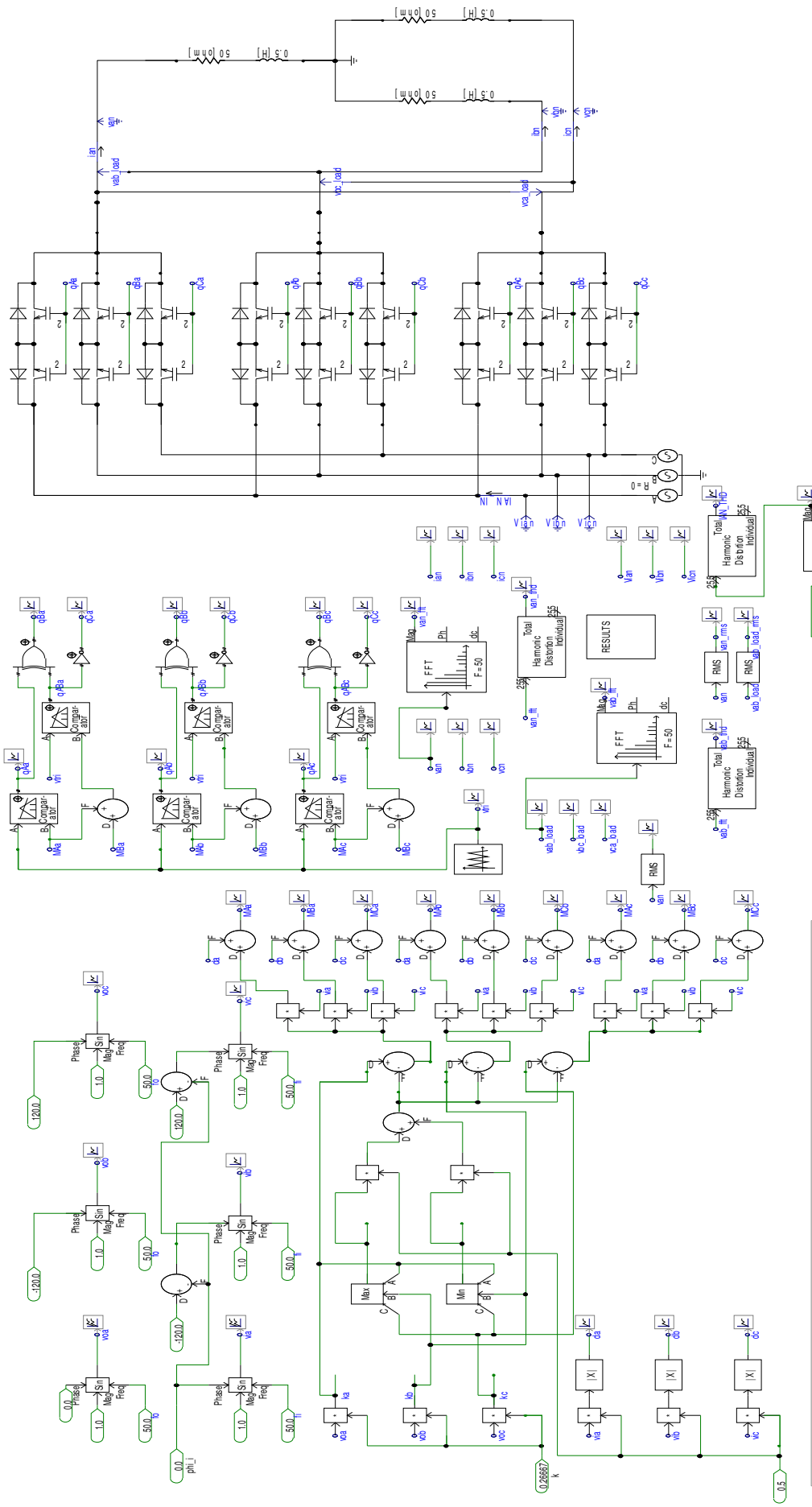


FIG. 14.5 MODEL OF THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MC USING NED MOHAN ALGORITHM

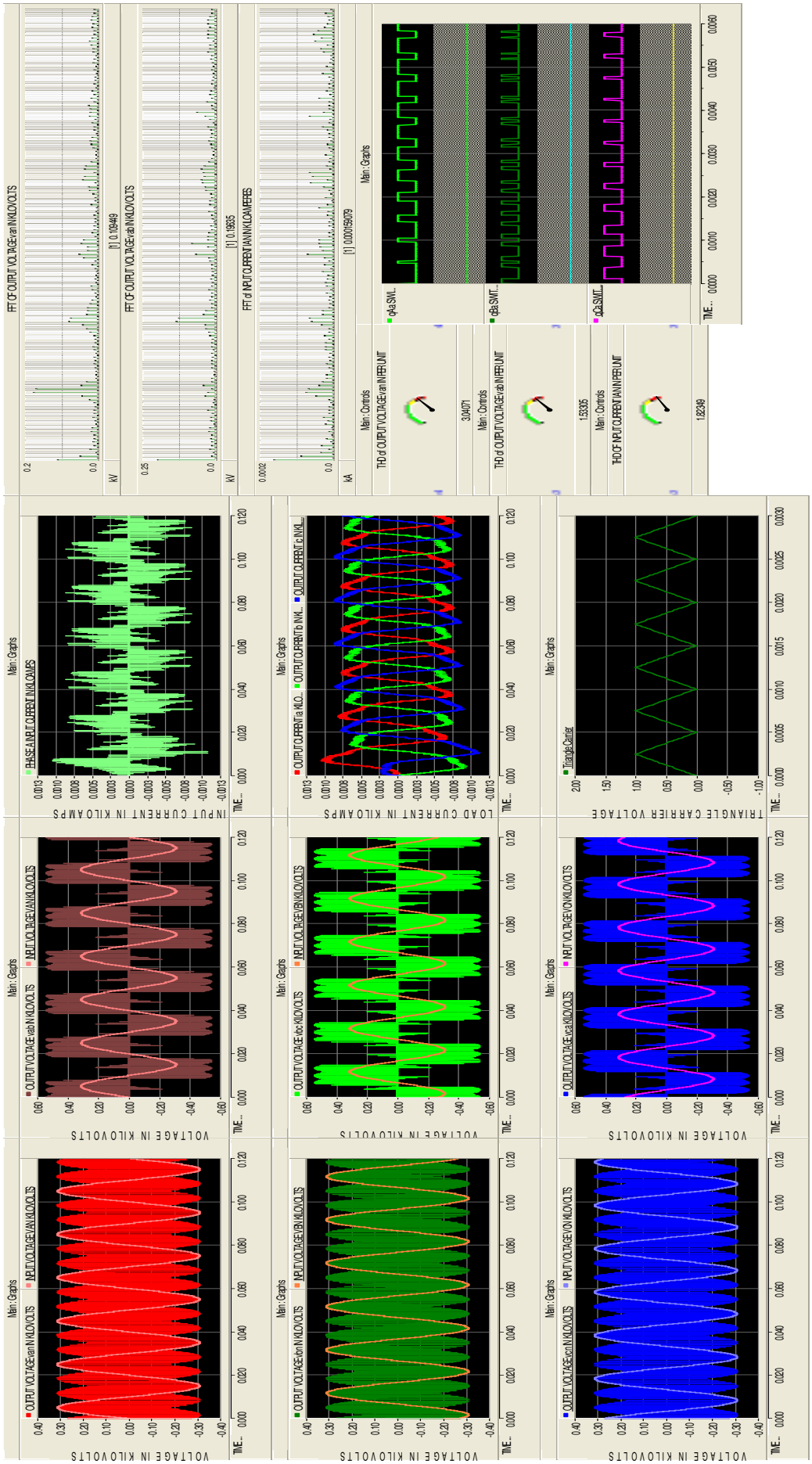


FIG. 14.6 THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MC USING NED MOHAN ALGORITHM - SIMULATION RESULTS

TABLE 14.3: PH3 MC – PSCAD Simulation Results 3

Sl.No.	Algorithm	THD of Line to Neutral Output Voltage (p.u.)	THD Line to Line Output Voltage (p.u.)	THD of Input Current (p.u.)
1	Ned Mohan	3.04	1.533	1.823

14.5 MODEL OF MULTILEVEL MATRIX CONVERTER WITH THREE FLYING CAPACITORS PER OUTPUT PHASE: The development model for the multilevel matrix converter with three flying capacitors per output phase using Venturini modulation algorithm has already been discussed in Section 7.2 of Chapter VII. In this section the model of the three phase MMC with three FC is re-examined using PSIM9 software [52]. The PSIM model of the three phase MMC with three FC is shown in Fig. 14.7. The parameters are given in Table 7.3 of Chapter VII. The simulation results using PSIM9 are shown in Figs. 14.8(A) to 14.8(L). The simulation results are tabulated in Table 14.4.

TABLE 14.4: PH3 MMC with Three FC – PSIM Simulation Result

Sl.No.	Topology	Parameters	Line to Neutral Output Voltage		Line to Line Output Voltage		Phase A Input Current	
			Peak Fundamental (Volts)	T.H.D. (p.u.)	Peak Funda-mental (Volts)	T.H.D. (p.u.)	Peak Funda-mental (Amps)	T.H.D. (p.u.)
1)	Three Phase MMC With THREE FC	Table 7.3 Of Chapter VII	149.14	1.0978	260.57	0.7229	1.9398	1.918

In addition the line to neutral output voltage va of phase a and the Phase A input current iA are theoretically calculated using equations 7.4 and 7.5 of Chapter VII. The relevant logic gates, multiplication and summing blocks to theoretically calculate va and iA are shown in Fig. 14.7. This theoretical value and actual value by simulation are tabulated in Table 14.5.

TABLE 14.5: PH3 MMC with Three FC – PSIM Simulation Result Comparison

Sl.No.	Topology	Parameters	Line to Neutral Output Voltage (Volts)		Phase A Input Current (Amps)	
			Theoretical	Actual	Theoretical	Actual
1)	Three Phase MMC With THREE FC	Table 7.3 Of Chapter VII	148.95	156.337	3.237	2.9606

14.6 MODEL OF MULTILEVEL MATRIX CONVERTER WITH SIX FLYING CAPACITORS PER OUTPUT PHASE: Three phase AC to three phase AC MMC with six FC per output phase using Venturini algorithm is already discussed in Section 7.9 of Chapter VII. In this section the model of the three phase MMC with six FC per output phase is re-examined using PSIM9 software [52]. The PSIM model of the three phase MMC with six FC is shown in Fig. 14.9. The parameters are given in Table 7.3 of Chapter VII. The simulation results using PSIM9 are shown in Figs. 14.10(A) to 14.10(J). The simulation results are tabulated in Table 14.6.

TABLE 14.6: PH3 MMC with Six FC – PSIM Simulation Results

Sl.No.	Topology	Parameters	Line to Neutral Output Voltage		Line to Line Output Voltage		Phase A Input Current	
			Peak Funda-mental (Volts)	T.H.D. (p.u.)	Peak Funda-mental (Volts)	T.H.D. (p.u.)	Peak Funda-mental (Amps)	T.H.D. (p.u.)
1)	Three Phase MMC With SIX FC	Table 7.3	161.95	0.816	257.95	0.6346	1.652	1.508

14.7 MODEL OF DUAL PROGRAMMABLE AC TO DC RECTIFIER: The principle of operation relating to the discovery of the dual programmable AC to DC rectifier and its modelling is discussed in Section 10.3 and 10.4 of Chapter X. In this chapter this model performance is re-examined using PSCAD [53]. The model of the dual programmable AC to DC rectifier is shown in Fig. 14.11. The simulation results for the above rectifier for various output voltage phase angle φ_O is shown in Fig. 14.12(A) to (N). The PSCAD simulation results are tabulated in Table 14.7.

TABLE 14.7: Dual Programmable AC to DC Rectifier - PSCAD Simulation Results

Sl.No.	φo radians	Vo1 Volts	Vo2 Volts	Sl.No.	φo radians	Vo1 Volts	Vo2 Volts
1	0	67.5	135	8	±π	-67.5	-135
2	+π/6	116.5	116.5	9	-5π/6	-116.5	-116.5
3	+π/3	135	67.5	10	-2π/3	-135	-67.5
4	+π/2	116.5	0	11	-π/2	-116.5	0
5	+2π/3	67.5	-67.5	12	-π/3	-67.5	67.5
6	+3 π/4	35	-95	13	- π/4	-35	95
7	+5π/6	0	-116.5	14	-π/6	0	116.5

14.8 DELTA-SIGMA MODULATED MATRIX CONVERTER USING VENTURINI ALGORITHM: The model of three phase AC to three phase AC MC delta-sigma modulated using Venturini algorithm is already explained in Section 11.3 and 11.4 of Chapter XI. Here the model of the above MC is developed in PSIM9[52]. This PSIM model of the above MC is shown in Fig. 14.13. The simulation parameters are shown in Table 11.2 of Chapter XI. The simulation results using PSIM are shown in Fig. 14.14(A) to 14.14(L) and in Fig. 14.15(A) to 14.15(L). The simulation results are also tabulated in Table 14.8.

TABLE 14.8: Delta-Sigma Modulated PH3 MC – PSIM Simulation Reults 1

Sl.No.	Frequency Input-Output Hz	Line to Neutral Output voltage THD (p.u.)	Line to Line Output Voltage THD (p.u.)	Input current THD (p.u.)	Load current THD (p.u.)
1)	50 – 50	1.632	1.5129	6.522	0.392
2)	50 – 10	1.650	1.5123	6.959	2.788

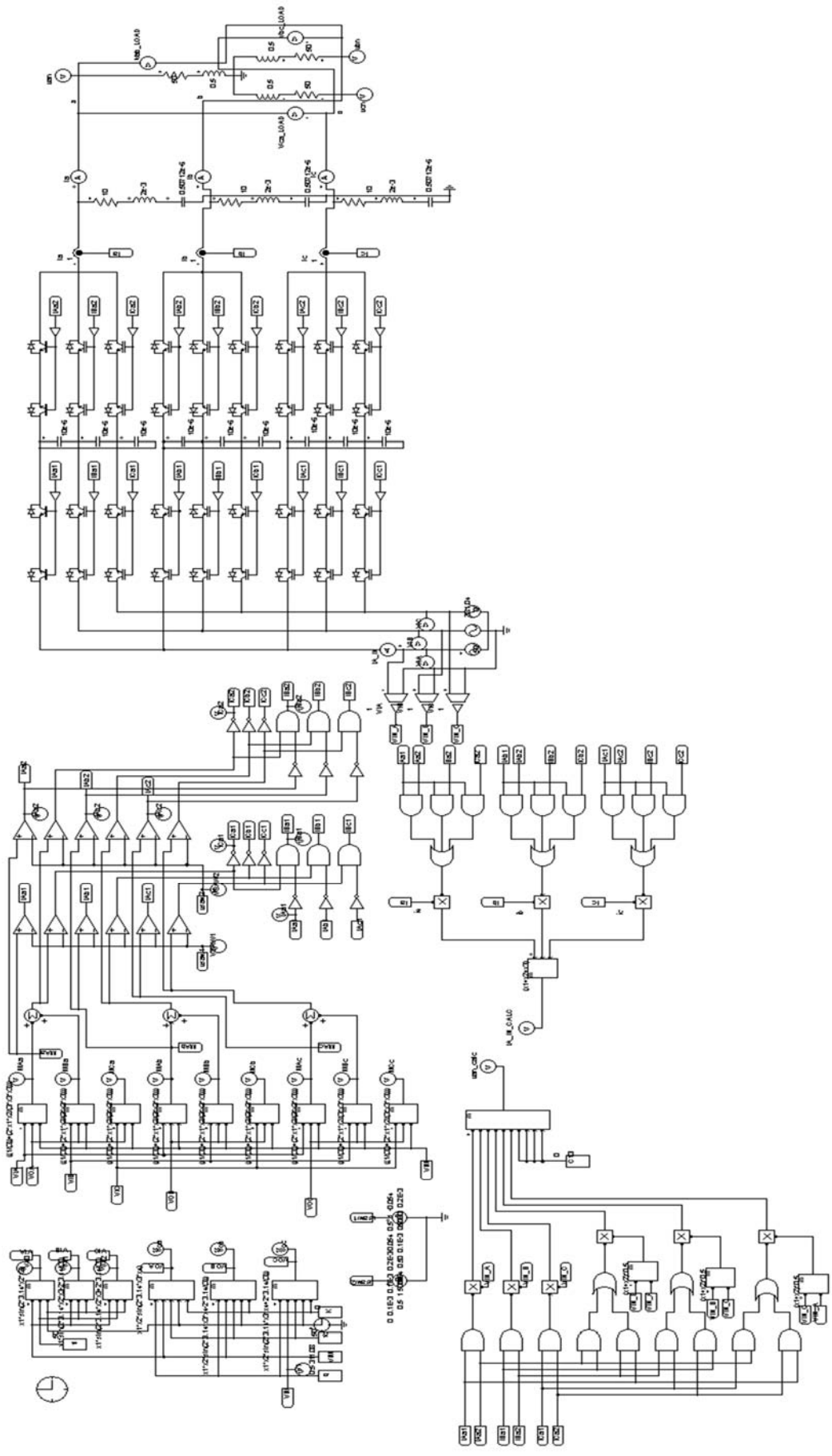
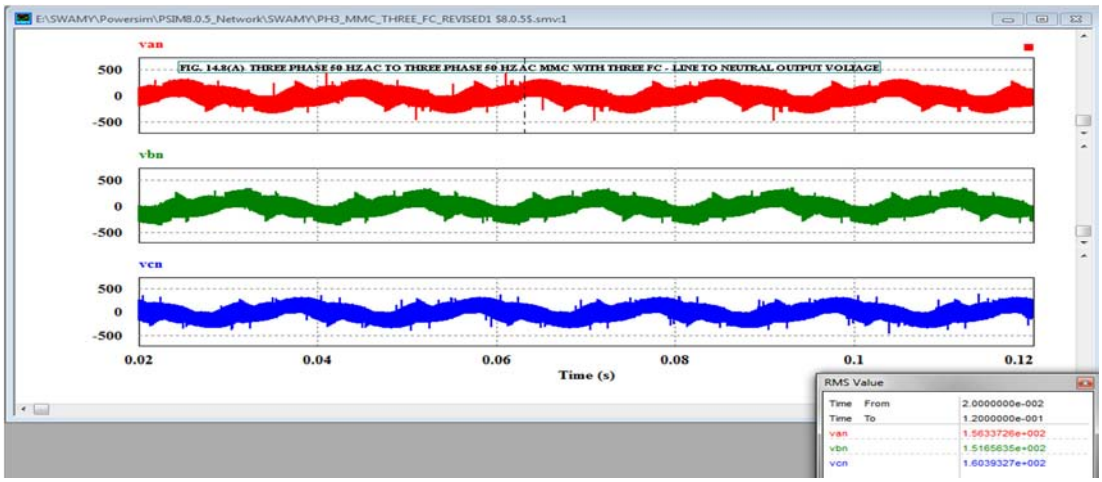
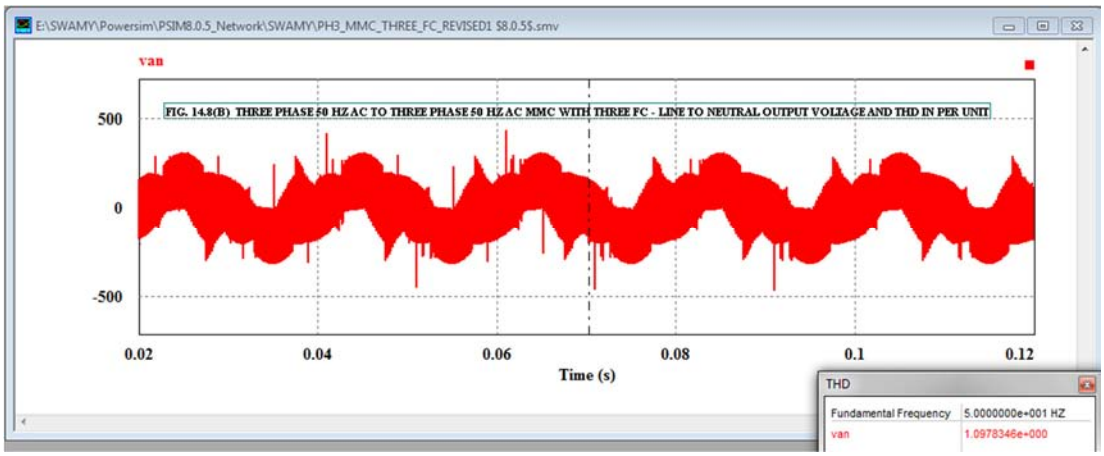
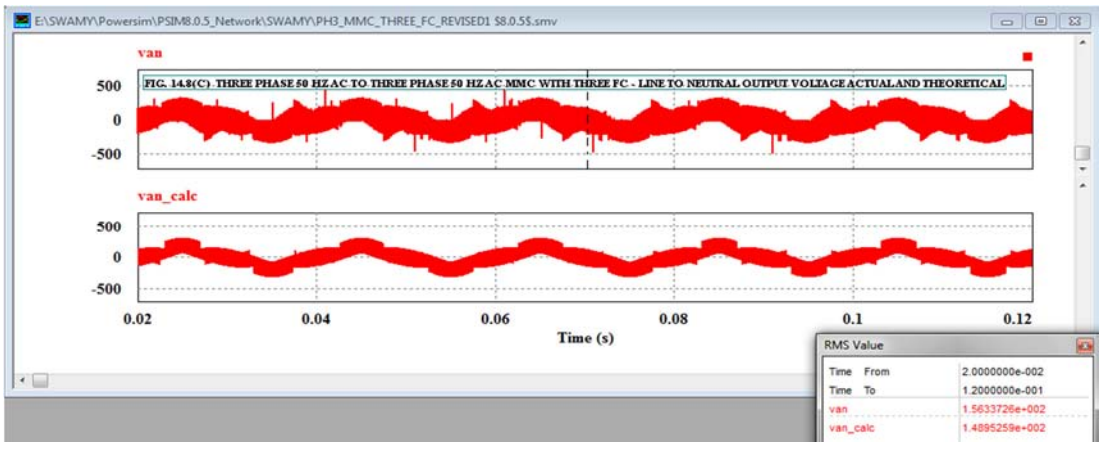
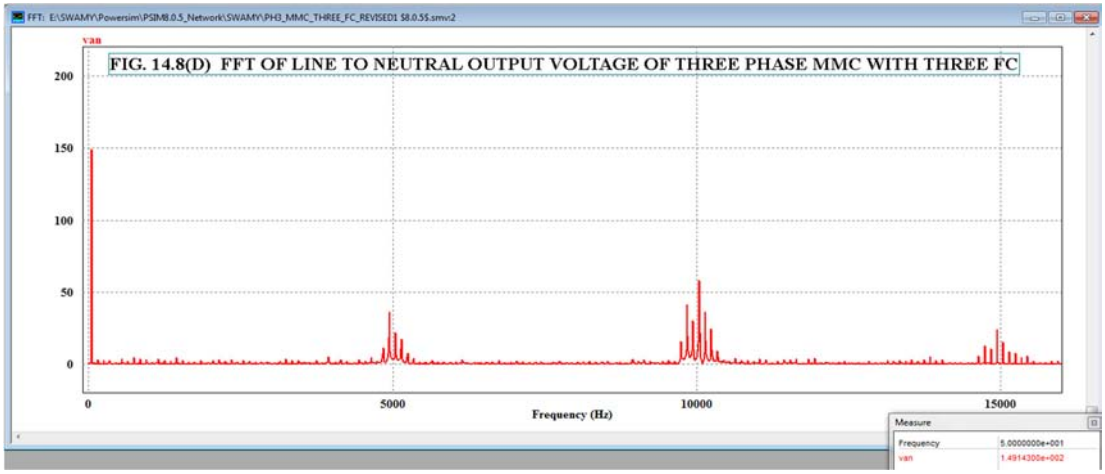


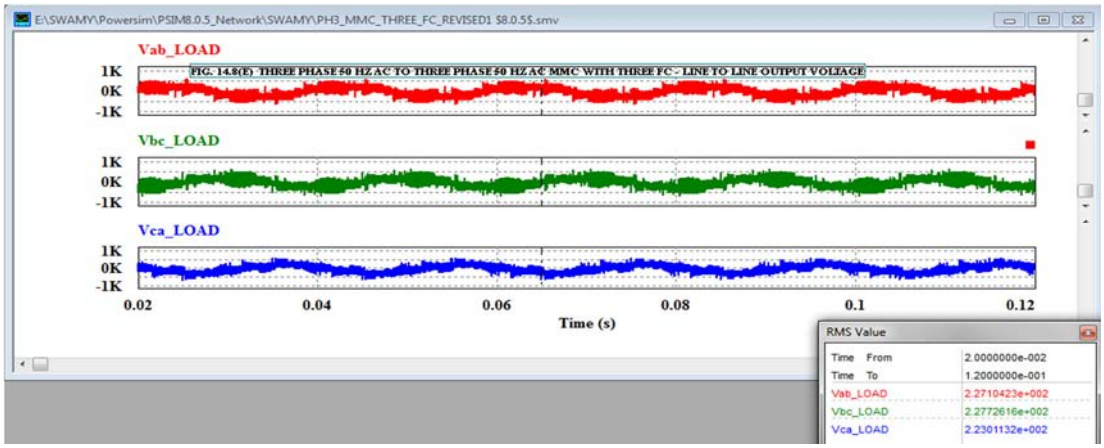
FIG. 14.7 MODEL OF THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH THREE FC

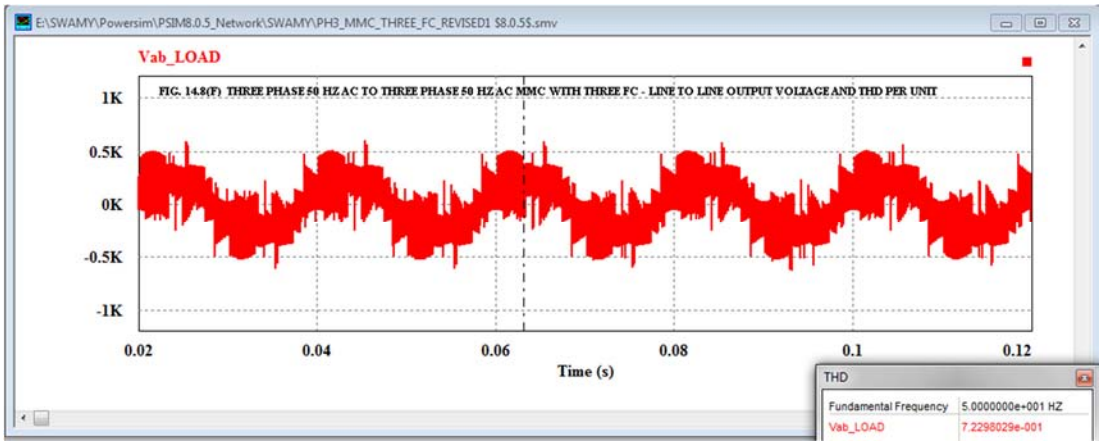

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_THREE_FC_REVISED1 $8.0.5$.smv:1
van
FIG. 14.8(A) THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH THREE FC - LINE TO NEUTRAL OUTPUT VOLTAGE
vbn
vcn
500
0
-500
0.02
0.04
0.06
0.08
0.1
0.12
Time (s)
RMS Value
Time From 2.0000000e-002
Time To 1.2000000e-001
van 1.5633726e+002
vbn 1.5165635e+002
vcn 1.6039327e+002

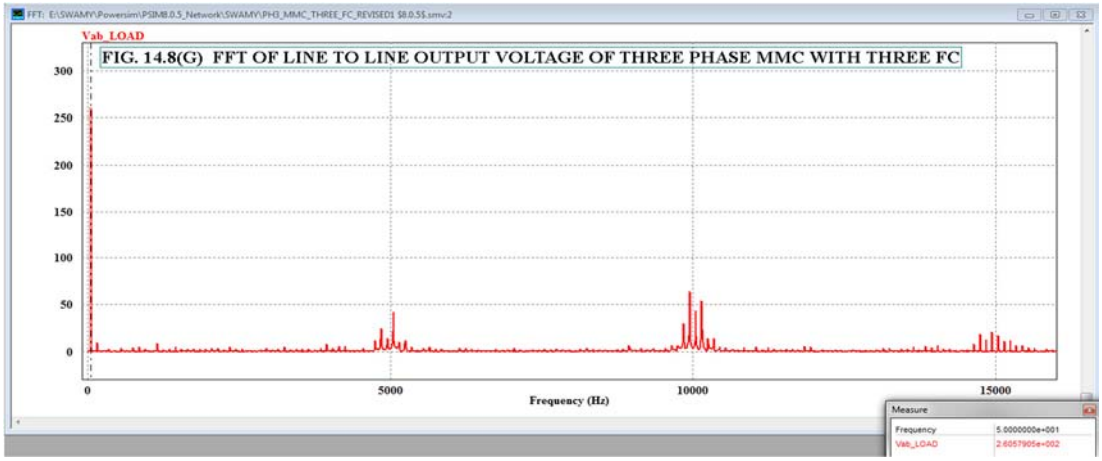

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_THREE_FC_REVISED1 $8.0.5$.smv
van
FIG. 14.8(B) THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH THREE FC - LINE TO NEUTRAL OUTPUT VOLTAGE AND THD IN PER UNIT
500
0
-500
0.02
0.04
0.06
0.08
0.1
0.12
Time (s)
THD
Fundamental Frequency 5.0000000e+001 HZ
van 1.0978346e+000

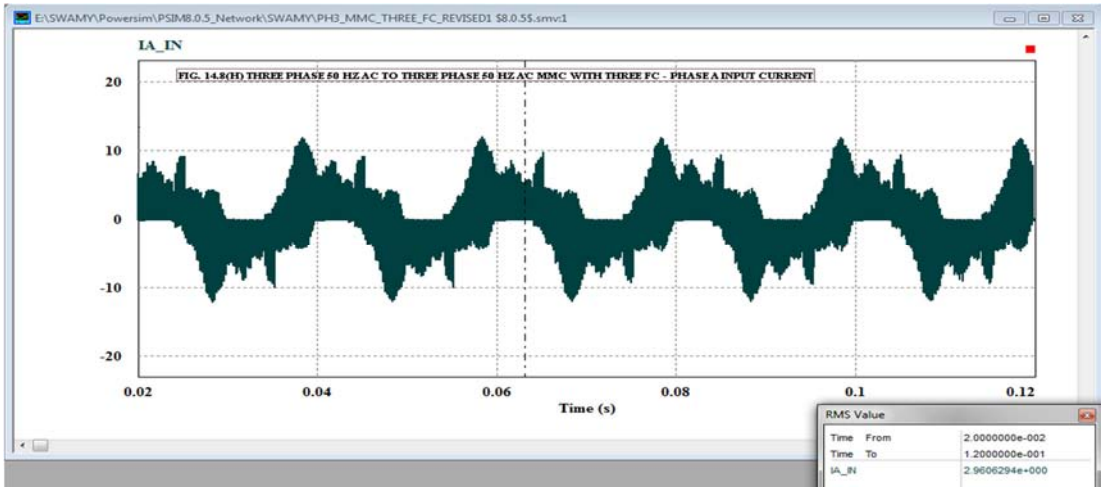

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_THREE_FC_REVISED1 $8.0.5$.smv
van
FIG. 14.8(C) THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH THREE FC - LINE TO NEUTRAL OUTPUT VOLTAGE ACTUAL AND THEORETICAL
van_calc
500
0
-500
0.02
0.04
0.06
0.08
0.1
0.12
Time (s)
RMS Value
Time From 2.0000000e-002
Time To 1.2000000e-001
van 1.5633726e+002
van_calc 1.4895259e+002

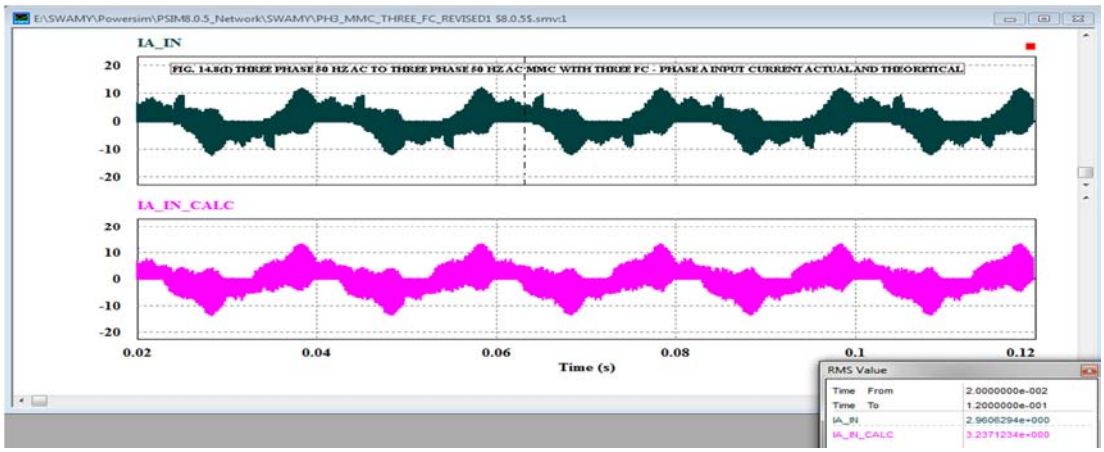

FFT: E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_THREE_FC_REVISED1 $8.0.5$.smv:2
van
FIG. 14.8(D) FFT OF LINE TO NEUTRAL OUTPUT VOLTAGE OF THREE PHASE MMC WITH THREE FC
200
150
100
50
0
0
5000
10000
15000
Frequency (Hz)
Measure
Frequency 5.0000000e+001
van 1.4914300e+002


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_THREE_FC_REVISED1 $8.0.5$.smv
Vab_LOAD
FIG. 14.8(E) THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH THREE FC - LINE TO LINE OUTPUT VOLTAGE
Vbc_LOAD
Vca_LOAD
1K
0K
-1K
0.02
0.04
0.06
0.08
0.1
0.12
Time (s)
RMS Value
Time From 2.0000000e-002
Time To 1.2000000e-001
Vab_LOAD 2.2710423e+002
Vbc_LOAD 2.2772616e+002
Vca_LOAD 2.2301132e+002


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_THREE_FC_REVISED1 $8.0.5$.smv
Vab_LOAD
FIG. 14.8(F) THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH THREE FC - LINE TO LINE OUTPUT VOLTAGE AND THD PER UNIT
1K
0.5K
0K
-0.5K
-1K
0.02
0.04
0.06
0.08
0.1
0.12
Time (s)
THD
Fundamental Frequency 5.0000000e+001 HZ
Vab_LOAD 7.2298029e-001


Vab_LOAD
FIG. 14.8(G) FFT OF LINE TO LINE OUTPUT VOLTAGE OF THREE PHASE MMC WITH THREE FC
300
250
200
150
100
50
0
0
5000
10000
15000
Frequency (Hz)
Measure
Frequency 5.0000000e+001
Vab_LOAD 2.6057905e+002


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_THREE_FC_REVISED1 $8.0.5$.smv:1
IA_IN
FIG. 14.8(H) THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH THREE FC - PHASE A INPUT CURRENT
20
10
0
-10
-20
0.02
0.04
0.06
0.08
0.1
0.12
Time (s)
RMS Value
Time From 2.0000000e-002
Time To 1.2000000e-001
IA_IN 2.9606294e+000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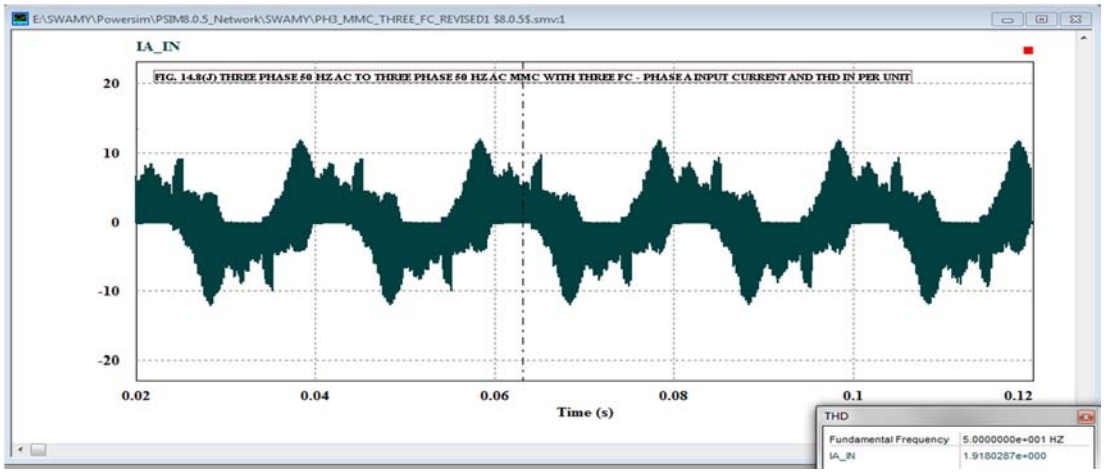
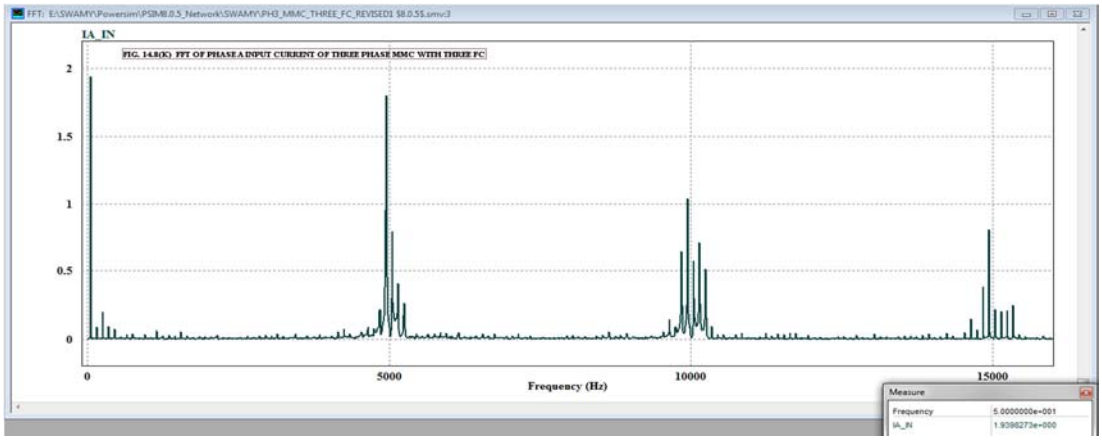
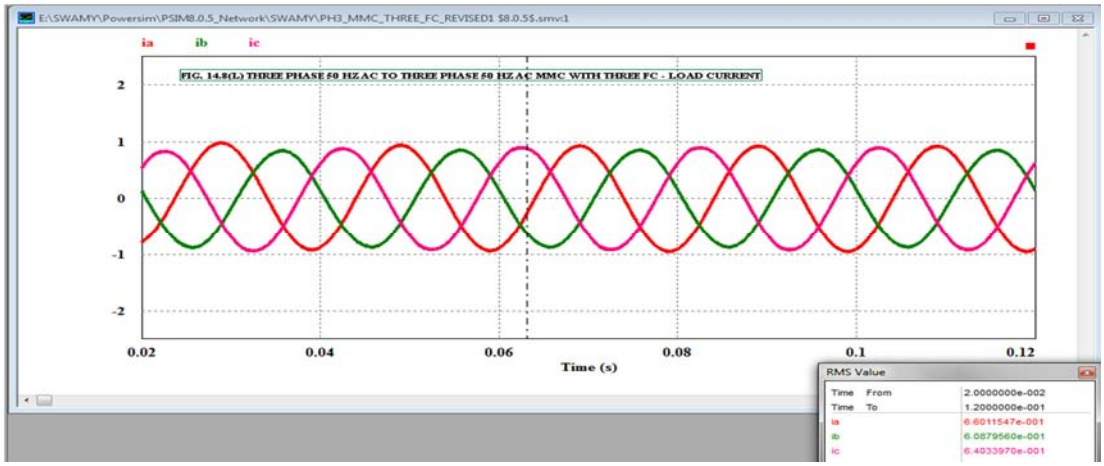
IA_IN
FIG. 14.8(I) THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH THREE FC - PHASE A INPUT CURRENT ACTUAL AND THEORETICAL
IA_IN_CALC
Time (s)
RMS Value
Time From 2.0000000e-002
Time To 1.2000000e-001
IA_IN 2.9606294e+000
IA_IN_CALC 3.2371234e+000


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_THREE_FC_REVISED1 $8.0.5$.smv:1
IA_IN
FIG. 14.8(J) THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH THREE FC - PHASE A INPUT CURRENT AND THD IN PER UNIT
Time (s)
THD
Fundamental Frequency 5.0000000e+001 HZ
IA_IN 1.9180287e+000


IA_IN
FIG. 14.8(K) FFT OF PHASE A INPUT CURRENT OF THREE PHASE MMC WITH THREE FC
Frequency (Hz)
Measure
Frequency 5.0000000e+001
IA_IN 1.9398273e+000


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_THREE_FC_REVISED1 $8.0.5$.smv:1
ia ib ic
FIG. 14.8(L) THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH THREE FC - LOAD CURRENT
Time (s)
RMS Value
Time From 2.0000000e-002
Time To 1.2000000e-001
ia 6.6011547e-001
ib 6.0879560e-001
ic 6.4033970e-001

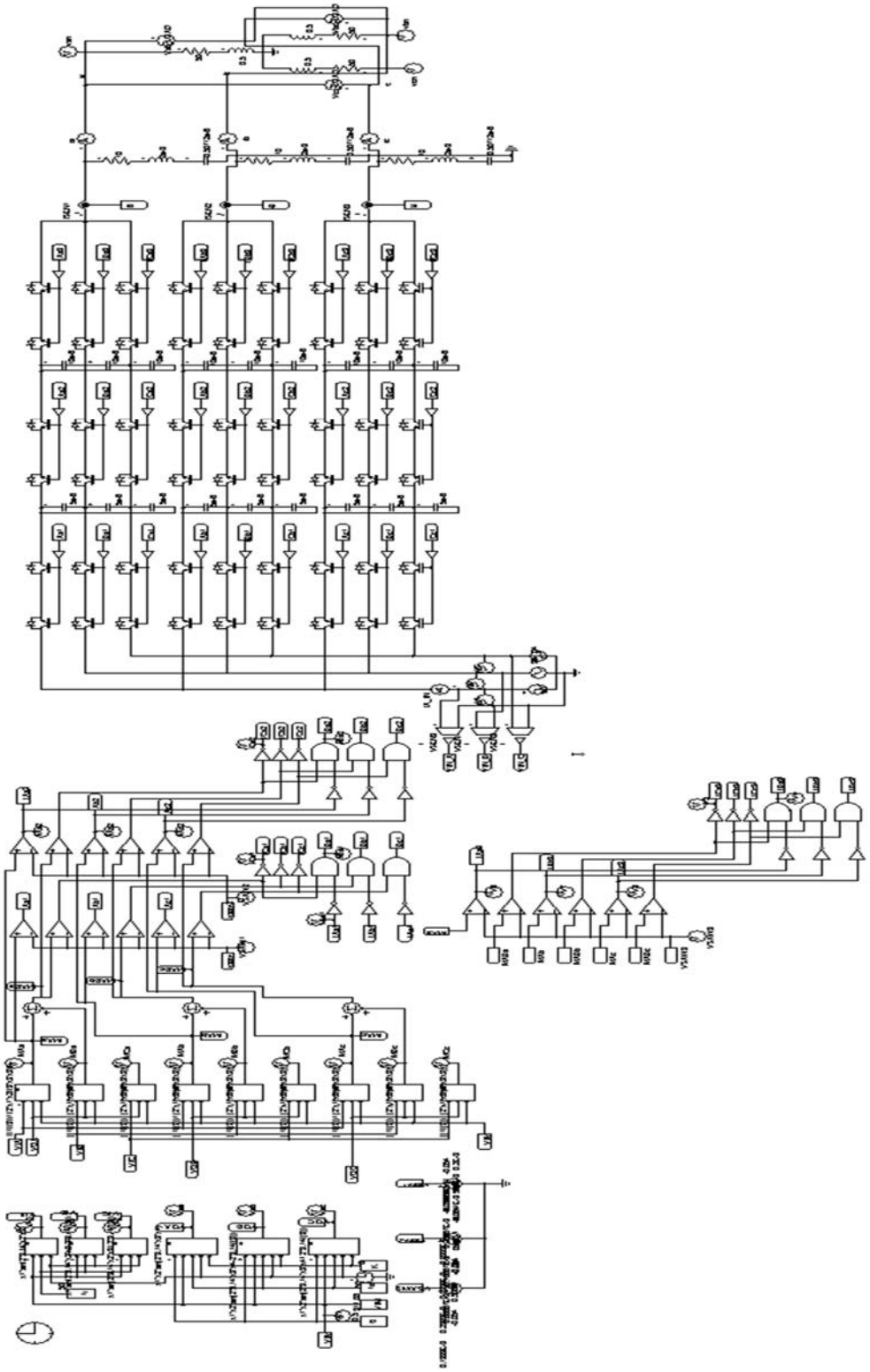
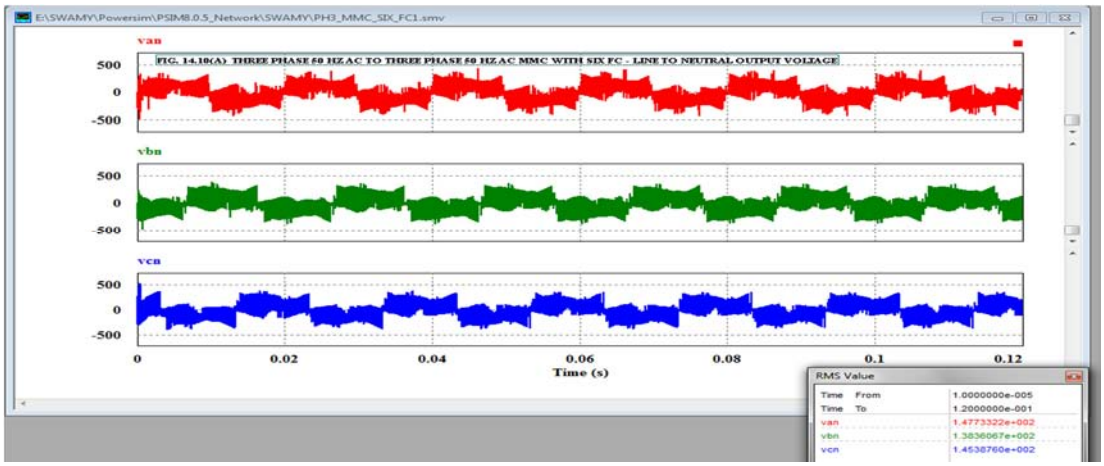
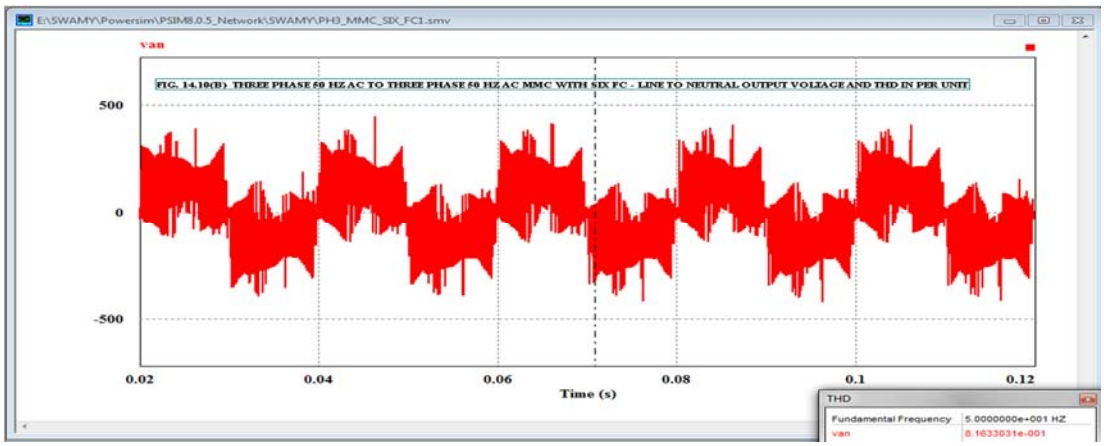
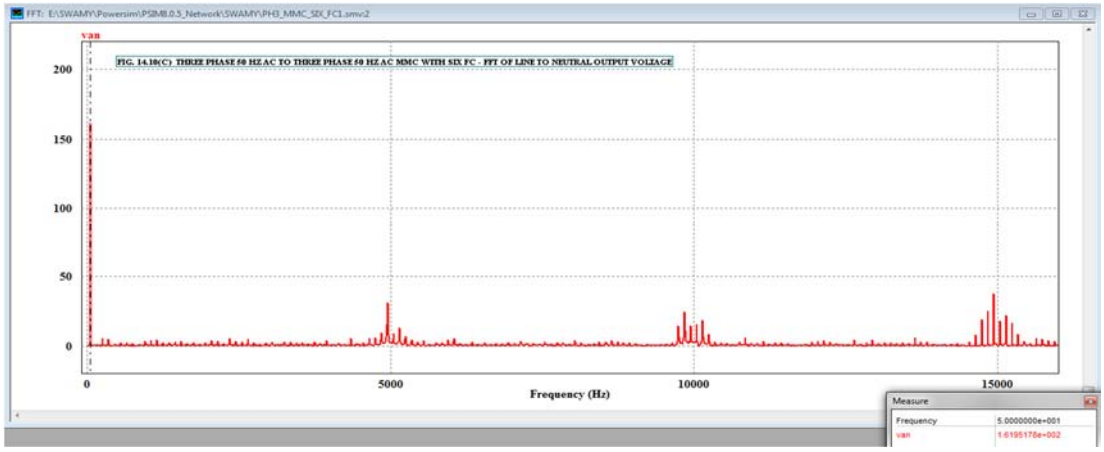
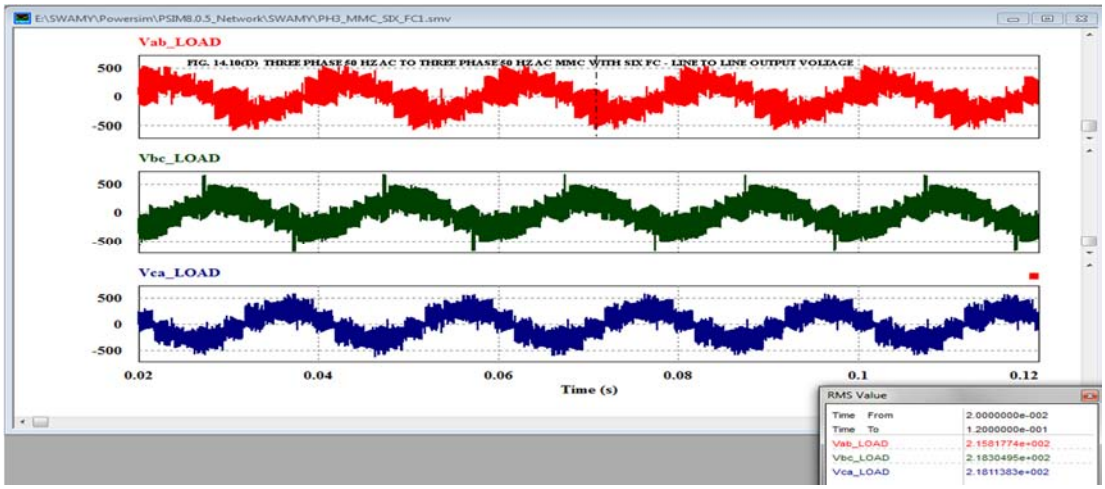


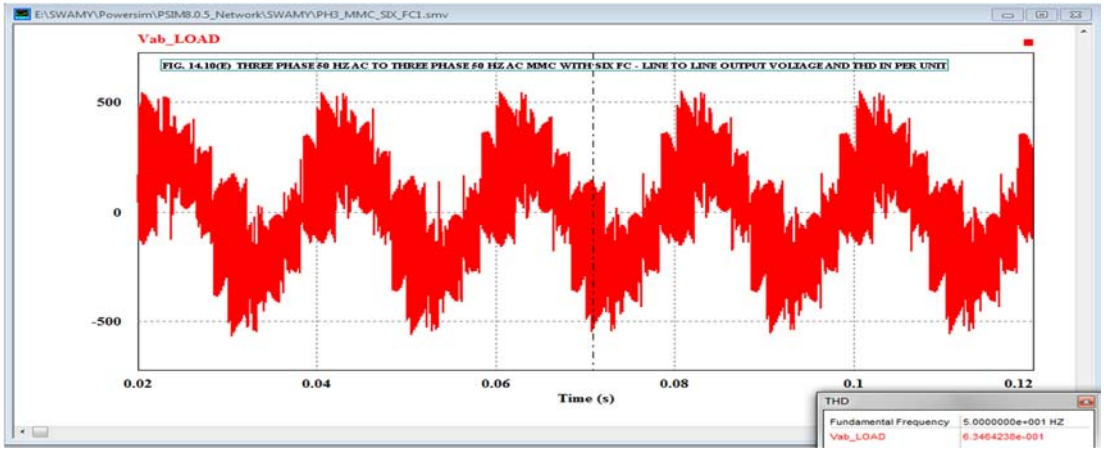
FIG. 14.9 MODEL OF THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH SIX FC

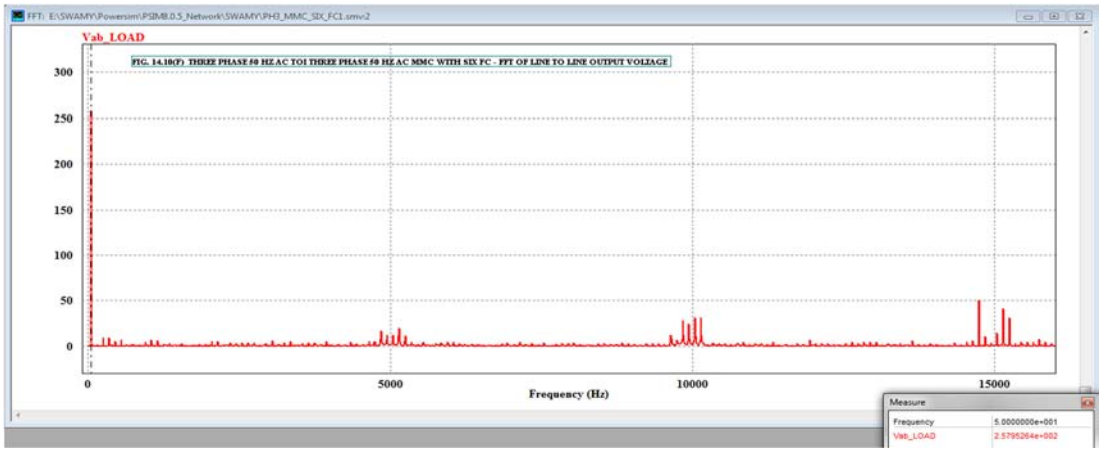

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_SIX_FC1.smv
van
FIG. 14.10(A) THREE PHASE 60 HZ AC TO THREE PHASE 60 HZ AC MMC WITH SIX FC - LINE TO NEUTRAL OUTPUT VOLTAGE
vbn
vcn
500
0
-500
0
0.02
0.04
0.06
0.08
0.1
0.12
Time (s)
RMS Value
Time From 1.0000000e-005
Time To 1.2000000e-001
van 1.4773322e+002
vbn 1.3836067e+002
vcn 1.4538760e+002

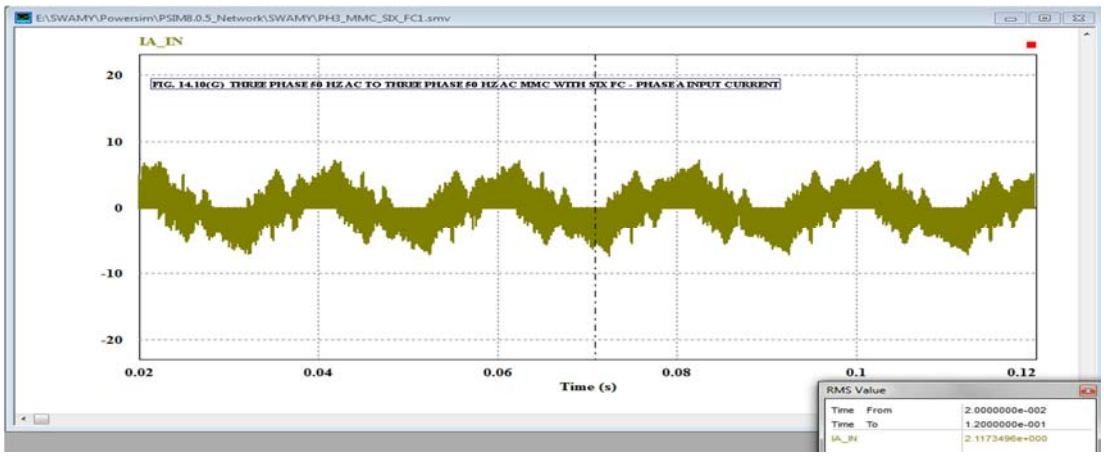

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_SIX_FC1.smv
van
FIG. 14.10(B) THREE PHASE 60 HZ AC TO THREE PHASE 60 HZ AC MMC WITH SIX FC - LINE TO NEUTRAL OUTPUT VOLTAGE AND THD IN PER UNIT
500
0
-500
0.02
0.04
0.06
0.08
0.1
0.12
Time (s)
THD
Fundamental Frequency 5.0000000e+001 HZ
van 8.1633031e-001

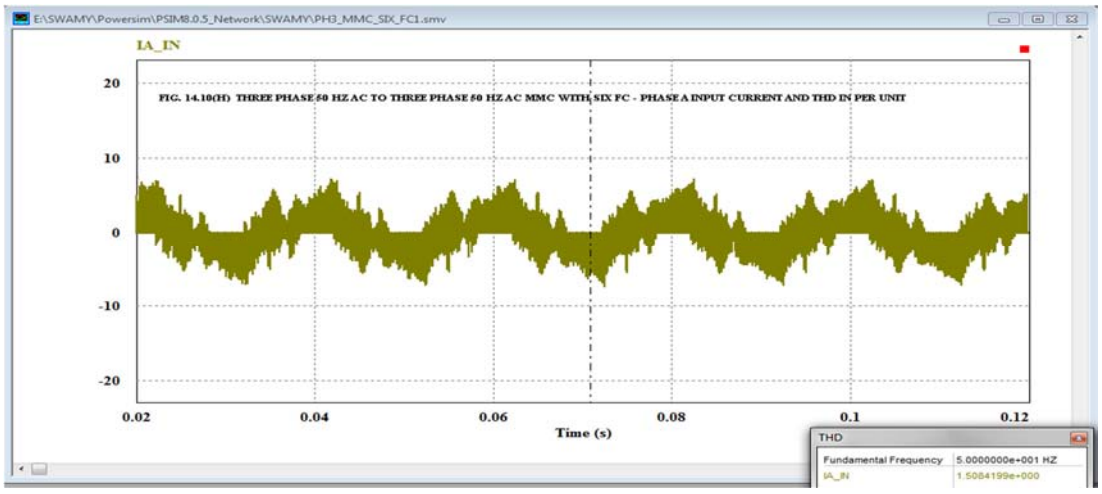

FFT: E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_SIX_FC1.smv2
van
FIG. 14.10(C) THREE PHASE 60 HZ AC TO THREE PHASE 60 HZ AC MMC WITH SIX FC - FFT OF LINE TO NEUTRAL OUTPUT VOLTAGE
200
150
100
50
0
0
5000
10000
15000
Frequency (Hz)
Measure
Frequency 5.0000000e+001
van 1.6195178e-002

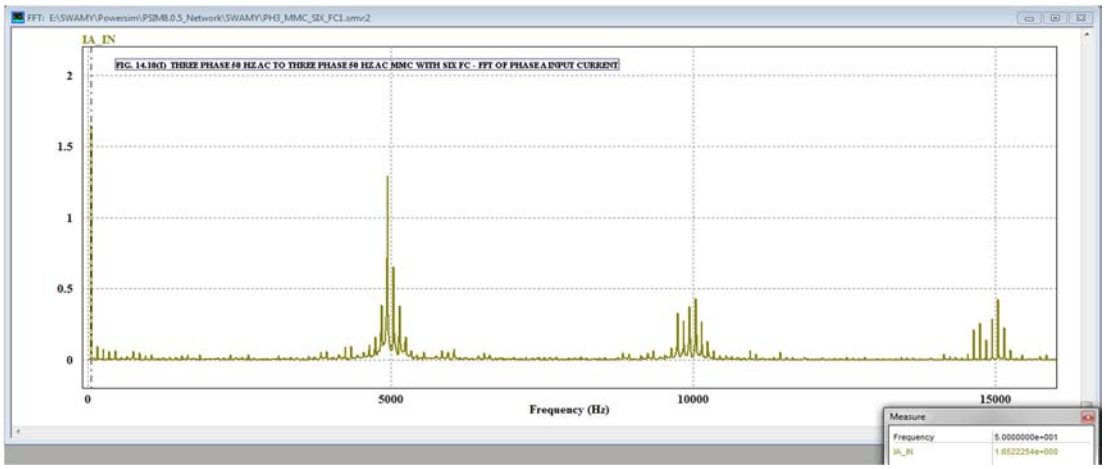

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_SIX_FC1.smv
Vab_LOAD
FIG. 14.10(D) THREE PHASE 60 HZ AC TO THREE PHASE 60 HZ AC MMC WITH SIX FC - LINE TO LINE OUTPUT VOLTAGE
Vbc_LOAD
Vca_LOAD
500
0
-500
0.02
0.04
0.06
0.08
0.1
0.12
Time (s)
RMS Value
Time From 2.0000000e-002
Time To 1.2000000e-001
Vab_LOAD 2.1581774e+002
Vbc_LOAD 2.1830495e+002
Vca_LOAD 2.1811383e+002

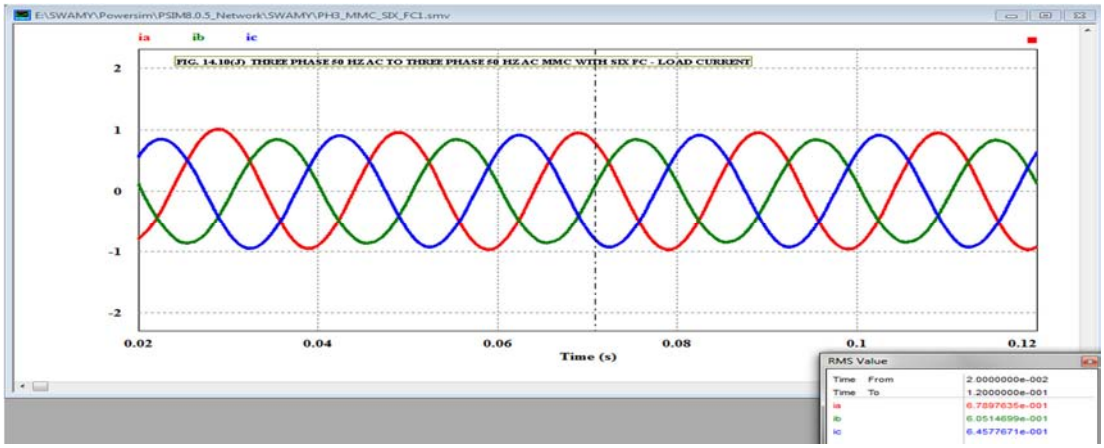

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_SIX_FC1.smv
Vab_LOAD
FIG. 14.10(E) THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH SIX FC - LINE TO LINE OUTPUT VOLTAGE AND THD IN PER UNIT
500
0
-500
0.02
0.04
0.06
0.08
0.1
0.12
Time (s)
THD
Fundamental Frequency
5.0000000e+001 HZ
Vab_LOAD
6.3464238e-001


FFT: E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_SIX_FC1.smv2
Vab_LOAD
FIG. 14.10(F) THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH SIX FC - FFT OF LINE TO LINE OUTPUT VOLTAGE
300
250
200
150
100
50
0
0
5000
10000
15000
Frequency (Hz)
Measure
Frequency
5.0000000e+001
Vab_LOAD
2.5795264e+002


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_SIX_FC1.smv
IA_IN
FIG. 14.10(G) THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH SIX FC - PHASE A INPUT CURRENT
20
10
0
-10
-20
0.02
0.04
0.06
0.08
0.1
0.12
Time (s)
RMS Value
Time From
2.0000000e-002
Time To
1.2000000e-001
IA_IN
2.1173496e+000


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MMC_SIX_FC1.smv
IA_IN
FIG. 14.10(H) THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MMC WITH SIX FC - PHASE A INPUT CURRENT AND THD IN PER UNIT
20
10
0
-10
-20
0.02
0.04
0.06
0.08
0.1
0.12
Time (s)
THD
Fundamental Frequency
5.0000000e+001 HZ
IA_IN
1.5084199e+000





14.9 DELTA-SIGMA MODULATED MATRIX CONVERTER USING ADVANCED MODULATION ALGORITHM: A novel carrier-based modulation scheme is proposed which requires no sector information and look-up table to calculate duty ratios, with output voltage amplitude 0.866 times that of the input voltage and the input power factor controllable [13, 16-17]. This has already been explained under Section 4.4 of Chapter IV. The model of three phase AC to three phase AC MC delta-sigma modulated using Ned Mohan algorithm is already explained in Section 11.5 and 11.6 of Chapter XI. Here the model of the above MC is developed in PSIM9[52]. This PSIM model of the above MC is shown in Fig. 14.16. The simulation parameters are shown in Table 11.4 of Chapter XI. The simulation results using PSIM are shown in Fig. 14.17(A) to 14.17(L) and Fig. 14.18(A) to 14.18(L). The simulation results are also tabulated in Table 14.9.

TABLE 14.9: Delta-Sigma Modulateed PH3 MC-PSIM Simulation Results 2

Sl.No.	Frequency Input-Output Hz	Line to Neutral Output voltage THD (p.u.)	Line to Line Output Voltage THD (p.u.)	Input current THD (p.u.)	Load current THD (p.u.)
1)	50 – 50	2.379	1.986	4.462	1.491
2)	50 – 10	1.770	2.144	3.926	2.190

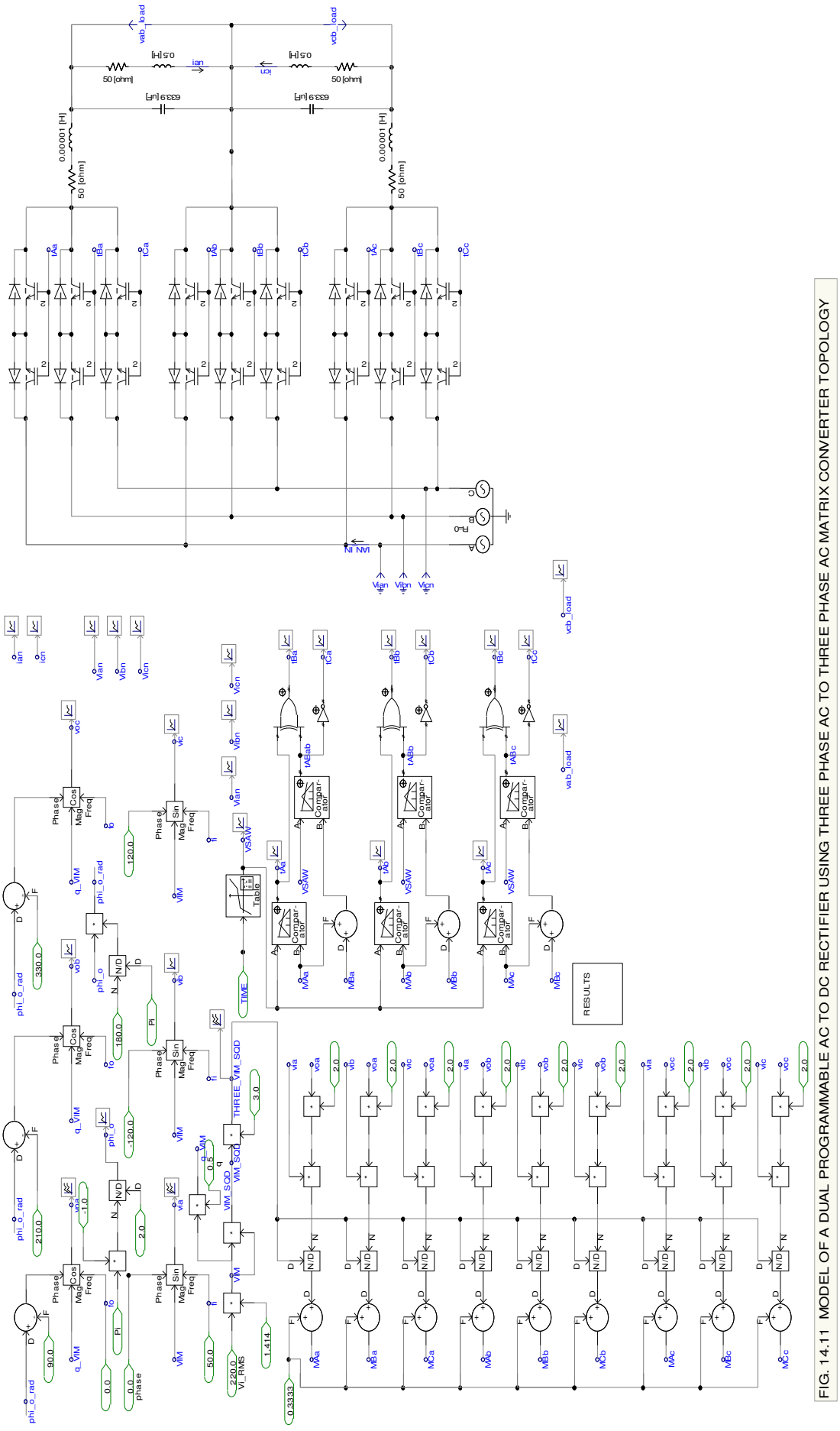


FIG. 14.11 MODEL OF A DUAL PROGRAMMABLE AC TO DC RECTIFIER USING THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER TOPOLOGY

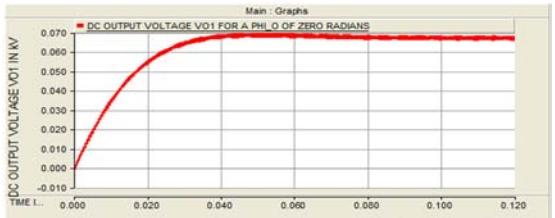
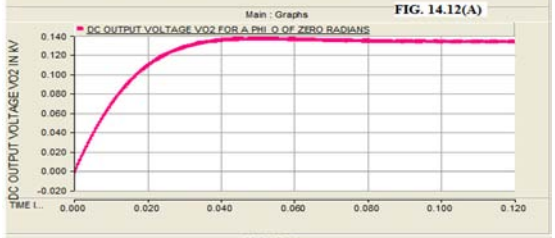


FIG. 14.12(A)



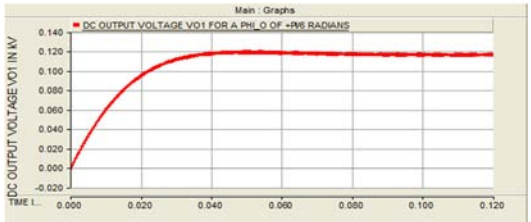
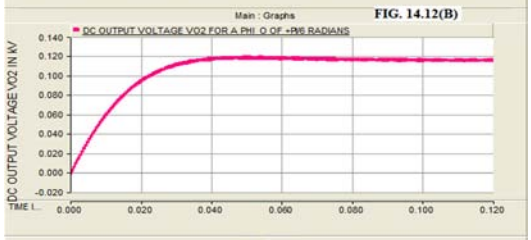


FIG. 14.12(B)



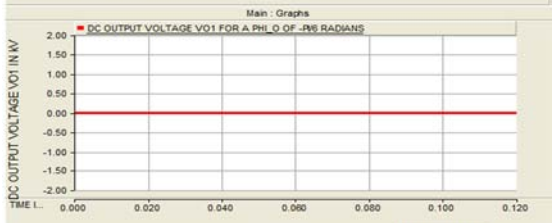
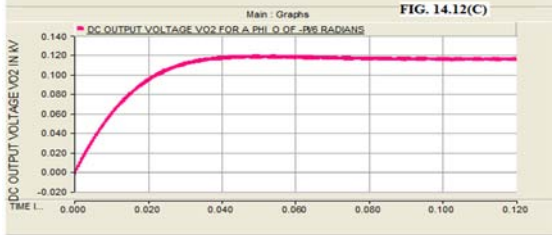


FIG. 14.12(C)



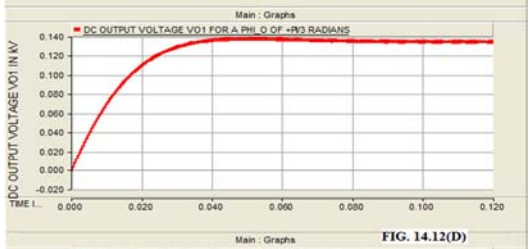


FIG. 14.12(D)

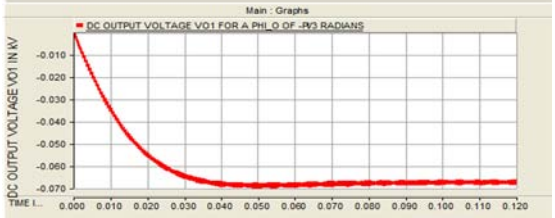


FIG. 14.12(E)

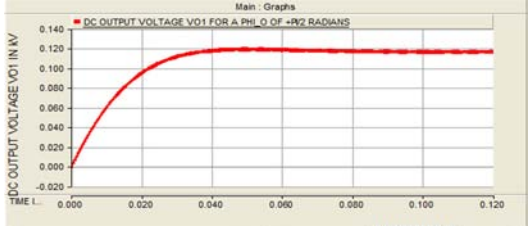


FIG. 14.12(F)

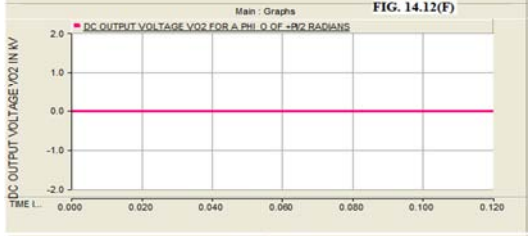
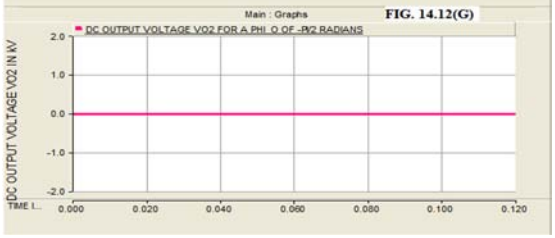


FIG. 14.12(G)



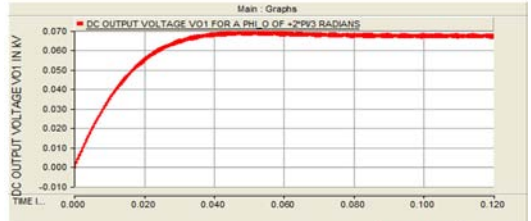
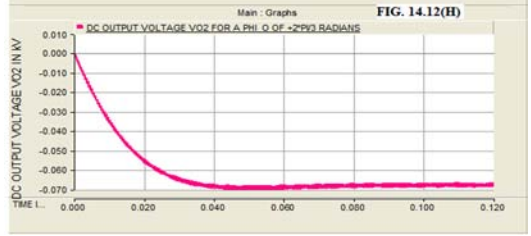
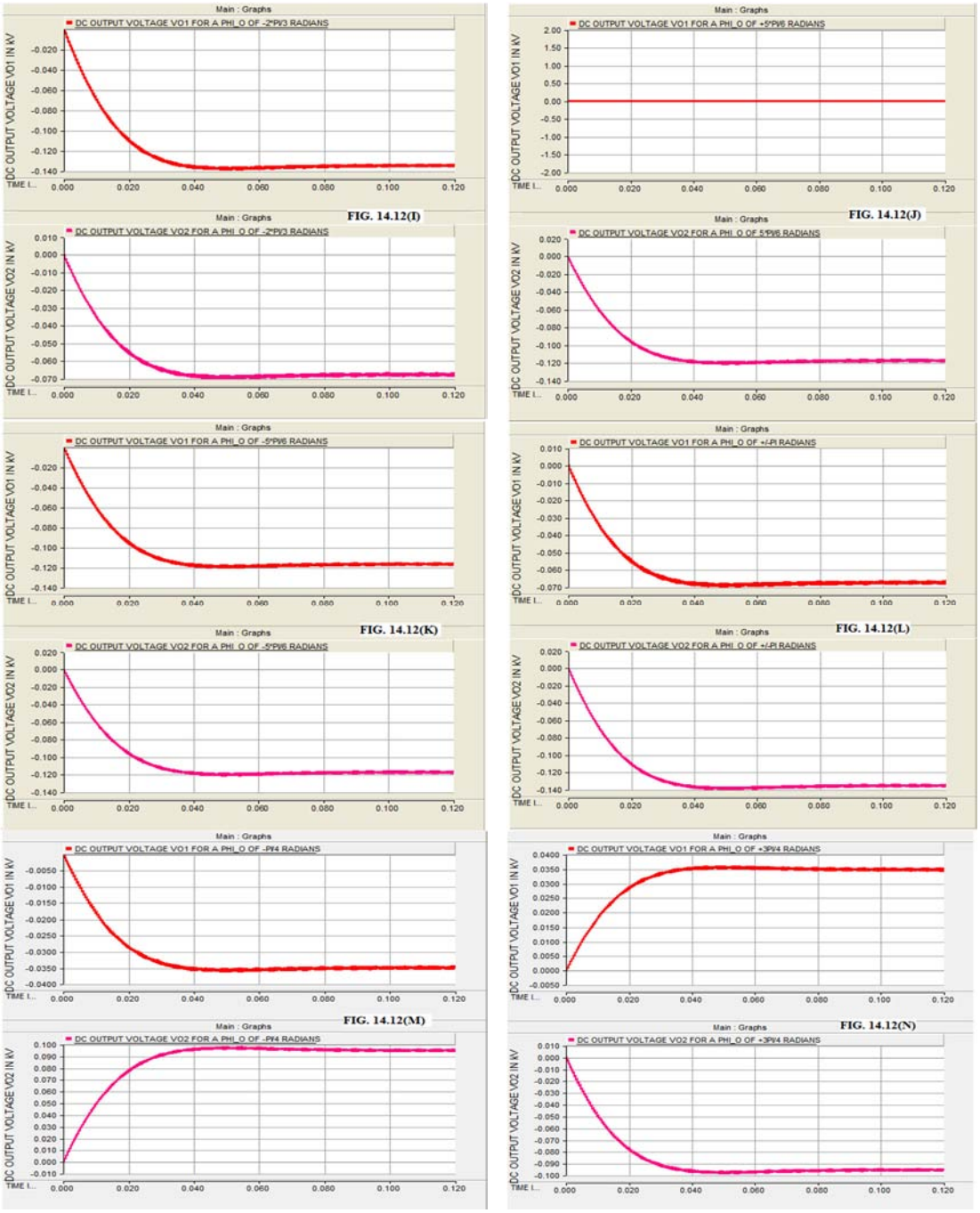


FIG. 14.12(H)





14.10 THREE PHASE INDUCTION MOTOR LOAD: The three phase delta-sigma modulated MC using Venturini and Advanced Modulation algorithm driving a three phase Induction Motor (IM) load are already discussed in Section 11.6 of Chapter XI. The parameters of the IM are given in Table 11.6 of Chapter XI. In this section the model of the above MC driving an IM is reviewed using PSIM9 [52].

The PSIM model of the delta-sigma modulated MC using Venturini modulation algorithm driving the IM is shown in Fig. 14.19. The simulation results are shown in Fig. 14.20. The PSIM model of the delta-sigma modulated MC using Advanced modulation algorithm driving the IM is shown in Fig.

14.21. The simulation results are shown in Fig. 14.22. In both cases the external mechanical load applied is zero.

14.11 SINGLE PHASE AC TO THREE PHASE AC MATRIX CONVERTER: The detailed analysis, design of compensation capacitor and modelling of a single phase AC to three phase AC MC has already been discussed in Chapter XII. In this chapter the modelling of the above MC is reviewed using PSIM9 [52]. The parameters of the three phase Induction Motor and the values of the parameters used for the three phase input voltage, input and output frequency, saw-tooth carrier frequency, modulation index, filter inductor, filter capacitor and compensation capacitor are given in Table 12.1 and 12.2 of Chapter XII respectively. The PSIM model of the above MC driving the IM is shown in Fig. 14.23 and the simulation results are shown in Fig. 14.24(A) and Fig. 14.24 (B). The PSIM model of the above MC connected to a static R-L load is shown in Fig. 14.25 and the simulation results are shown in Fig. 14.26(A) for an output frequency of 50 Hz and in Fig. 14.26(B) for an output frequency of 20 Hz respectively.

14.12 DIRECT SPACE VECTOR MODULATION OF MATRIX CONVERTER: The modelling of MC using Direct Asymmetrical Space Vector Modulation (ASVM) technique is discussed in Section 8.2 and 8.3 of Chapter VIII. The modelling of three phase ASVM MC using PSIM9 [52] is reviewed here. The model of the Direct ASVM three phase AC to three phase AC MC is developed using PSIM in the same way as discussed in Section 8.3 of Chapter VIII. This model is shown in Fig. 14.27. The parameters are shown in Table 8.6 of Chapter VIII. The simulation results for output frequencies of 50 Hz and 20 Hz are shown in Figs. 14.28(A) to 14.28(I) and in Fig. 14.29(A) to 14.29(I) respectively. The simulation results are tabulated in Table 14.10.

TABLE 14.10: PH3 ASVM MC – PSIM Simulation Results

Sl.No.	Three Phase ASVM MC Input – Output Frequency Hz	Line to Line Output Voltage THD p.u.	Line to Neutral Output Voltage THD p.u.	Load Current THD p.u.
1)	50 – 50	0.720	1.136	0.182
2)	50 – 20	0.950	1.668	0.320

The model of the Direct Symmetrical Space Vector Modulated (SSVM) MC using SIMULINK is already discussed in Section 8.5 of Chapter VIII. The model of the three phase Direct SSVM MC using PSIM9 [52] is reviewed here. The PSIM model of three phase Direct SSVM MC is shown in Fig. 14.30. This model is developed in the same way as discussed in Section 8.5 of Chapter VIII. The simulation results for output frequencies of 50 Hz and 20 Hz are shown in Figs. 14.31(A) to 14.31(I) and in Figs. 14.32(A) to 14.32(I) respectively. The simulation results are tabulated in Table 14.11.

TABLE 14.11: PH3 SSVM MC – PSIM Simulation Results

Sl.No.	Three Phase SSVM MC Input – Output Frequency Hz	Line to Line Output Voltage THD p.u.	Line to Neutral Output Voltage THD p.u.	Load Current THD p.u.
1)	50 – 50	0.8368	1.75	0.406
2)	50 – 20	0.9197	1.782	0.4188

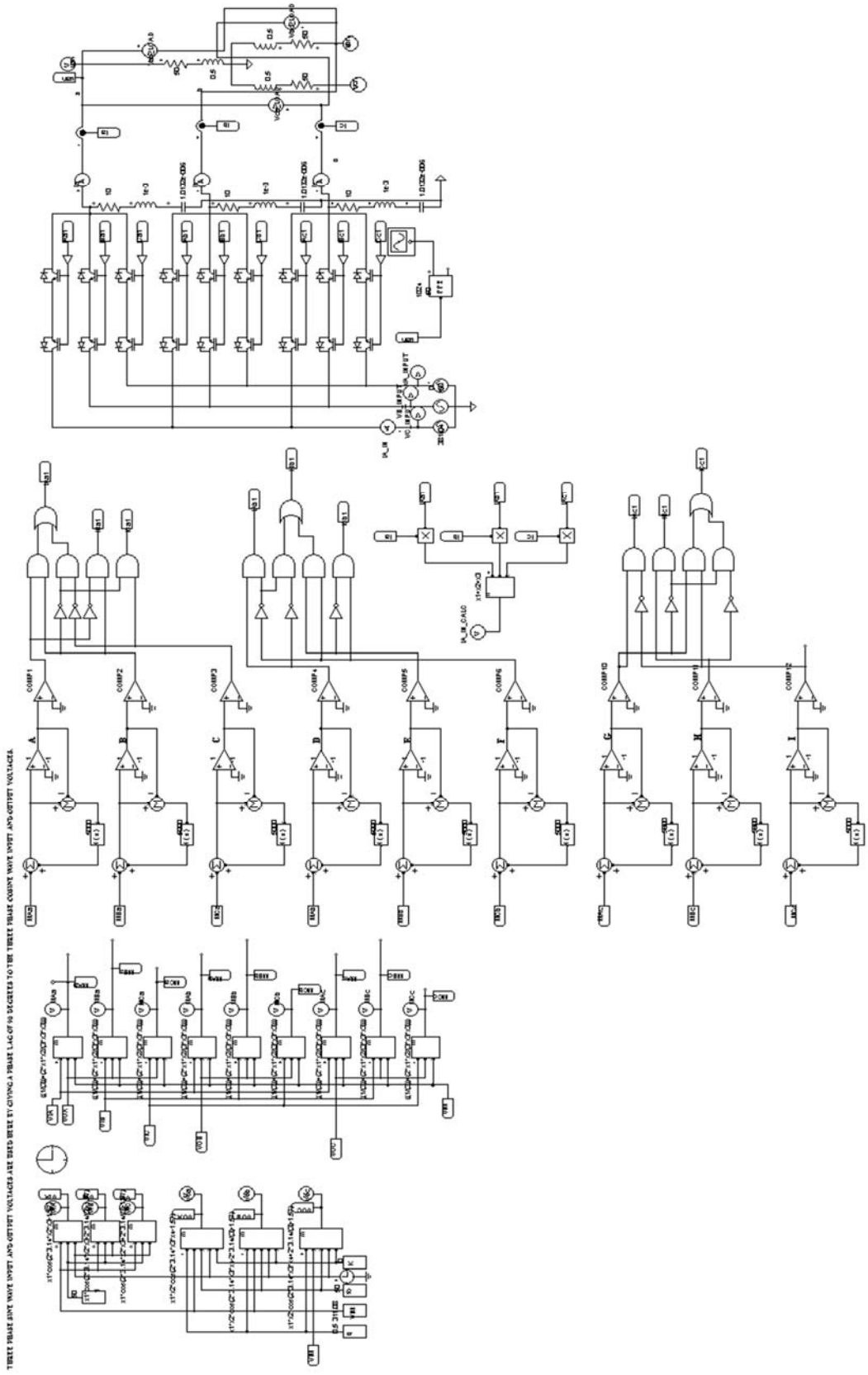
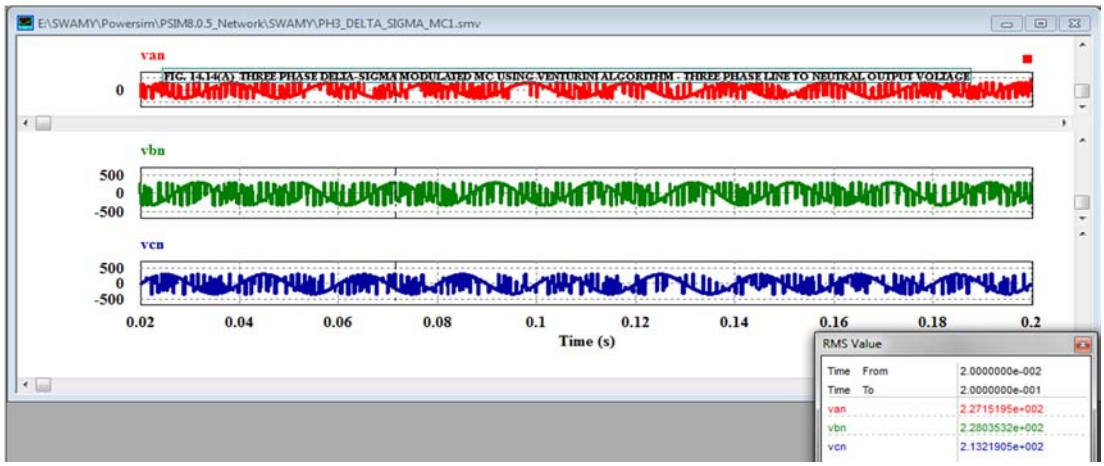
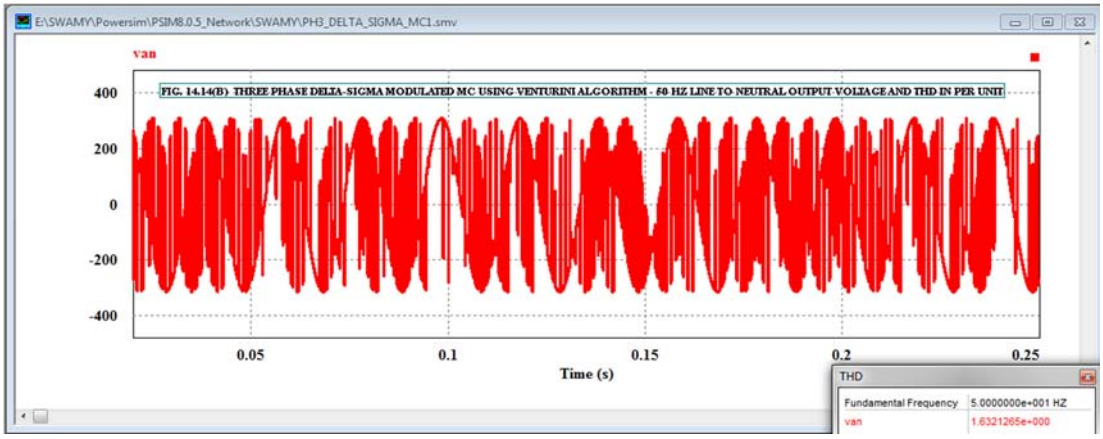
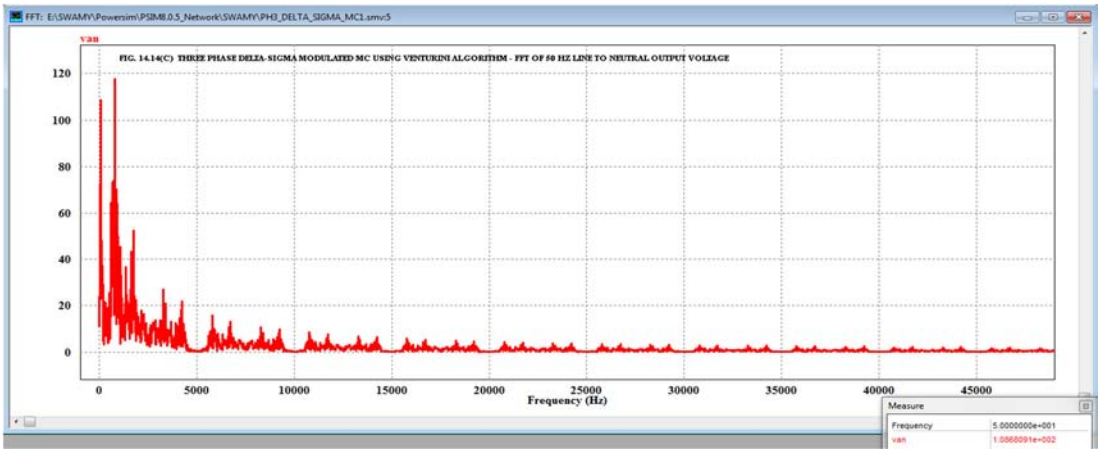
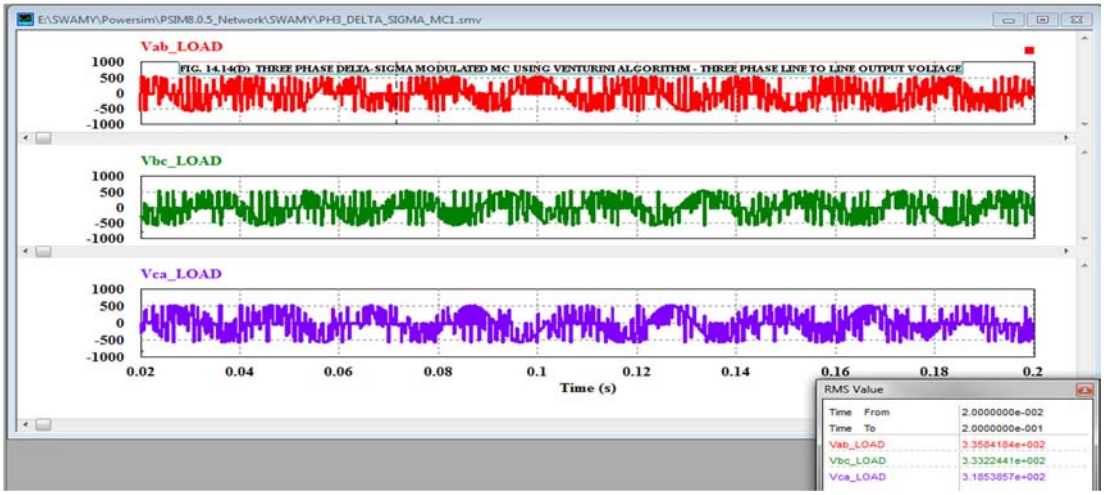


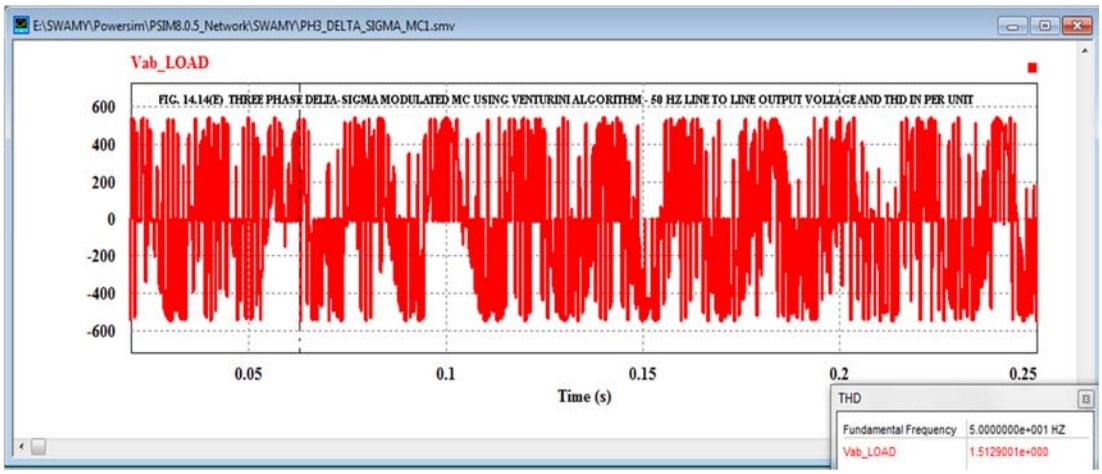
FIG. 14.13 MODEL OF THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MC - DELTA-SIGMA MODULATED USING VENTURINI ALGORITHM

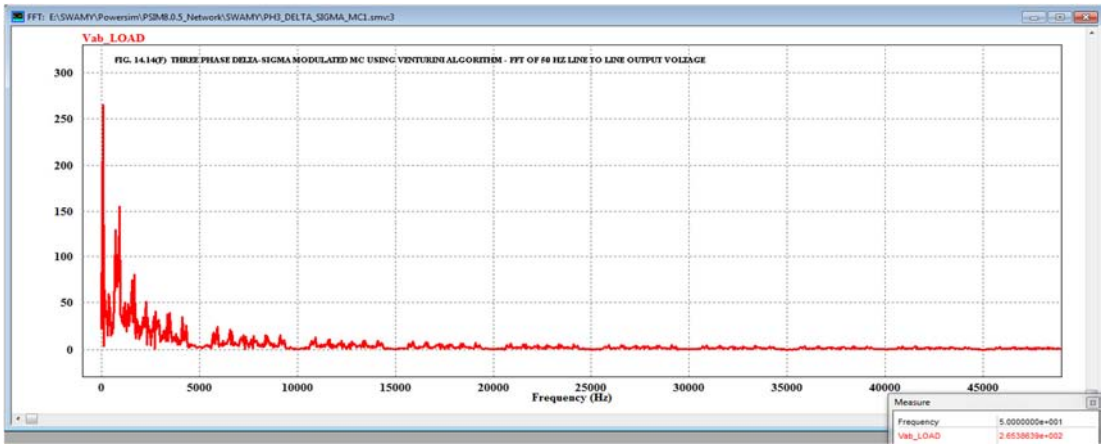

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv
van
FIG. 14.14(A) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - THREE PHASE LINE TO NEUTRAL OUTPUT VOLTAGE
vbn
vcn
Time (s)
RMS Value
Time From 2.0000000e-002
Time To 2.0000000e-001
van 2.2715195e+002
vbn 2.2803532e+002
vcn 2.1321905e+002

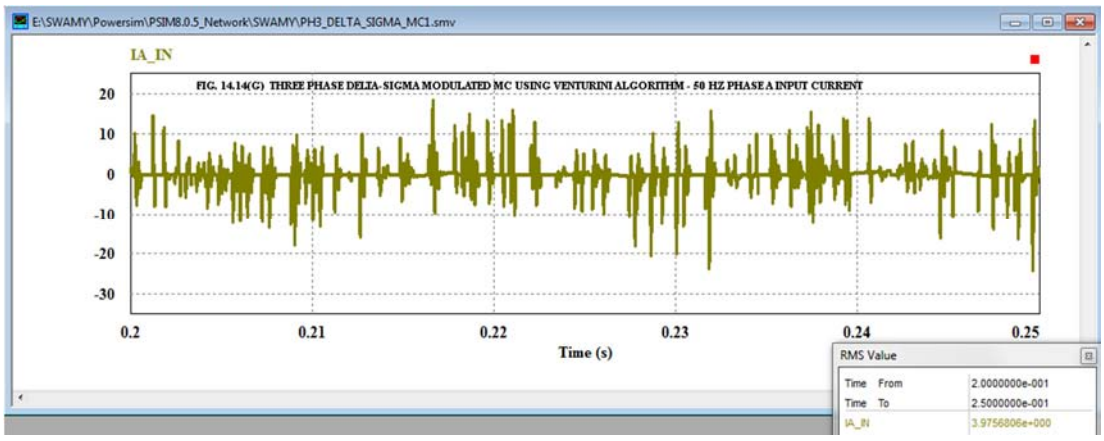

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv
van
FIG. 14.14(B) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - 60 HZ LINE TO NEUTRAL OUTPUT VOLTAGE AND THD IN PER UNIT
Time (s)
THD
Fundamental Frequency 5.0000000e+001 HZ
van 1.6321265e+000

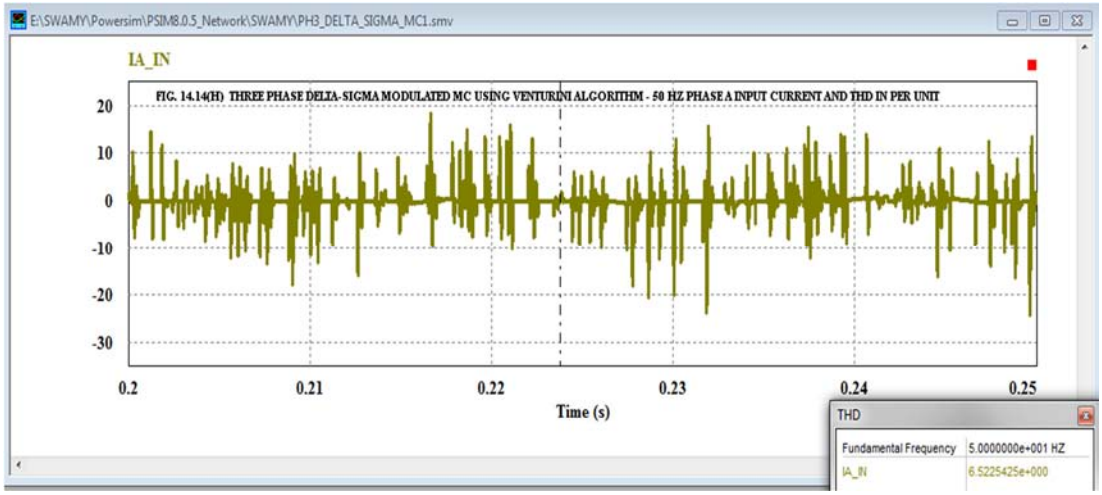

FFT: E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv:5
van
FIG. 14.14(C) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - FFT OF 60 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
Frequency (Hz)
Measure
Frequency 5.0000000e+001

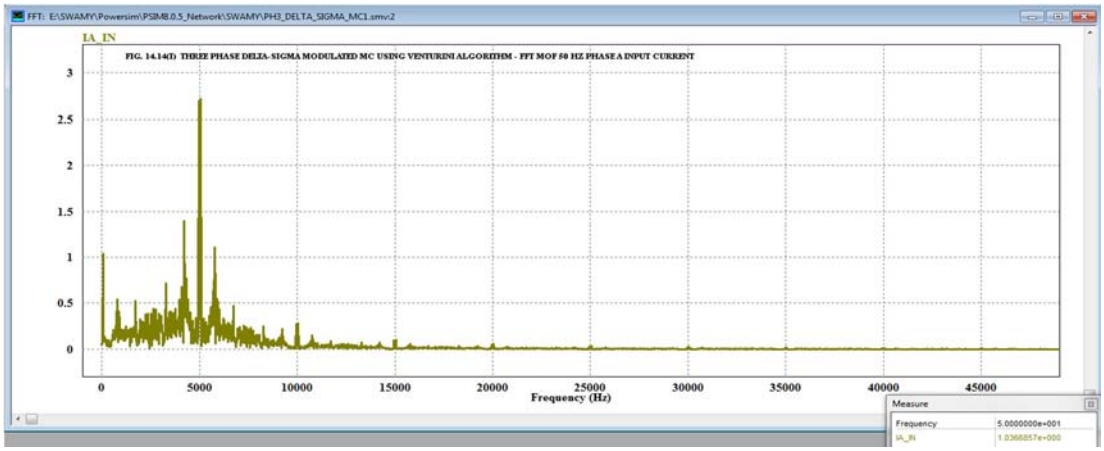

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv
Vab_LOAD
FIG. 14.14(D) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - THREE PHASE LINE TO LINE OUTPUT VOLTAGE
Vbc_LOAD
Vca_LOAD
Time (s)
RMS Value
Time From 2.0000000e-002
Time To 2.0000000e-001
Vab_LOAD 3.3584184e+002
Vbc_LOAD 3.3322441e+002
Vca_LOAD 3.1853857e+002

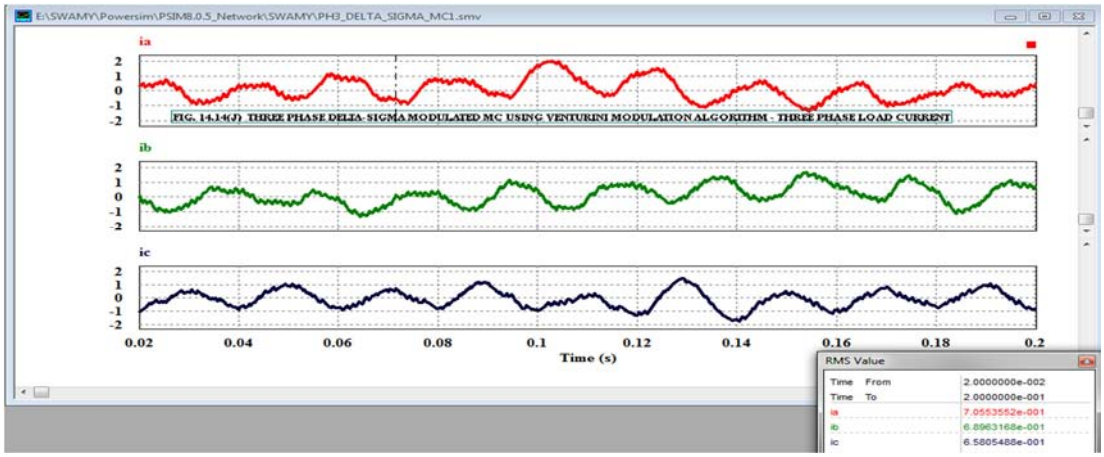

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv
Vab_LOAD
FIG. 14.14(E) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - 50 HZ LINE TO LINE OUTPUT VOLTAGE AND THD IN PER UNIT
600
400
200
0
-200
-400
-600
0.05
0.1
0.15
0.2
0.25
Time (s)
THD
Fundamental Frequency
5.0000000e+001 HZ
Vab_LOAD
1.5129001e+000

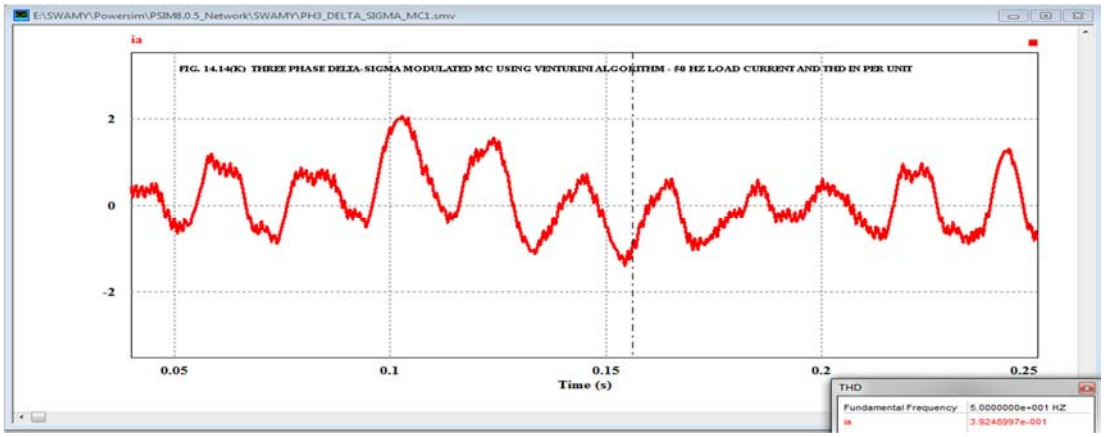

FFT: E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv:3
Vab_LOAD
FIG. 14.14(F) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - FFT OF 50 HZ LINE TO LINE OUTPUT VOLTAGE
300
250
200
150
100
50
0
0
5000
10000
15000
20000
25000
30000
35000
40000
45000
Frequency (Hz)
Measure
Frequency
5.0000000e+001
Vab_LOAD
2.6538639e+002

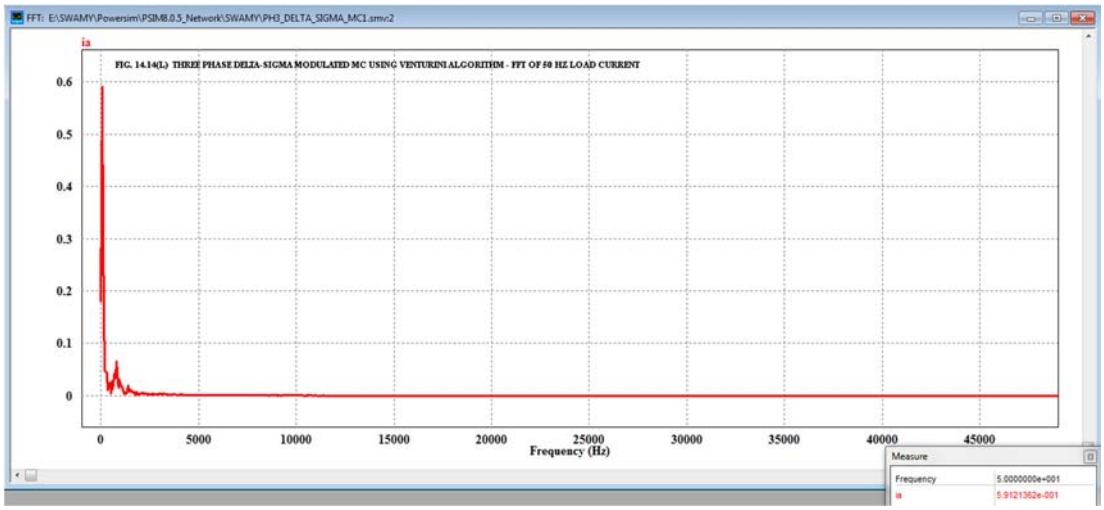

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv
IA_IN
FIG. 14.14(G) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - 50 HZ PHASE A INPUT CURRENT
20
10
0
-10
-20
-30
0.2
0.21
0.22
0.23
0.24
0.25
Time (s)
RMS Value
Time From
2.0000000e-001
Time To
2.5000000e-001
IA_IN
3.9756806e+000

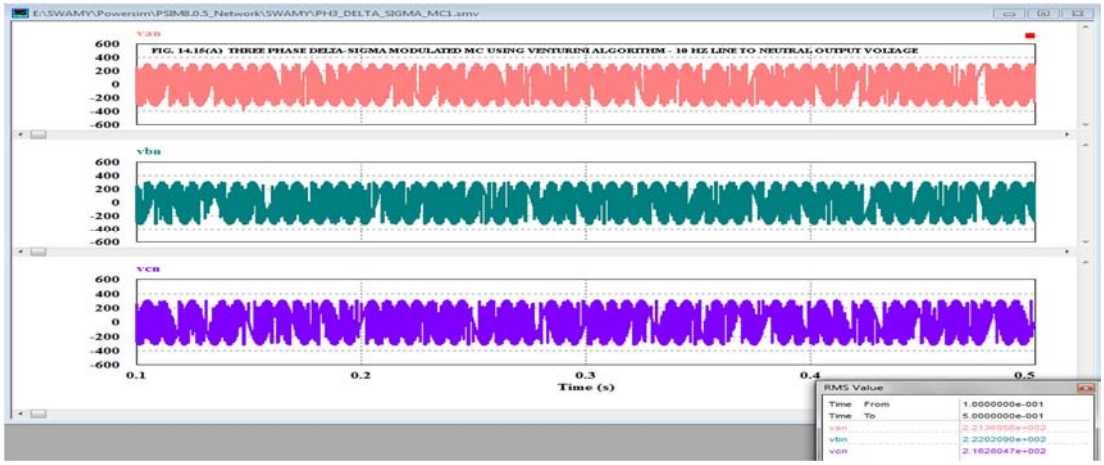

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv
IA_IN
FIG. 14.14(H) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - 50 HZ PHASE A INPUT CURRENT AND THD IN PER UNIT
20
10
0
-10
-20
-30
0.2
0.21
0.22
0.23
0.24
0.25
Time (s)
THD
Fundamental Frequency
5.0000000e+001 HZ
IA_IN
6.5225425e+000

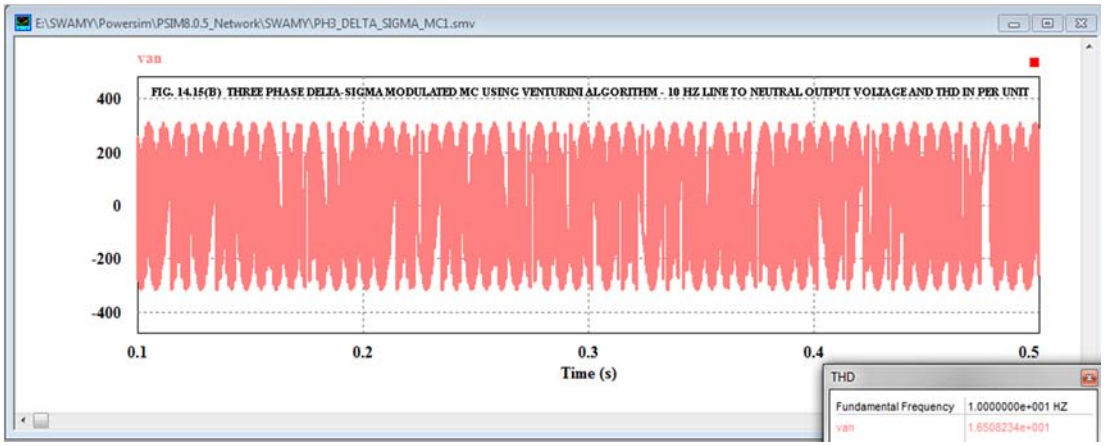

FFT: E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv:2
IA_IN
FIG. 14.14(I) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - FFT MOF 50 HZ PHASE A INPUT CURRENT
Frequency (Hz)
Measure
Frequency 5.0000000e+001
IA_IN 1.0366857e+000

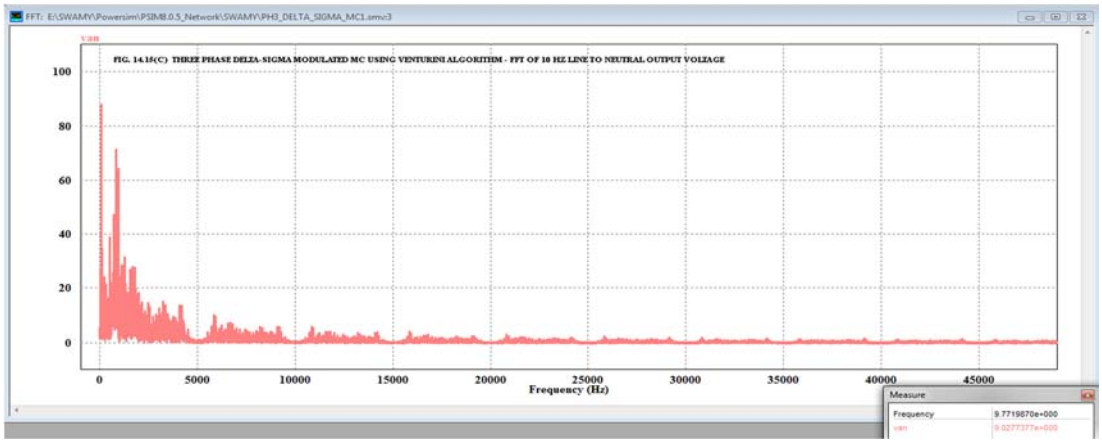

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv
ia
FIG. 14.14(J) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI MODULATION ALGORITHM - THREE PHASE LOAD CURRENT
ib
ic
Time (s)
RMS Value
Time From 2.0000000e-002
Time To 2.0000000e-001
ia 7.0553552e-001
ib 6.8963168e-001
ic 6.5805488e-001

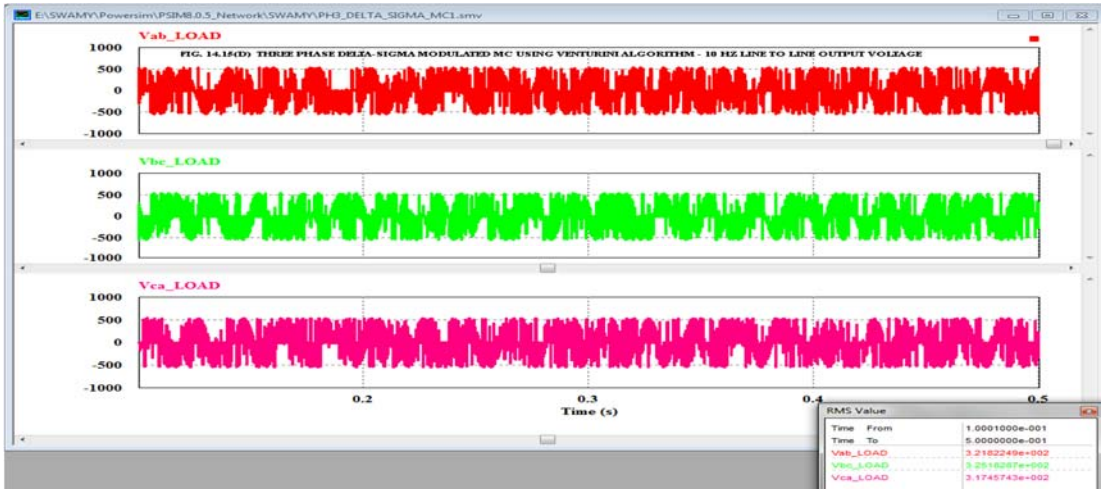

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv
ia
FIG. 14.14(K) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - 50 HZ LOAD CURRENT AND THD IN PER UNIT
Time (s)
THD
Fundamental Frequency 5.0000000e+001 HZ
ia 3.9248997e-001

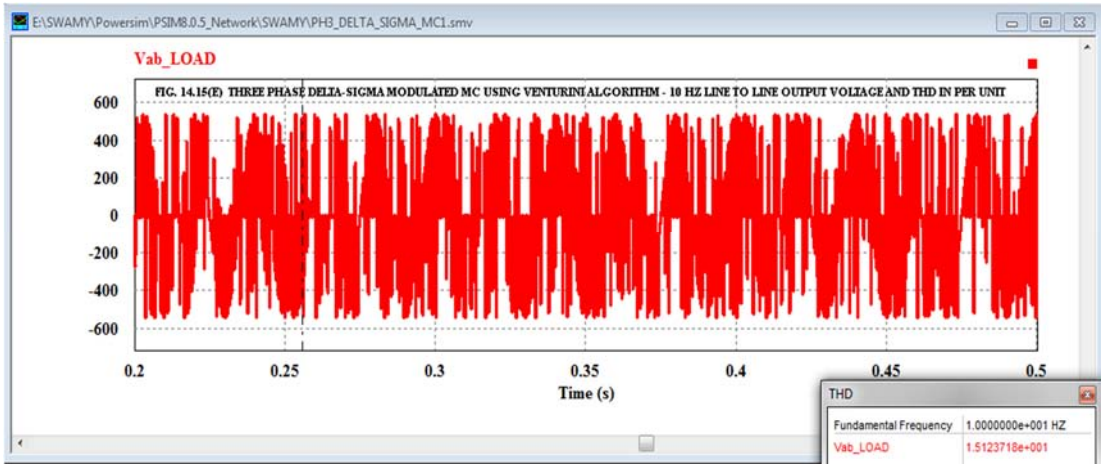

FFT: E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv:2
ia
FIG. 14.14(L) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - FFT OF 50 HZ LOAD CURRENT
Frequency (Hz)
Measure
Frequency 5.0000000e+001
ia 5.9121362e-001

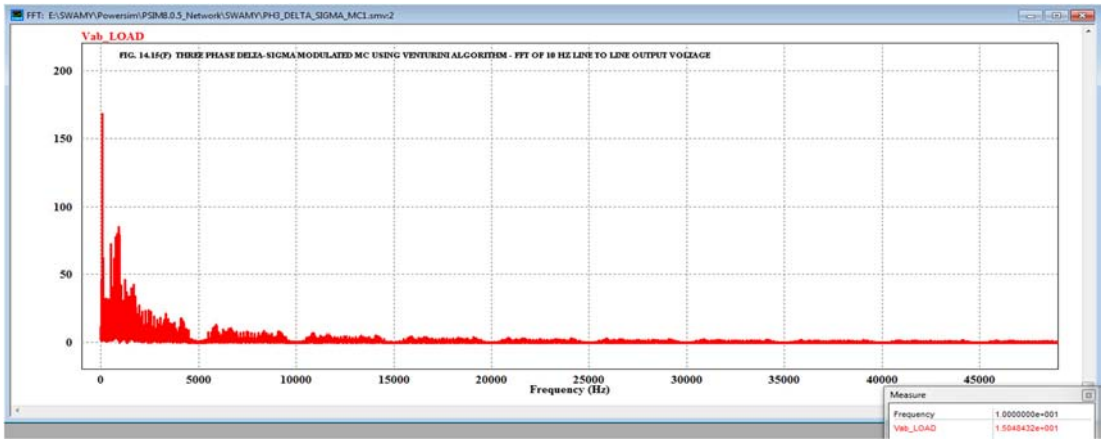

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv
van
FIG. 14.15(A) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - 10 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
vbn
vcn
Time (s)
RMS Value

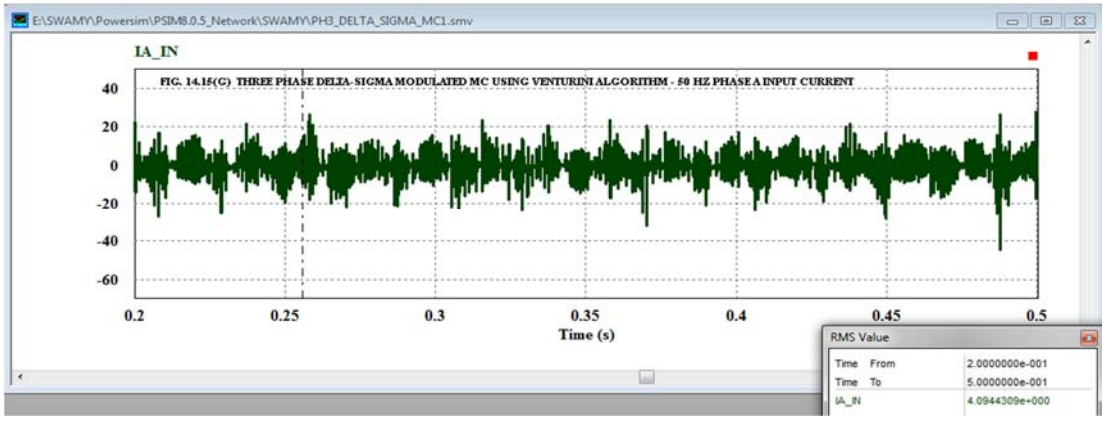

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv
van
FIG. 14.15(B) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - 10 HZ LINE TO NEUTRAL OUTPUT VOLTAGE AND THD IN PER UNIT
Time (s)
THD
Fundamental Frequency
1.0000000e+001 HZ

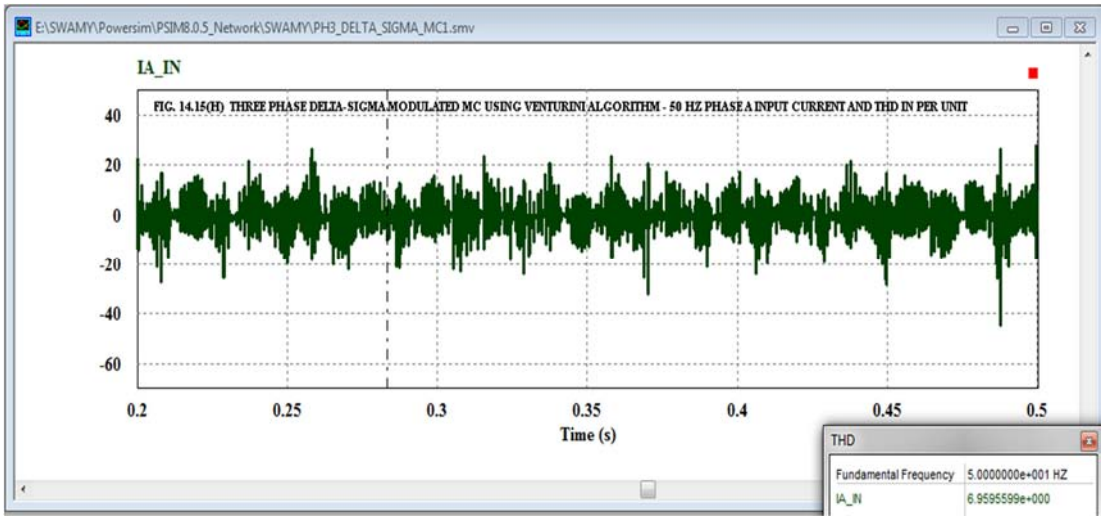

FFT: E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smc3
van
FIG. 14.15(C) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - FFT OF 10 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
Frequency (Hz)
Measure
Frequency

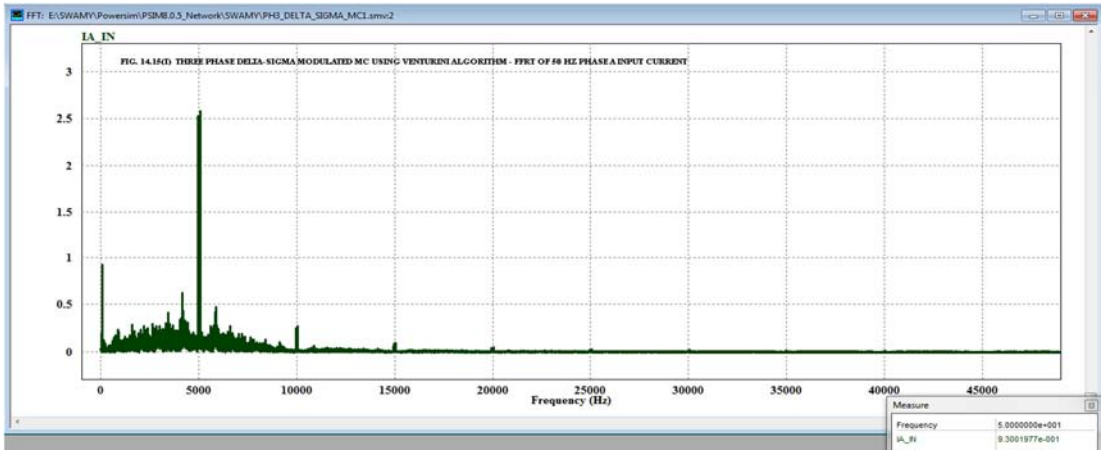

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv
Vab_LOAD
FIG. 14.15(D) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - 10 HZ LINE TO LINE OUTPUT VOLTAGE
Vbc_LOAD
Vca_LOAD
Time (s)
RMS Value

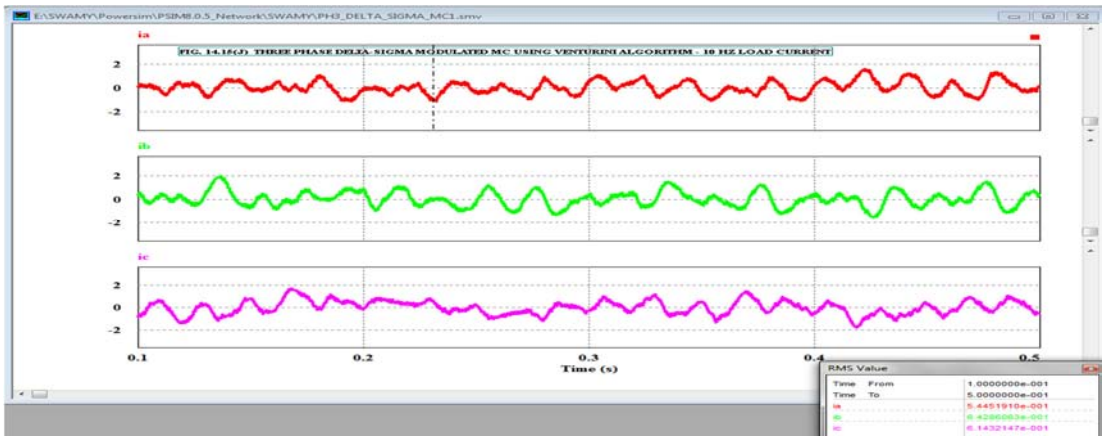

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv
Vab_LOAD
FIG. 14.15(E) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - 10 HZ LINE TO LINE OUTPUT VOLTAGE AND THD IN PER UNIT
600
400
200
0
-200
-400
-600
0.2
0.25
0.3
0.35
0.4
0.45
0.5
Time (s)
THD
Fundamental Frequency
1.0000000e+001 HZ
Vab_LOAD
1.5123718e+001

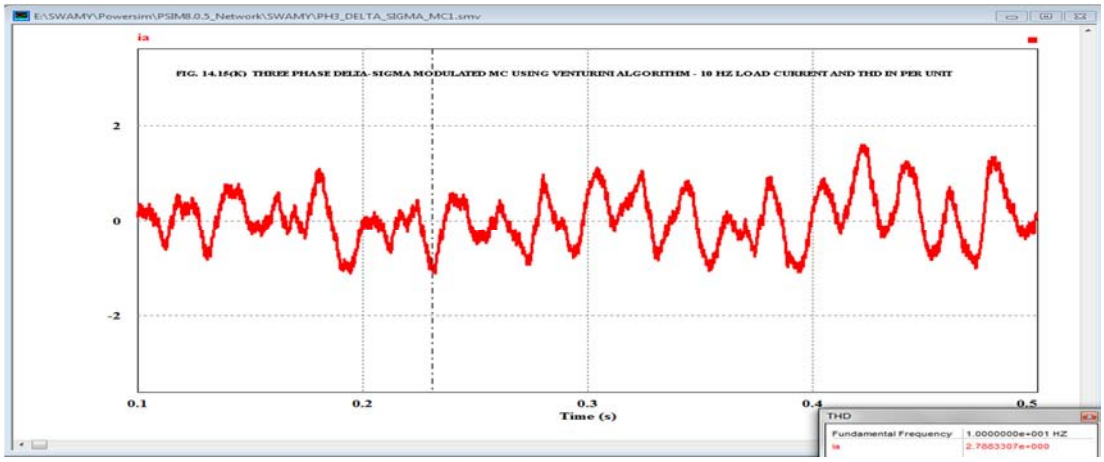

FFT: E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv:2
Vab_LOAD
FIG. 14.15(F) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - FFT OF 10 HZ LINE TO LINE OUTPUT VOLTAGE
200
150
100
50
0
0
5000
10000
15000
20000
25000
30000
35000
40000
45000
Frequency (Hz)
Measure
Frequency
1.0000000e+001
Vab_LOAD
1.5048432e+001

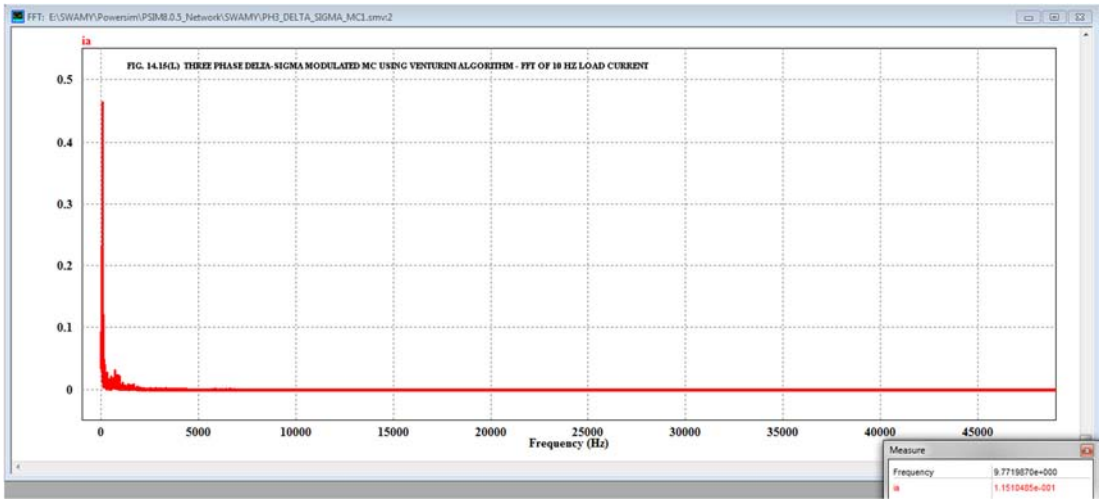

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv
IA_IN
FIG. 14.15(G) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - 50 HZ PHASE A INPUT CURRENT
40
20
0
-20
-40
-60
0.2
0.25
0.3
0.35
0.4
0.45
0.5
Time (s)
RMS Value
Time From
2.0000000e-001
Time To
5.0000000e-001
IA_IN
4.0944309e+000


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_DELTA_SIGMA_MC1.smv
IA_IN
FIG. 14.15(H) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - 50 HZ PHASE A INPUT CURRENT AND THD IN PER UNIT
40
20
0
-20
-40
-60
0.2
0.25
0.3
0.35
0.4
0.45
0.5
Time (s)
THD
Fundamental Frequency
5.0000000e+001 HZ
IA_IN
6.9595599e+000


IA_IN
FIG. 14.15(I) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - FFRT OF 50 HZ PHASE A INPUT CURRENT
Frequency (Hz)


ia
FIG. 14.15(J) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - 10 HZ LOAD CURRENT
ib
ic
Time (s)
RMS Value


ia
FIG. 14.15(K) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - 10 HZ LOAD CURRENT AND THD IN PER UNIT
Time (s)
THD


ia
FIG. 14.15(L) THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - FFT OF 10 HZ LOAD CURRENT
Frequency (Hz)

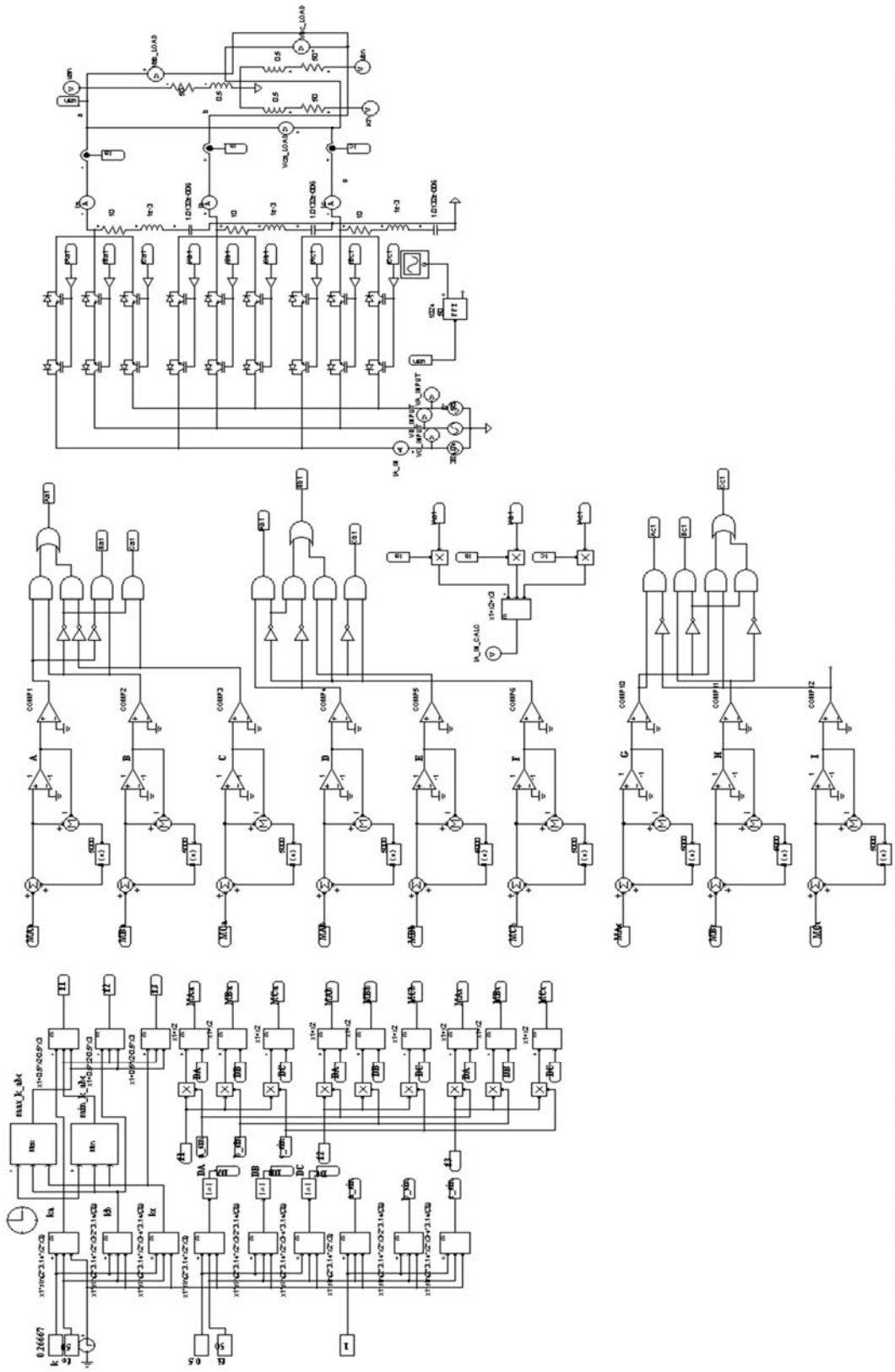
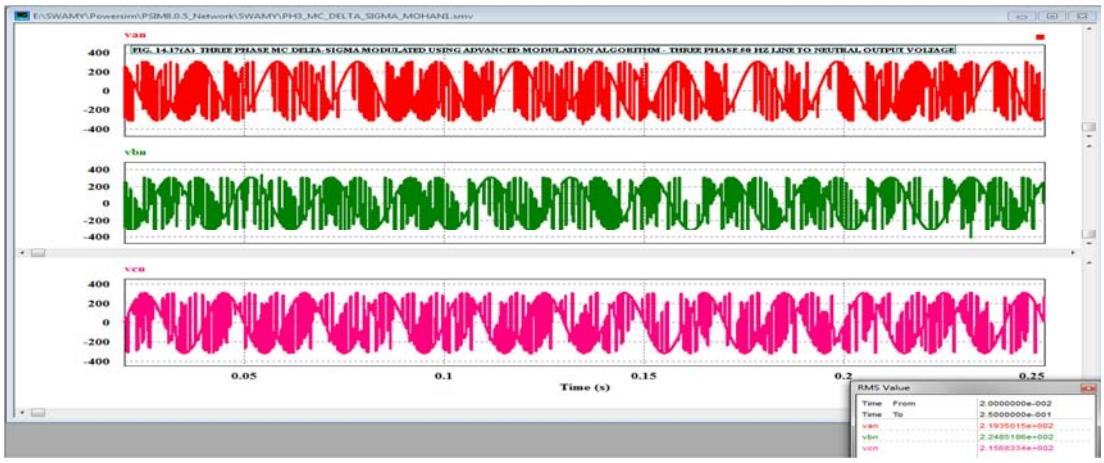
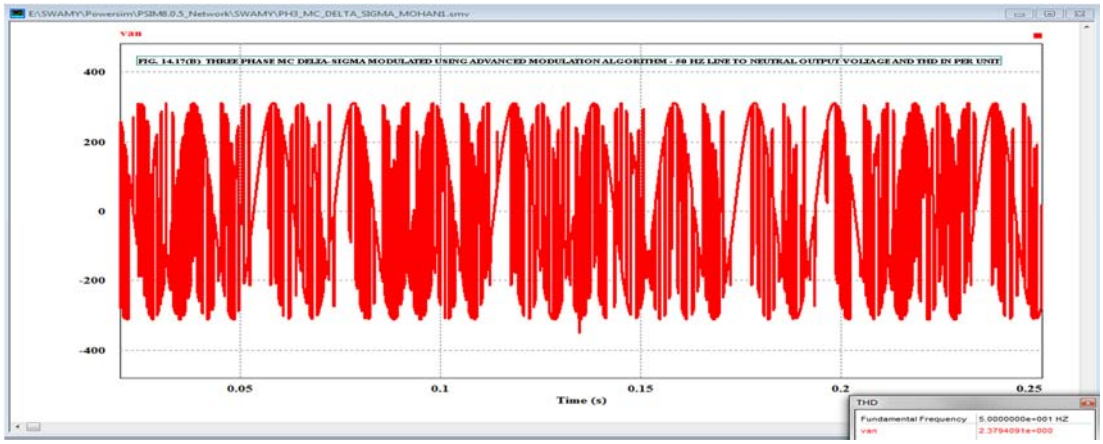
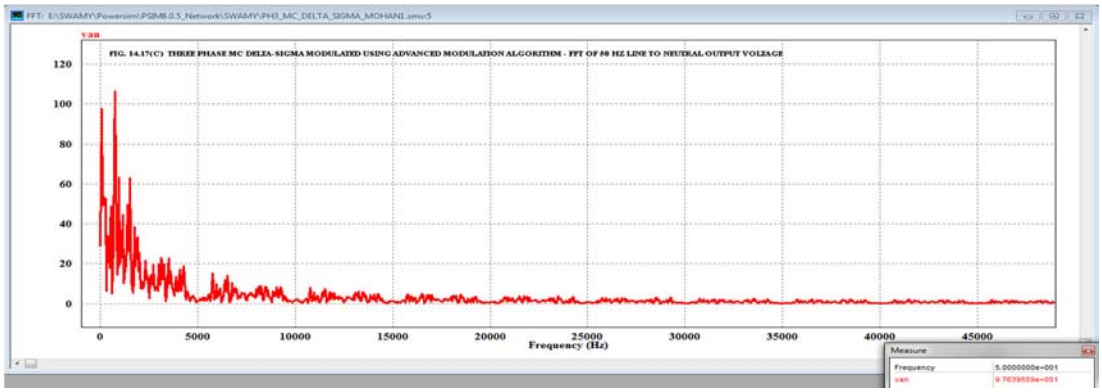
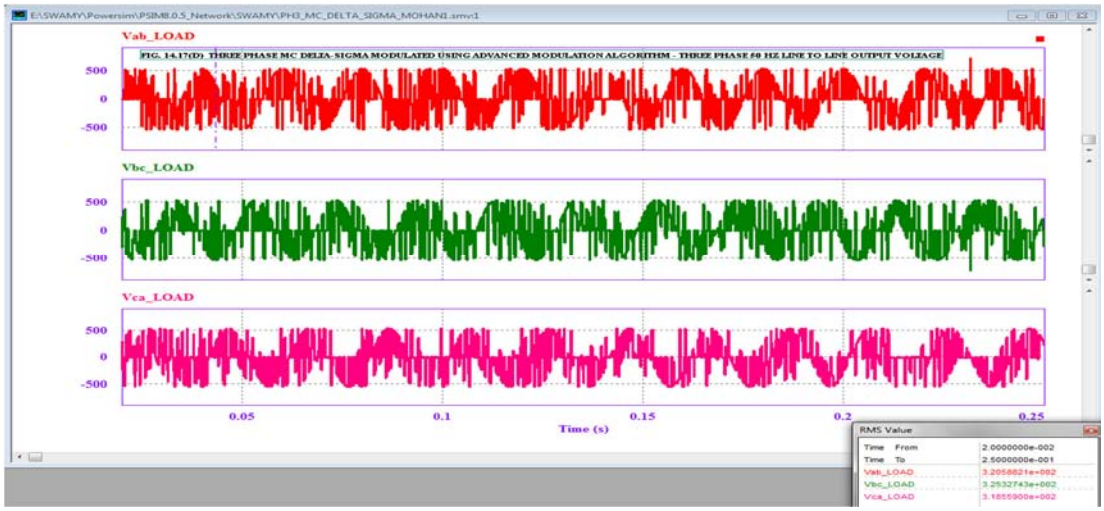


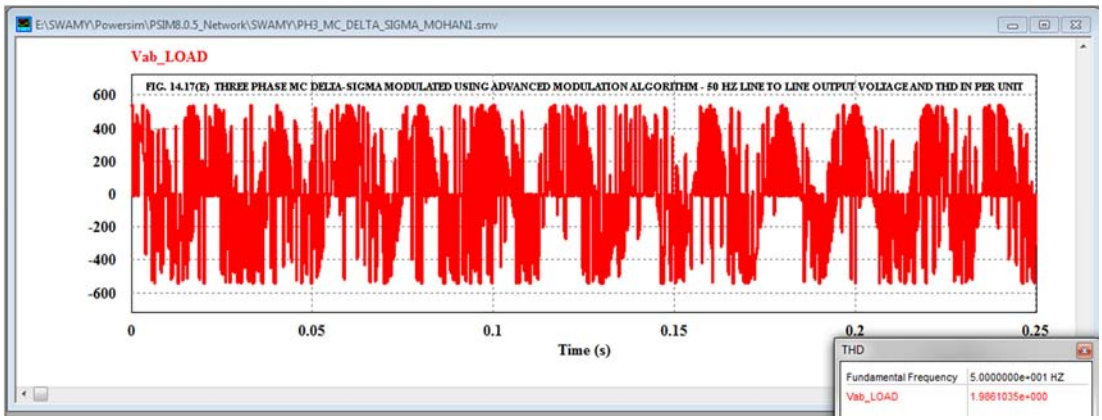
FIG. 14.16 MODEL OF THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MC - DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM

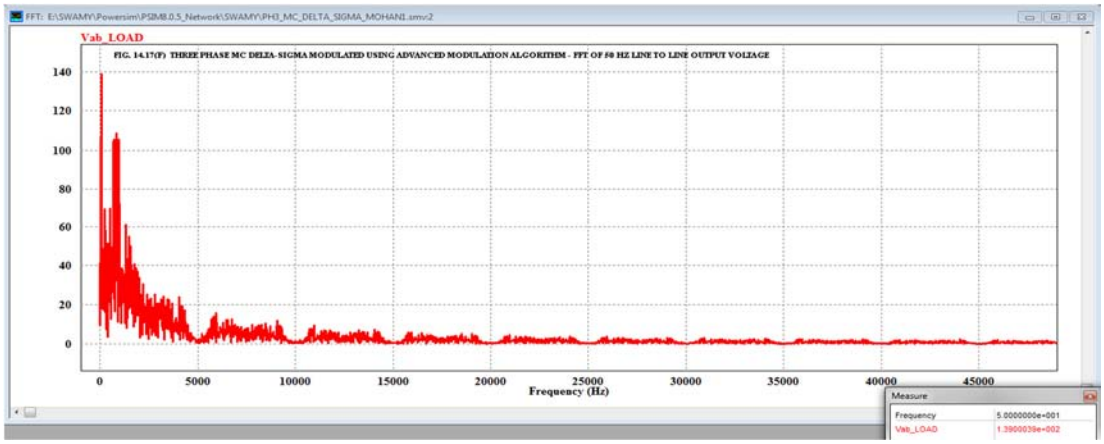

van
FIG. 14.17(A) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - THREE PHASE 60 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
vbn
vcn
Time (s)
RMS Value

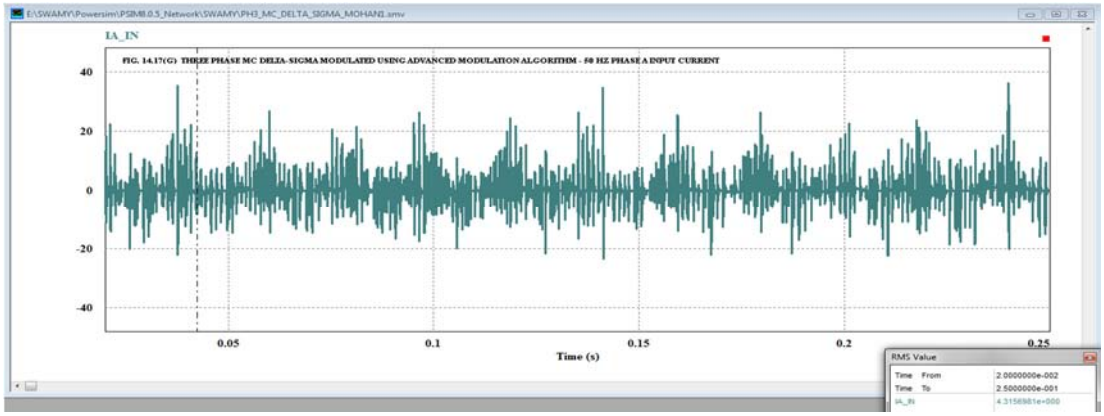

van
FIG. 14.17(B) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - 60 HZ LINE TO NEUTRAL OUTPUT VOLTAGE AND THD IN PER UNIT
Time (s)
THD
Fundamental Frequency

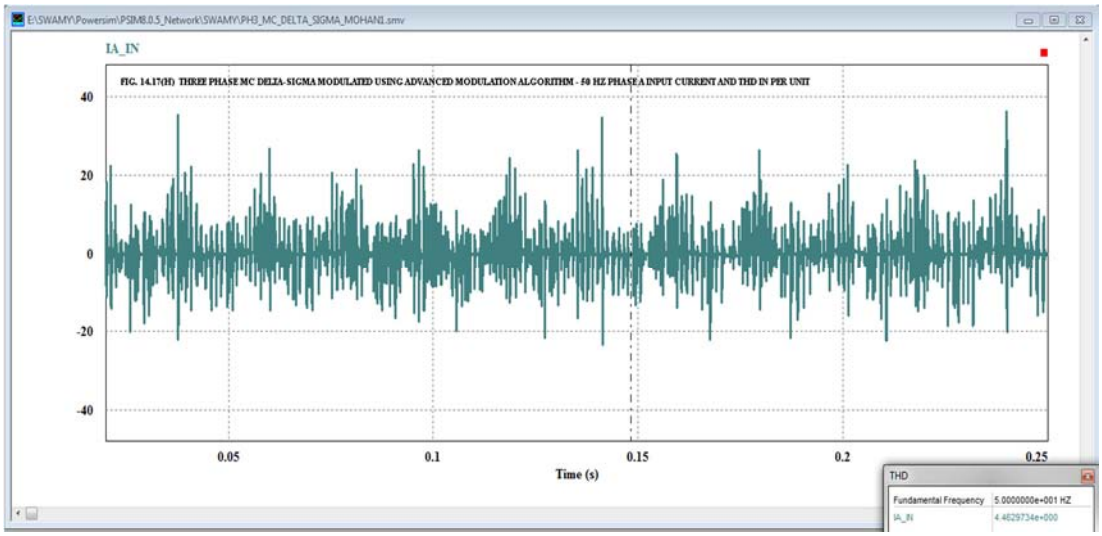

van
FIG. 14.17(C) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - FFT OF 60 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
Frequency (Hz)
Measure

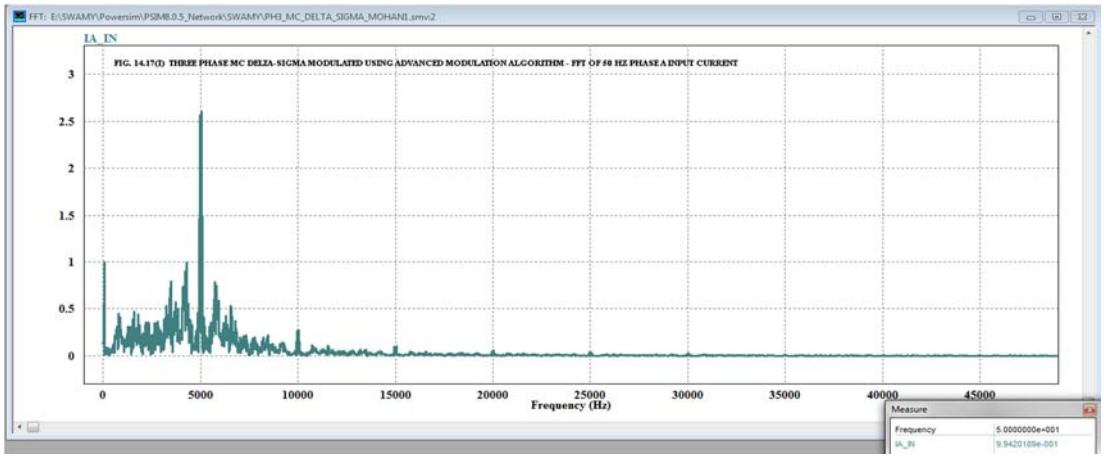

Vab_LOAD
FIG. 14.17(D) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - THREE PHASE 60 HZ LINE TO LINE OUTPUT VOLTAGE
Vbc_LOAD
Vca_LOAD
Time (s)
RMS Value

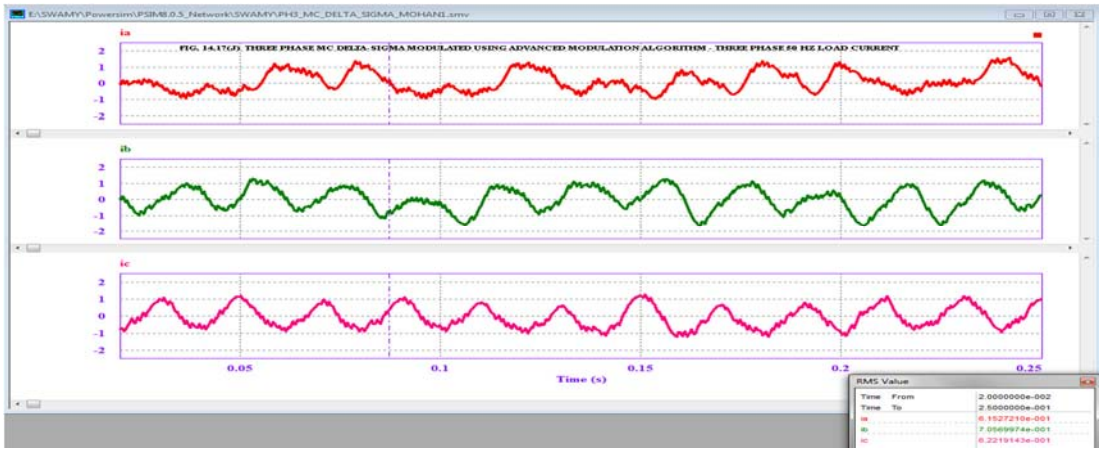

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_DELTA_SIGMA_MOHAN1.smv
Vab_LOAD
FIG. 14.17(E) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - 50 HZ LINE TO LINE OUTPUT VOLTAGE AND THD IN PER UNIT
600
400
200
0
-200
-400
-600
0
0.05
0.1
0.15
0.2
0.25
Time (s)
THD
Fundamental Frequency
5.0000000e+001 HZ
Vab_LOAD
1.9861035e+000

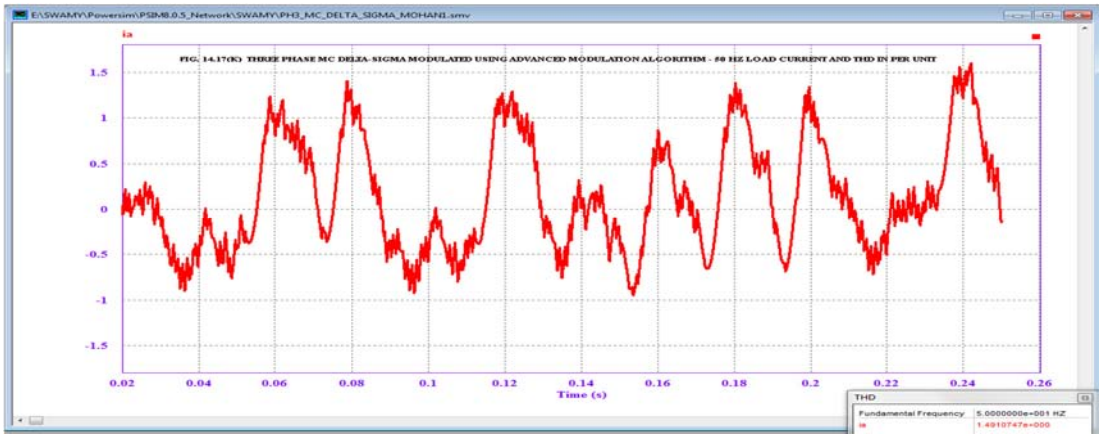

Vab_LOAD
FIG. 14.17(F) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - FFT OF 50 HZ LINE TO LINE OUTPUT VOLTAGE
140
120
100
80
60
40
20
0
0
5000
10000
15000
20000
25000
30000
35000
40000
45000
Frequency (Hz)
Measure
Frequency
5.0000000e+001
Vab_LOAD
1.3900039e+002

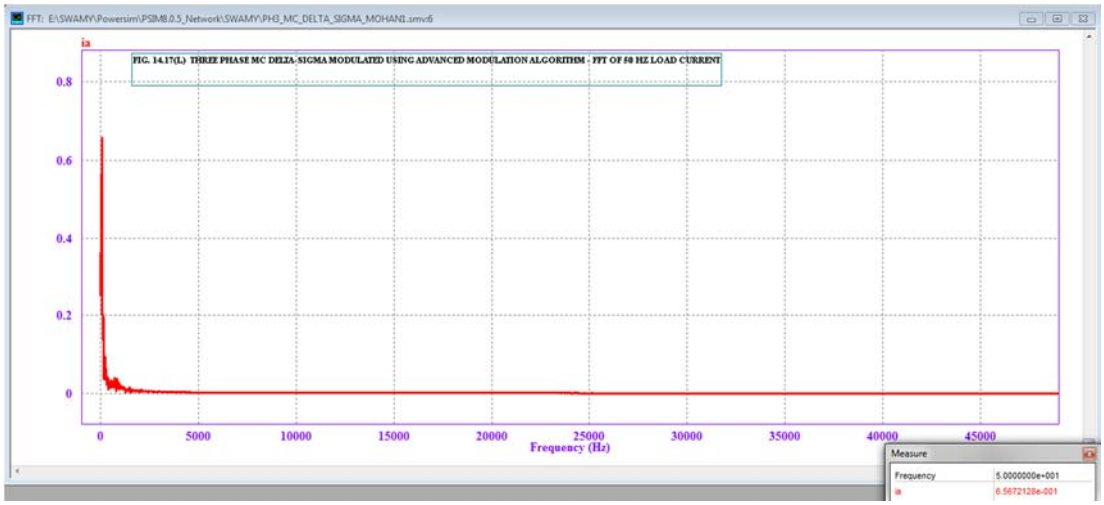

IA_IN
FIG. 14.17(G) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - 50 HZ PHASE A INPUT CURRENT
40
20
0
-20
-40
0.05
0.1
0.15
0.2
0.25
Time (s)
RMS Value
Time From
2.0000000e-002
Time To
2.5000000e-001
IA_IN
4.3156981e+000

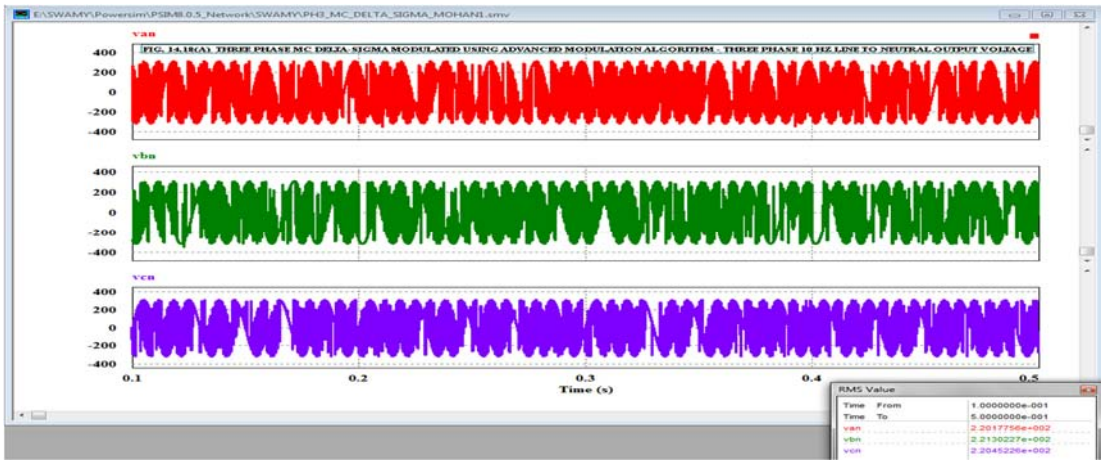

IA_IN
FIG. 14.17(H) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - 50 HZ PHASE A INPUT CURRENT AND THD IN PER UNIT
40
20
0
-20
-40
0.05
0.1
0.15
0.2
0.25
Time (s)
THD
Fundamental Frequency
5.0000000e+001 HZ
IA_IN
4.4629734e+000

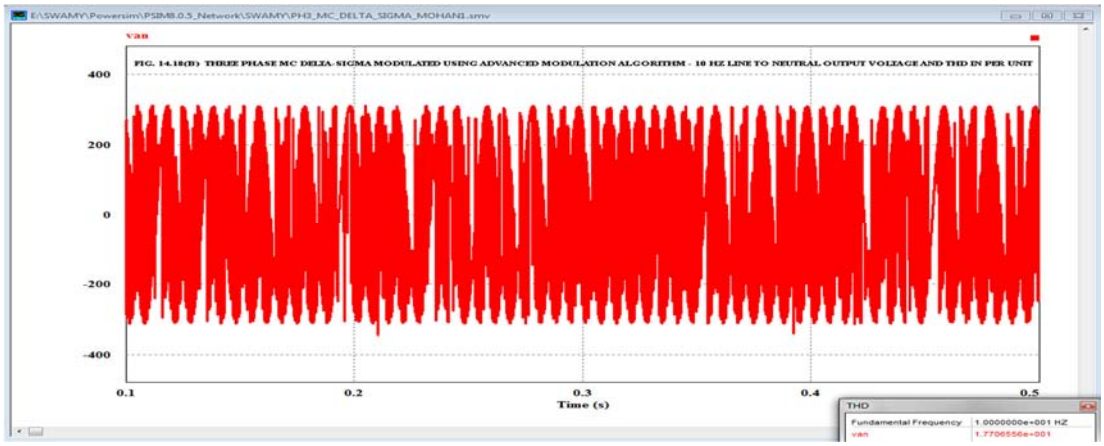

IA_IN
FIG. 14.17(I) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - FFT OF 50 HZ PHASE A INPUT CURRENT
Frequency (Hz)
Measure

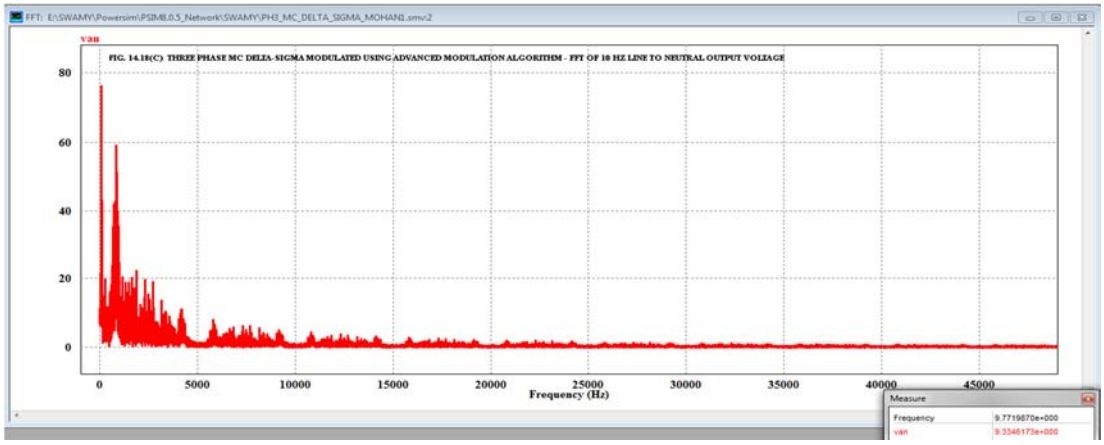

ia
ib
ic
FIG. 14.17(J) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - THREE PHASE 50 HZ LOAD CURRENT
Time (s)
RMS Value

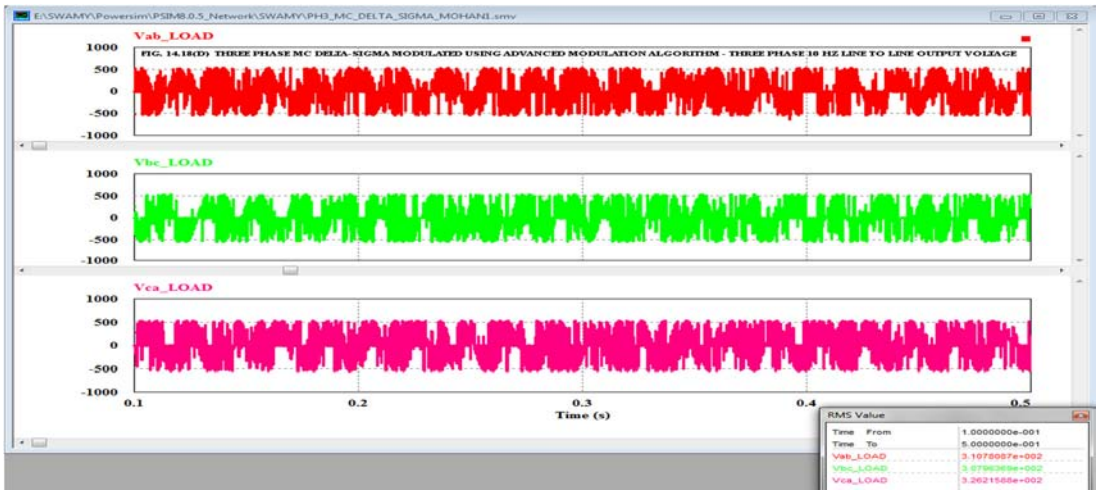

ia
FIG. 14.17(K) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - 50 HZ LOAD CURRENT AND THD IN PER UNIT
Time (s)
THD

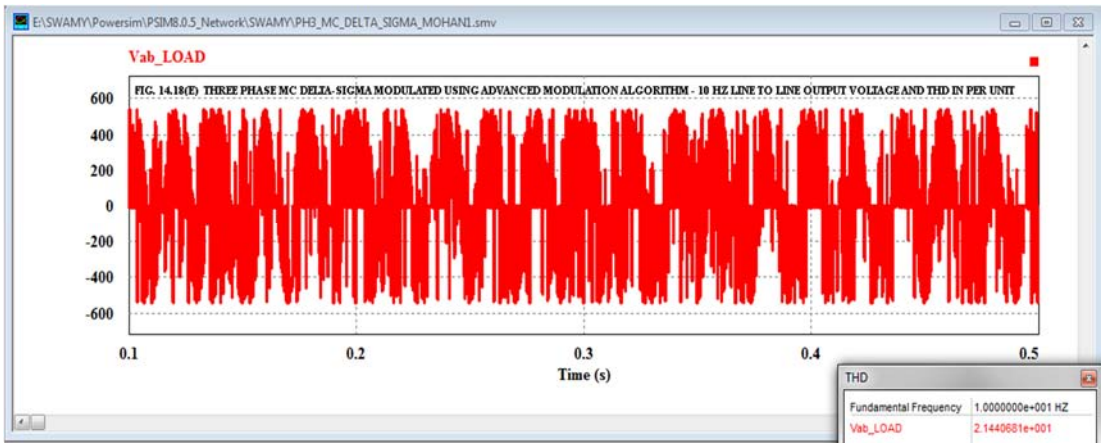

ia
FIG. 14.17(L) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - FFT OF 50 HZ LOAD CURRENT
Frequency (Hz)
Measure

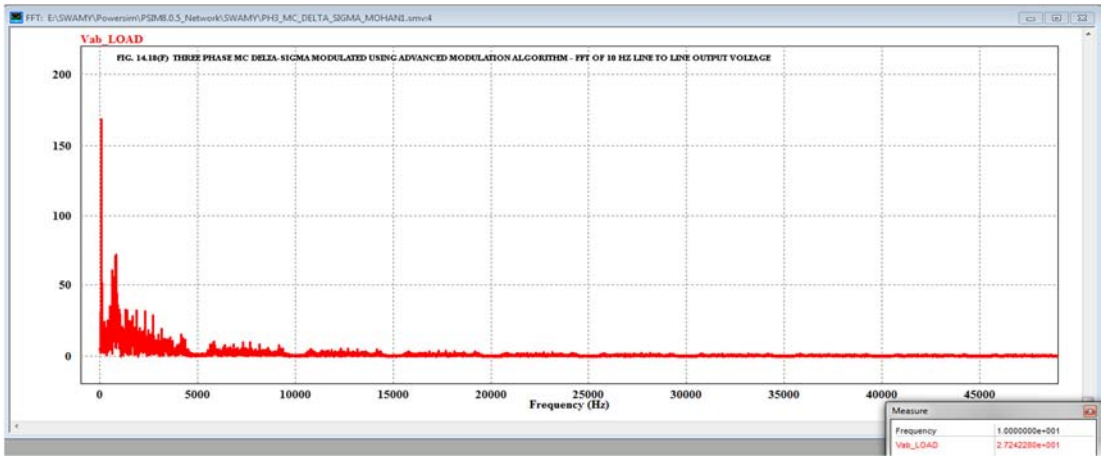

van
FIG. 14.18(A) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - THREE PHASE 10 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
vbn
vcn
Time (s)
RMS Value

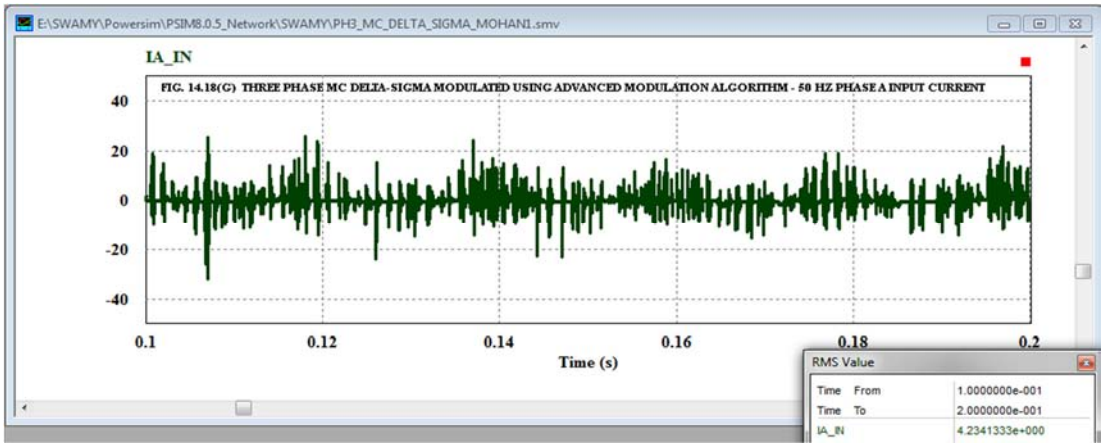

van
FIG. 14.18(B) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - 10 HZ LINE TO NEUTRAL OUTPUT VOLTAGE AND THD IN PER UNIT
Time (s)
THD

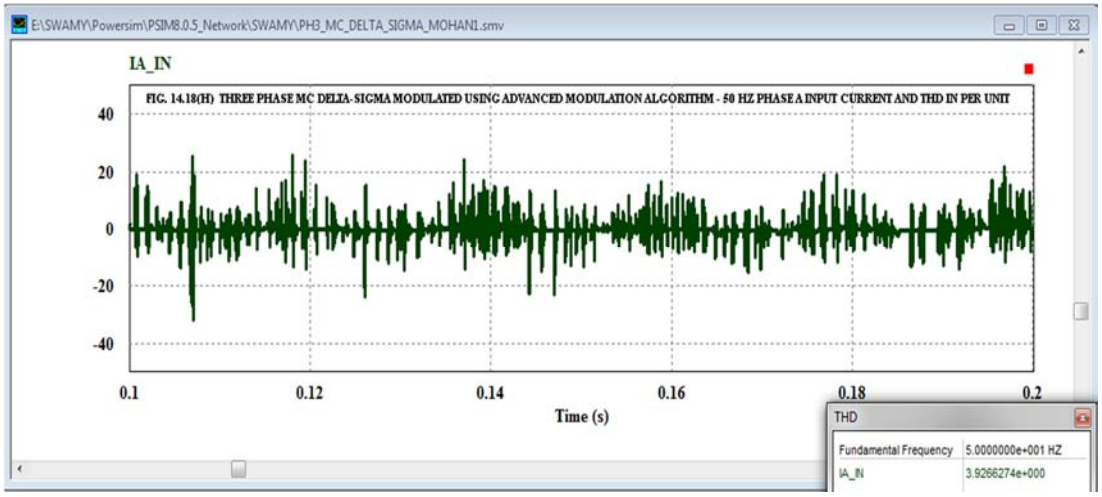

van
FIG. 14.18(C) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - FFT OF 10 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
Frequency (Hz)
Measure

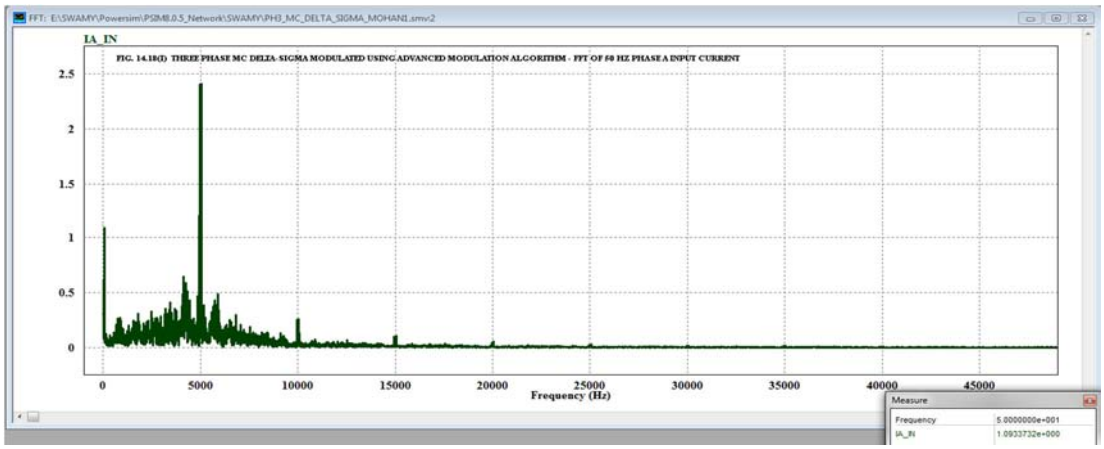

Vab_LOAD
FIG. 14.18(D) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - THREE PHASE 10 HZ LINE TO LINE OUTPUT VOLTAGE
Vbc_LOAD
Vca_LOAD
Time (s)
RMS Value

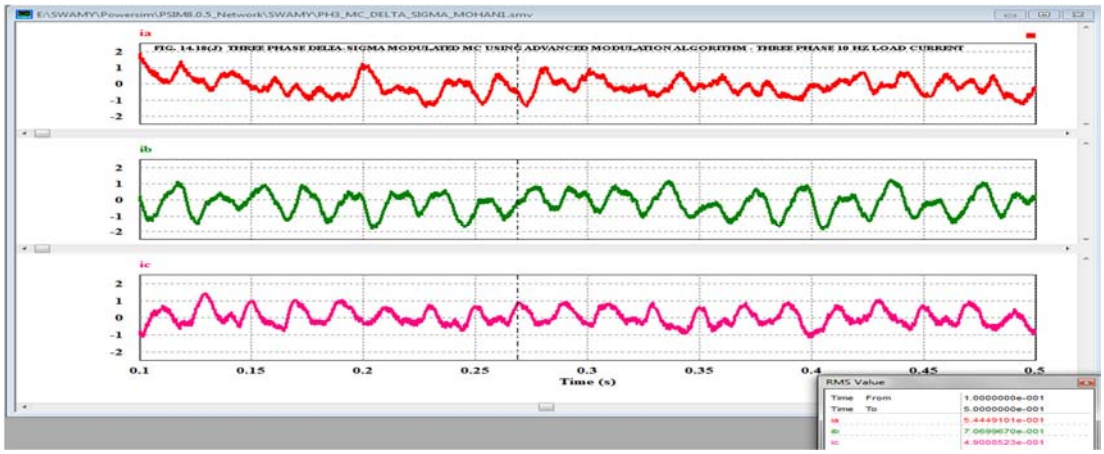

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_DELTA_SIGMA_MOHAN1.smv
Vab_LOAD
FIG. 14.18(E) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - 10 HZ LINE TO LINE OUTPUT VOLTAGE AND THD IN PER UNIT
600
400
200
0
-200
-400
-600
0.1
0.2
0.3
0.4
0.5
Time (s)
THD
Fundamental Frequency
1.0000000e+001 HZ
Vab_LOAD
2.1440681e+001

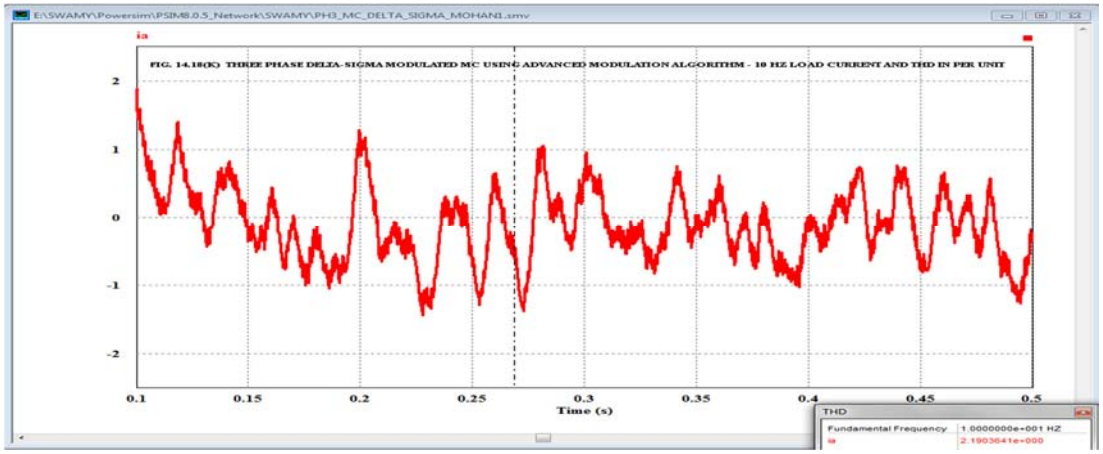

Vab_LOAD
FIG. 14.18(F) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - FFT OF 10 HZ LINE TO LINE OUTPUT VOLTAGE
200
150
100
50
0
0
5000
10000
15000
20000
25000
30000
35000
40000
45000
Frequency (Hz)
Measure

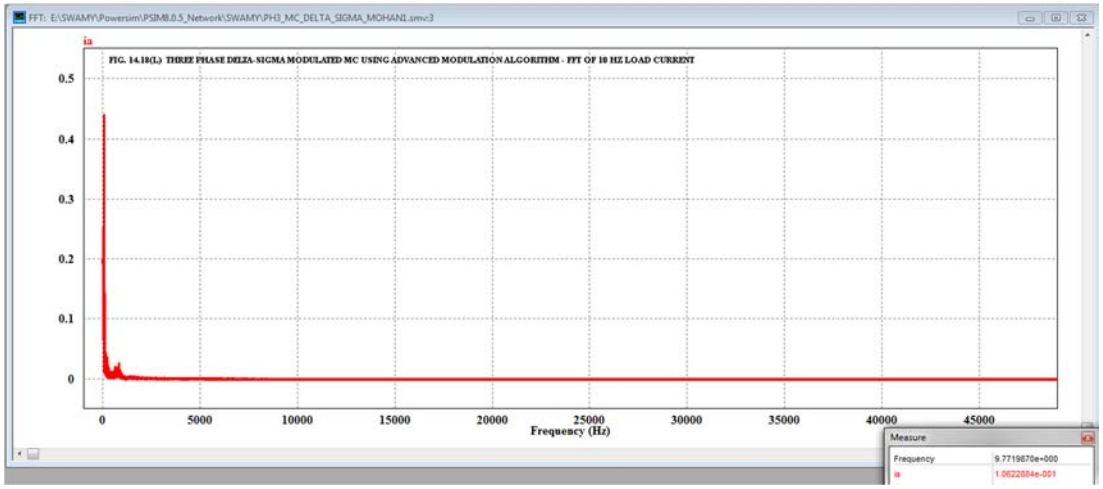

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_DELTA_SIGMA_MOHAN1.smv
IA_IN
FIG. 14.18(G) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - 50 HZ PHASE A INPUT CURRENT
40
20
0
-20
-40
0.1
0.12
0.14
0.16
0.18
0.2
Time (s)
RMS Value
Time From
1.0000000e-001
Time To
2.0000000e-001
IA_IN
4.2341333e+000


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_DELTA_SIGMA_MOHAN1.smv
IA_IN
FIG. 14.18(H) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - 50 HZ PHASE A INPUT CURRENT AND THD IN PER UNIT
40
20
0
-20
-40
0.1
0.12
0.14
0.16
0.18
0.2
Time (s)
THD
Fundamental Frequency
5.0000000e+001 HZ
IA_IN
3.9266274e+000


IA_IN
FIG. 14.18(I) THREE PHASE MC DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM - FFT OF 50 HZ PHASE A INPUT CURRENT
Frequency (Hz)
Measure


ia
ib
ic
FIG. 14.18(J) THREE PHASE DELTA-SIGMA MODULATED MC USING ADVANCED MODULATION ALGORITHM - THREE PHASE 10 HZ LOAD CURRENT
Time (s)
RMS Value


ia
FIG. 14.18(K) THREE PHASE DELTA-SIGMA MODULATED MC USING ADVANCED MODULATION ALGORITHM - 10 HZ LOAD CURRENT AND THD IN PER UNIT
Time (s)
THD
Fundamental Frequency


ia
FIG. 14.18(L) THREE PHASE DELTA-SIGMA MODULATED MC USING ADVANCED MODULATION ALGORITHM - FFT OF 10 HZ LOAD CURRENT
Frequency (Hz)
Measure

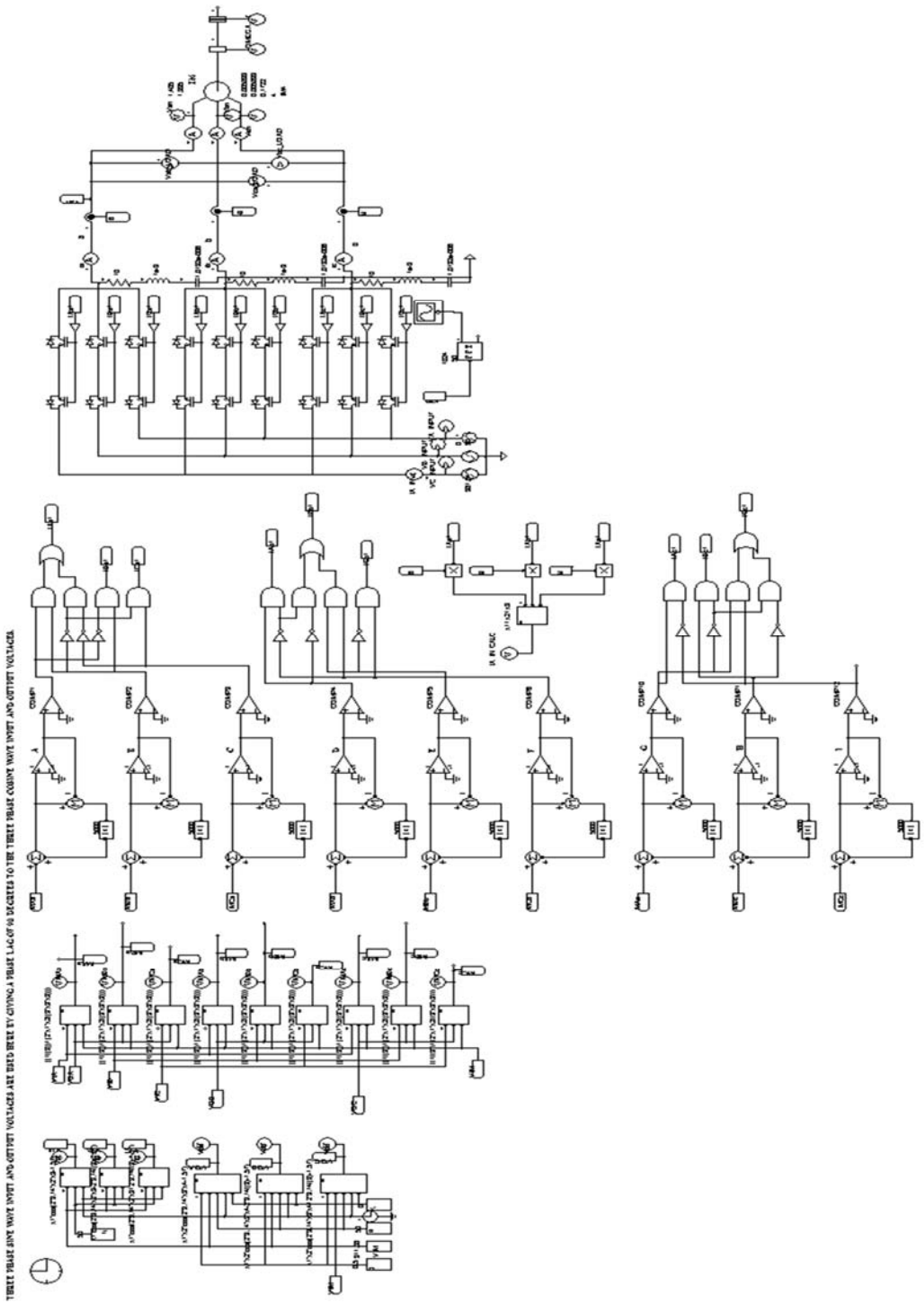
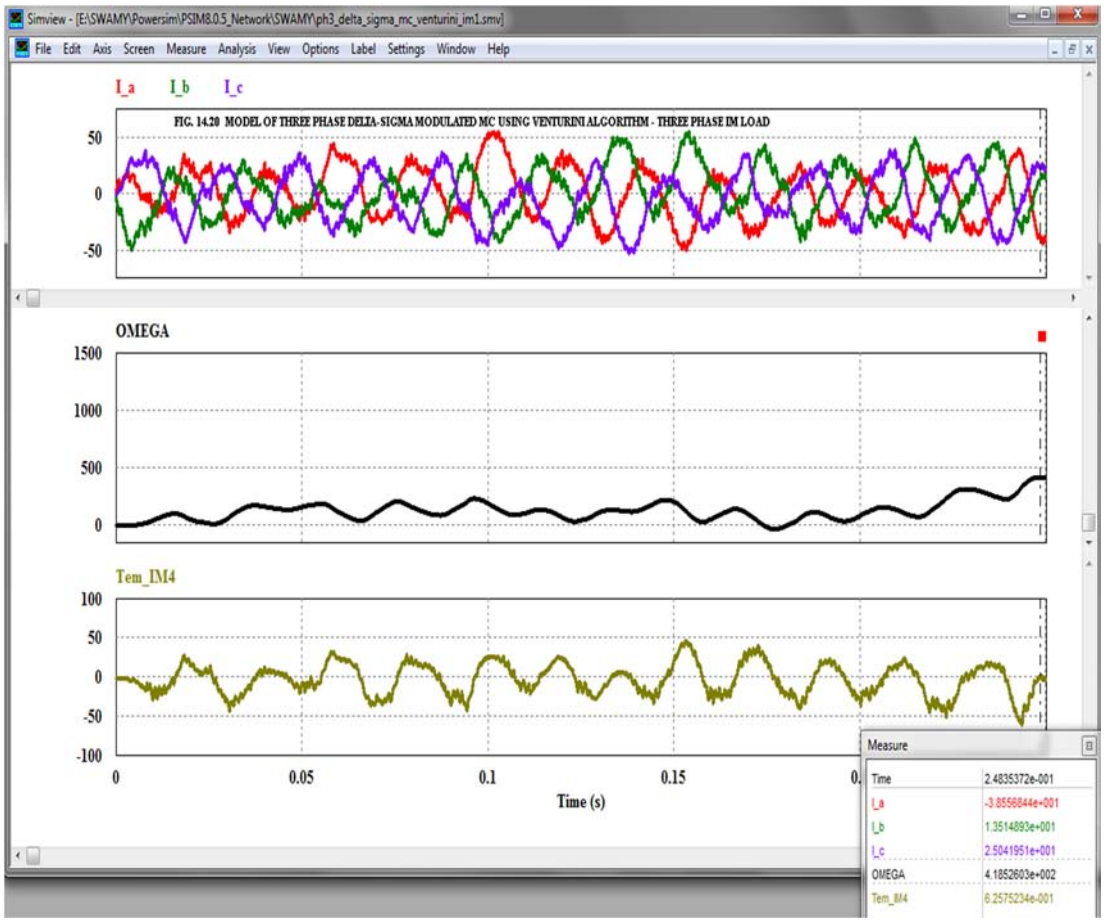
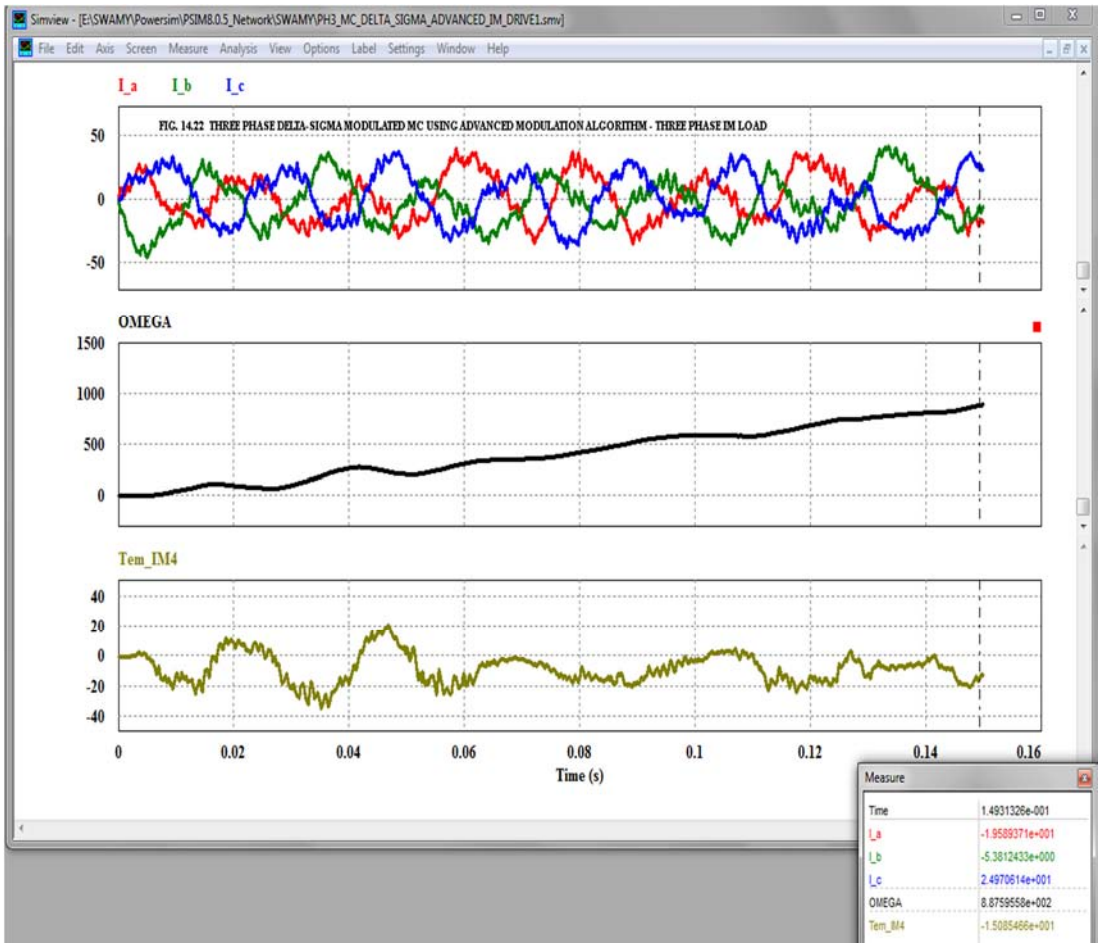


FIG. 14.19 MODEL OF THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MC - DELTA-SIGMA MODULATED USING VENTURINI ALGORITHM DRIVING A THREE PHASE IM LOAD


Simview - [E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\ph3_delta_sigma_mc_venturini_im1.smv]
File Edit Axis Screen Measure Analysis View Options Label Settings Window Help
I_a I_b I_c
FIG. 14.20 MODEL OF THREE PHASE DELTA-SIGMA MODULATED MC USING VENTURINI ALGORITHM - THREE PHASE IM LOAD
50
0
-50
OMEGA
1500
1000
500
0
Tem_IM4
100
50
0
-50
-100
0
0.05
0.1
0.15
Time (s)
Measure
Time 2.4835372e-001
I_a -3.8556844e+001
I_b 1.3514893e+001
I_c 2.5041951e+001
OMEGA 4.1852603e+002
Tem_IM4 6.2575234e-001


Simview - [E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_DELTA_SIGMA_ADVANCED_IM_DRIVE1.smv]
File Edit Axis Screen Measure Analysis View Options Label Settings Window Help
I_a I_b I_c
FIG. 14.22 THREE PHASE DELTA-SIGMA MODULATED MC USING ADVANCED MODULATION ALGORITHM - THREE PHASE IM LOAD
50
0
-50
OMEGA
1500
1000
500
0
Tem_IM4
40
20
0
-20
-40
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0.16
Time (s)
Measure
Time 1.4931326e-001
I_a -1.9589371e+001
I_b -5.3812433e+000
I_c 2.4970614e+001
OMEGA 8.8759558e+002
Tem_IM4 -1.5085466e+001

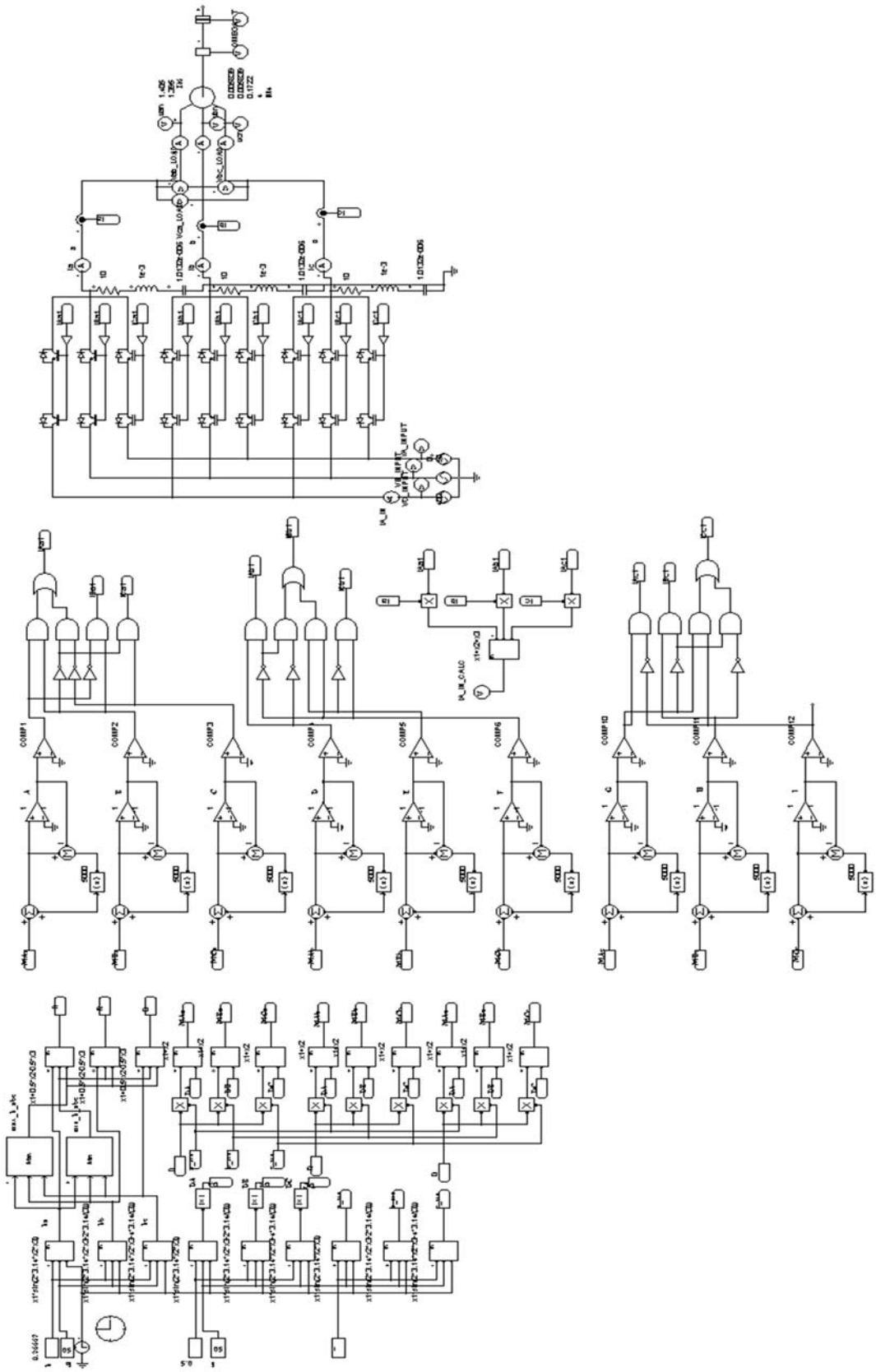


FIG. 14.21 MODEL OF THREE PHASE 50 HZ AC TO THREE PHASE 50 HZ AC MC - DELTA-SIGMA MODULATED USING ADVANCED MODULATION ALGORITHM DRIVING THREE PHASE IM LOAD

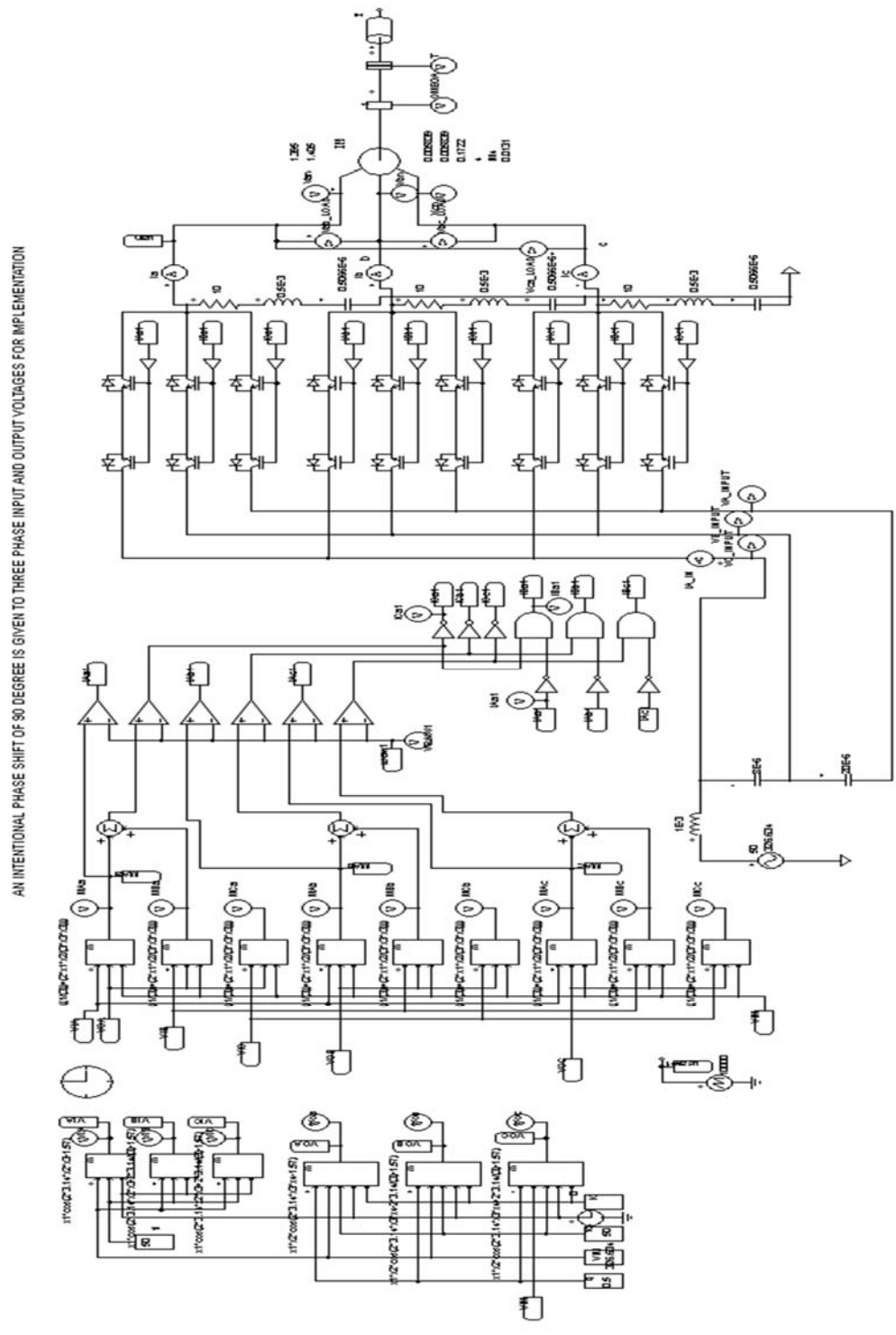
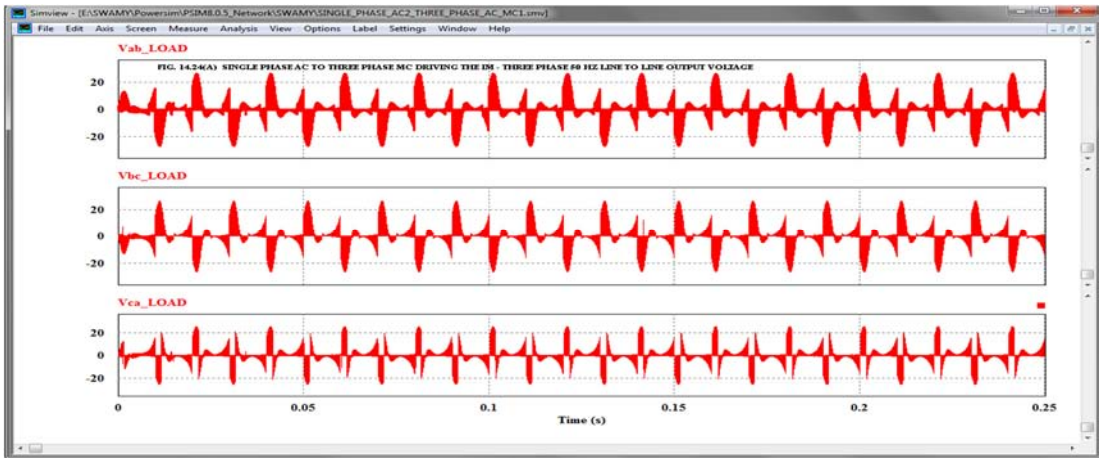
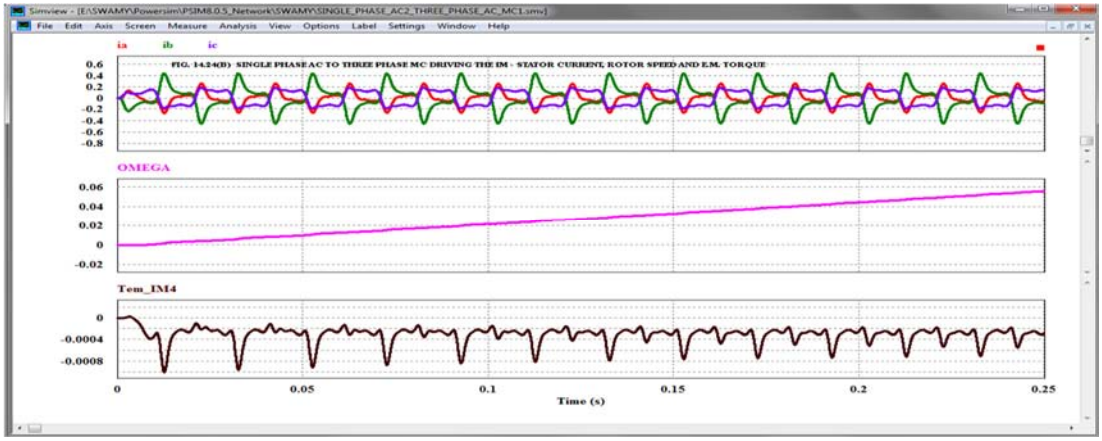
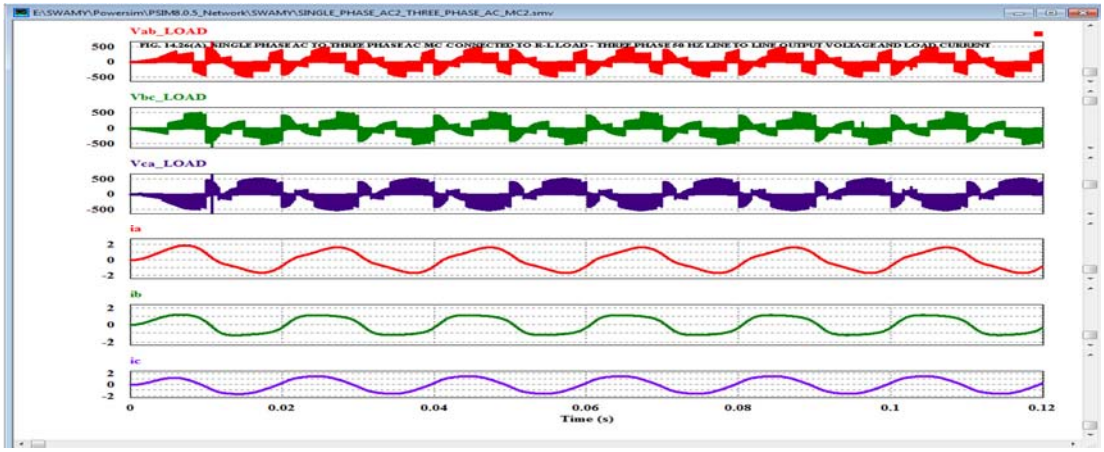
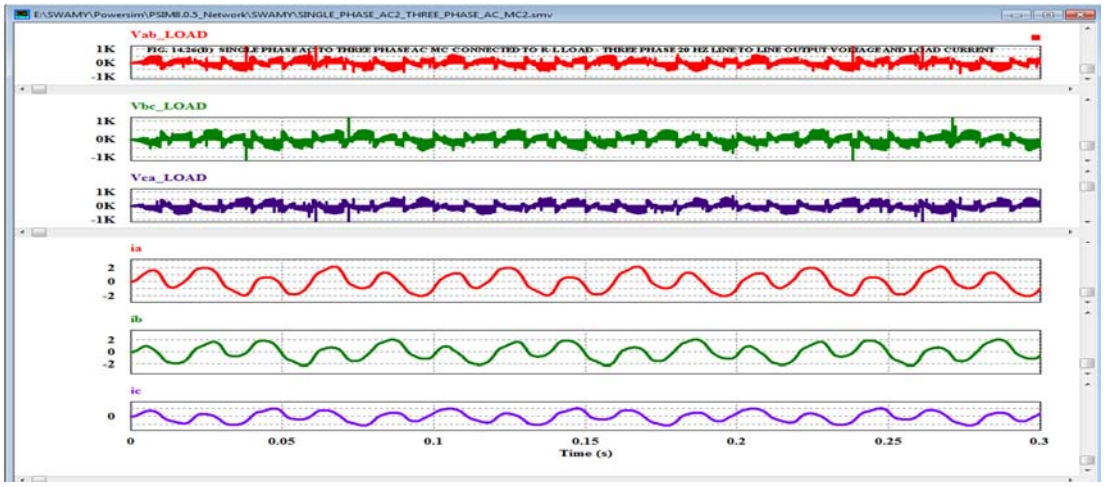


FIG. 14.23 MODEL OF SINGLE PHASE AC TO THREE PHASE AC MC DRIVING THE I.M.


Vab_LOAD
FIG. 14.24(A) SINGLE PHASE AC TO THREE PHASE MC DRIVING THE IM - THREE PHASE 50 HZ LINE TO LINE OUTPUT VOLTAGE
Vbc_LOAD
Vca_LOAD
Time (s)


ia ib ic
FIG. 14.24(B) SINGLE PHASE AC TO THREE PHASE MC DRIVING THE IM - STATOR CURRENT, ROTOR SPEED AND E.M. TORQUE
OMEGA
Tem_IM4
Time (s)


Vab_LOAD
Vbc_LOAD
Vca_LOAD
ia
ib
ic
Time (s)


Vab_LOAD
Vbc_LOAD
Vca_LOAD
ia
ib
ic
Time (s)

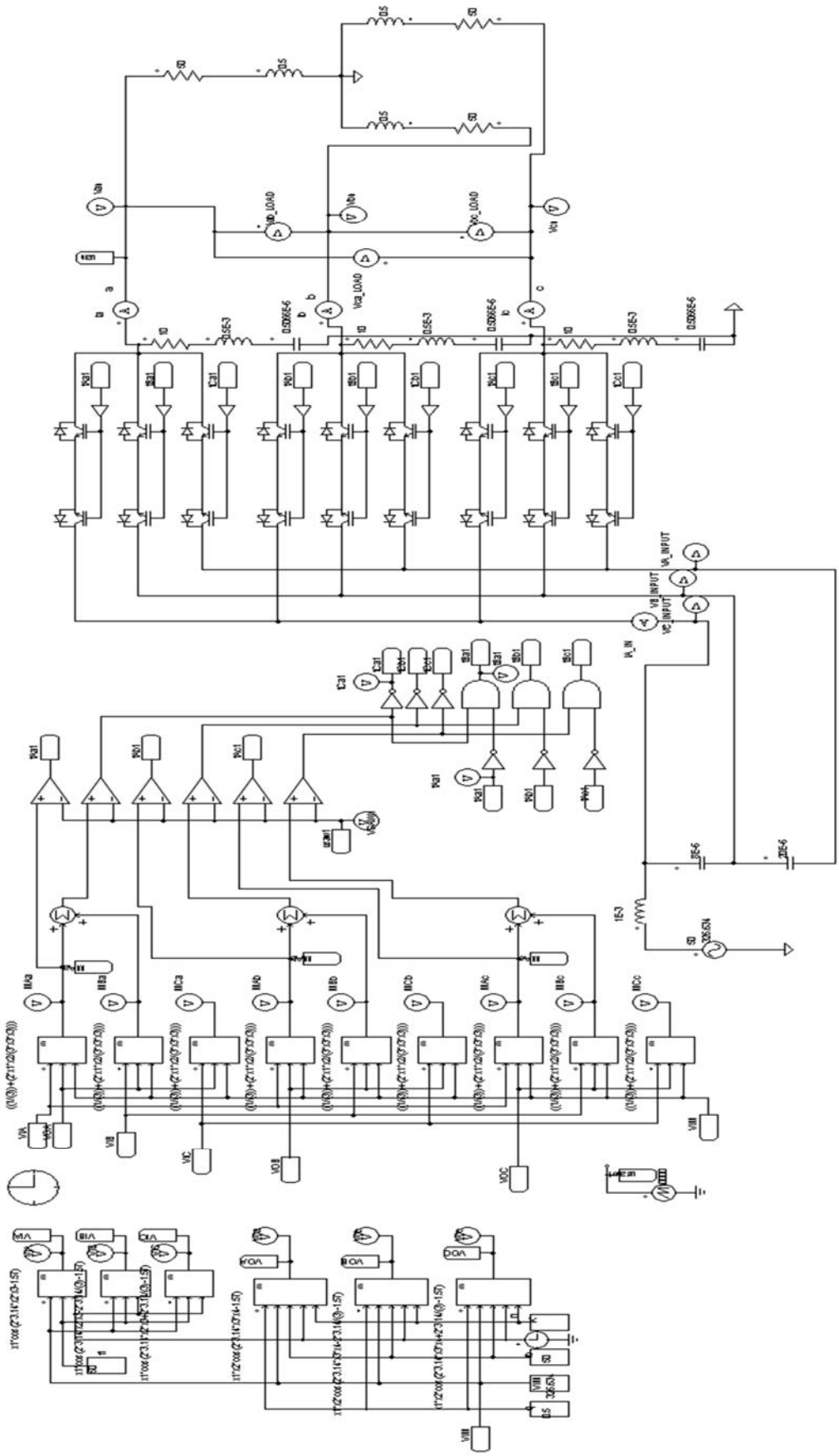


FIG. 14.25 MODEL OF SINGLE PHASE AC TO THREE PHASE AC MC CONNECTED TO R-L LOAD

14.13 INDIRECT SPACE VECTOR MODULATION OF MATRIX CONVERTER: The model of the Indirect Space Vector Modulated (ISVM) MC using SIMULINK is already discussed in Section 9.4 of Chapter IX. The model of the three phase Indirect SVM MC using PSIM9 [52] is reviewed here. The PSIM model of three phase Indirect SVM MC is shown in Fig. 14.33. This model is developed in the same way as discussed in Section 9.3 and 9.4 of Chapter IX. The simulation results for output frequencies of 50 Hz and 20 Hz are shown in Figs. 14.34(A) to 14.34(I) and in Figs. 14.35(A) to 14.35(I) respectively. The simulation results are tabulated in Table 14.12.

TABLE 14.12: PH3 ISVM MC – PSIM Simulation Results

Sl.No.	Three Phase Indirect SVM MC Input – Output Frequency Hz	THD of Line to Line Output Voltage p.u.	THD Of Line to Neutral Output Voltage p.u.	THD of Load Current p.u
1)	50 – 50	1.0814	1.5897	0.3738
2)	50 – 20	1.0435	1.7125	0.3554

14.14 DISCUSSION OF RESULTS: In this section the SIMULINK model performance for the respective category of the MC is compared with the relevant performance obtained by either PSCAD or PSIM presented in this chapter. The percentage error is calculated on the basis of SIMULINK model performance in the format given below:

$$Percentage\,Error \quad = \quad \frac{(SIMULINKModelResult - PSCAD/PSIMModelResult)*100}{SIMULINKModelResult}$$

Venturini algorithm assuming unity input power factor gives a percentage error of 3.94, -3.7 and 16.78 for the line to neutral output voltage, line to line output voltage and input current respectively. Sunter-Clare algorithm for MC gives a percentage error of -29.27, 15.5 and -28.61 for the line to neutral , line to line output voltages and input current respectively. Ned Mohan algorithm for MC gives a percentage error of -18.42, -11.32 and 30.47 for the line to neutral, line to line and input current respectively.

The simulation of three phase Multilevel MC (MMC) with three Flying capacitors (FC) per output phase is first carried out by SIMULINK and then this is also done by PSCAD and PSIM. Comparing the simulation using SIMULINK with PSIM, the percentage errors are -11.6, -29.2 and 76.21 for the line to neutral, line to line output voltages and input current respectively. The simulation of three phase MMC with six FC per output phase is carried out using PSCAD and PSIM only and hence the percentage error is NOT calculated.

The simulation of three phase Direct ASVM MC for an input and output frequency of 50 Hz respectively gives percentage error of 29.36, 29.89 and 37.79 for the line to neutral, line to line output voltages and load current respectively. For this Direct ASVM MC, the percentage error in the above order for an input and output frequency of 50 Hz and 20 Hz are -41.77, 0.6172 and 12.99 respectively. The simulation results for the Direct SSVM MC for an input and output frequency of 50 Hz respectively gives percentage error of 5.4, 15.58 and 10.59 in the above order. For this Direct SSVM MC the percentage error in the above order for an input and output frequency of 50 Hz and 20 Hz are

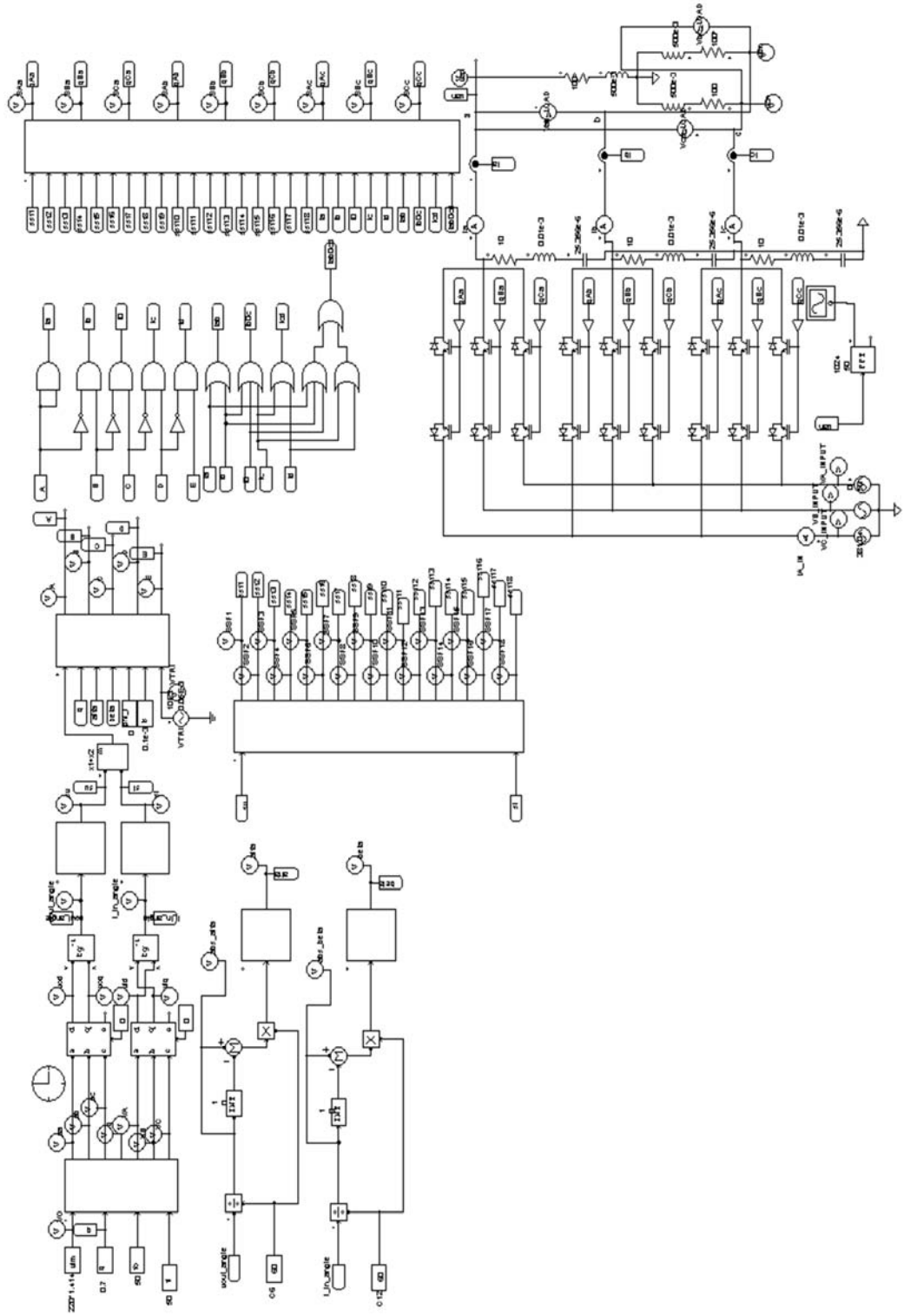


FIG. 14.27 MODEL OF DIRECT ASVM THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER

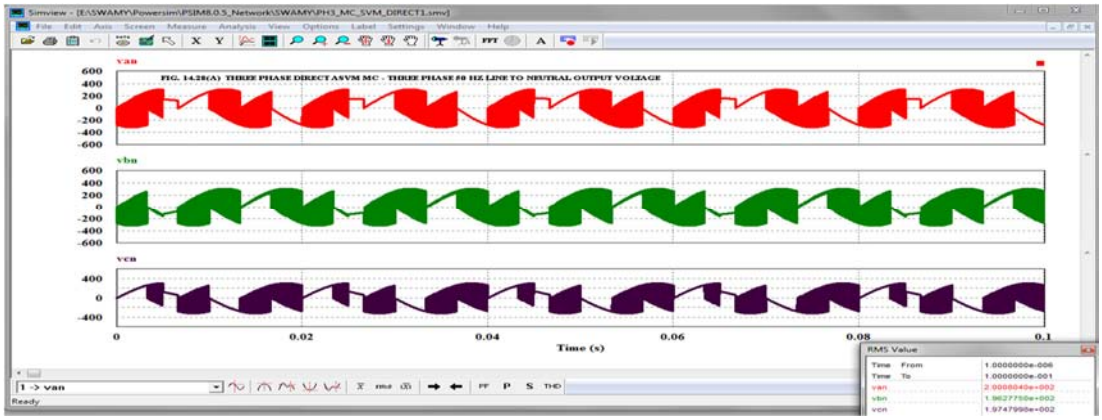


FIG. 14.28(A) THREE PHASE DIRECT ASVM MC - THREE PHASE 50 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
van
vbn
vcn
Time (s)
RMS Value


FIG. 14.28(B) THREE PHASE DIRECT ASVM MC - 50 HZ LINE TO NEUTRAL OUTPUT VOLTAGE AND THD IN PER UNIT
van
Time (s)
THD
Fundamental Frequency

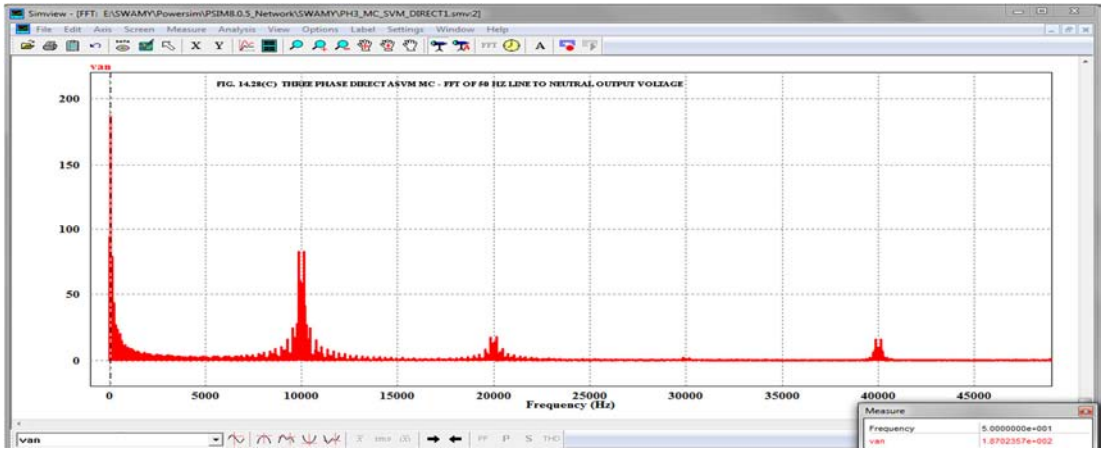
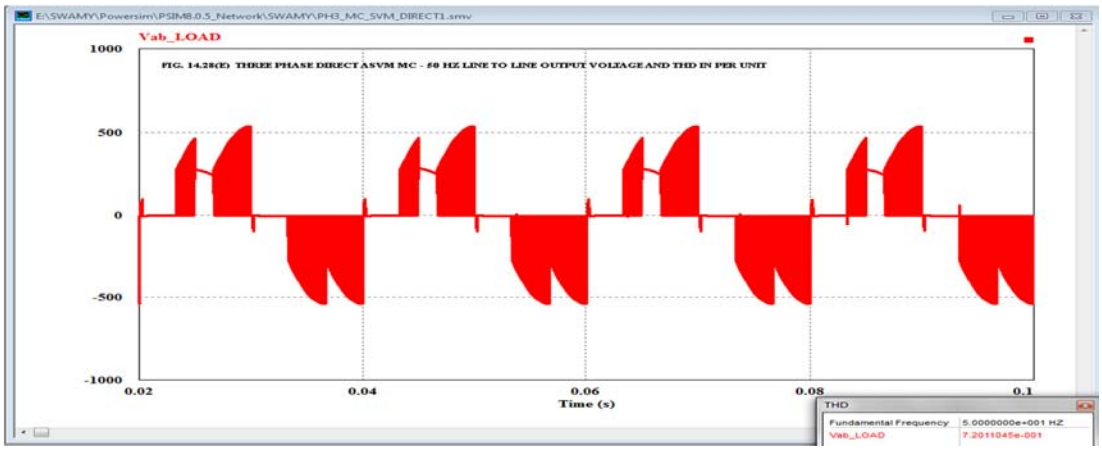
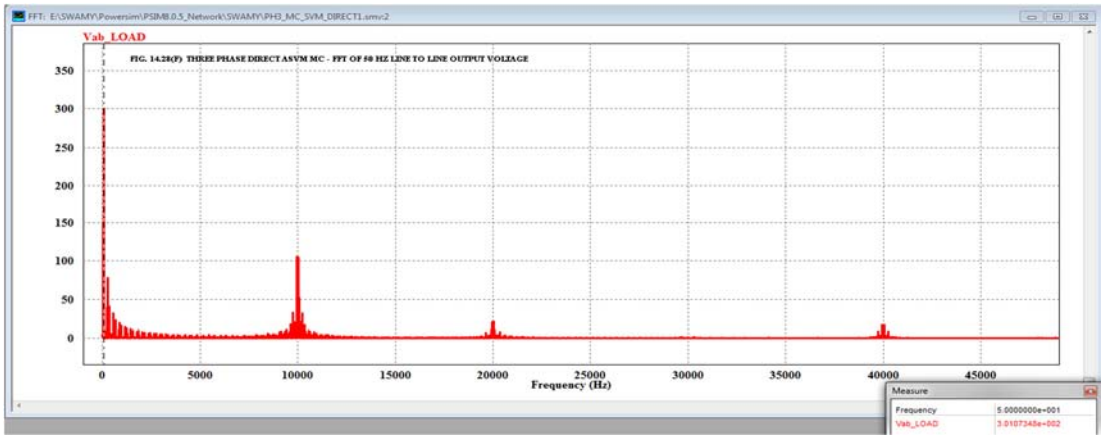
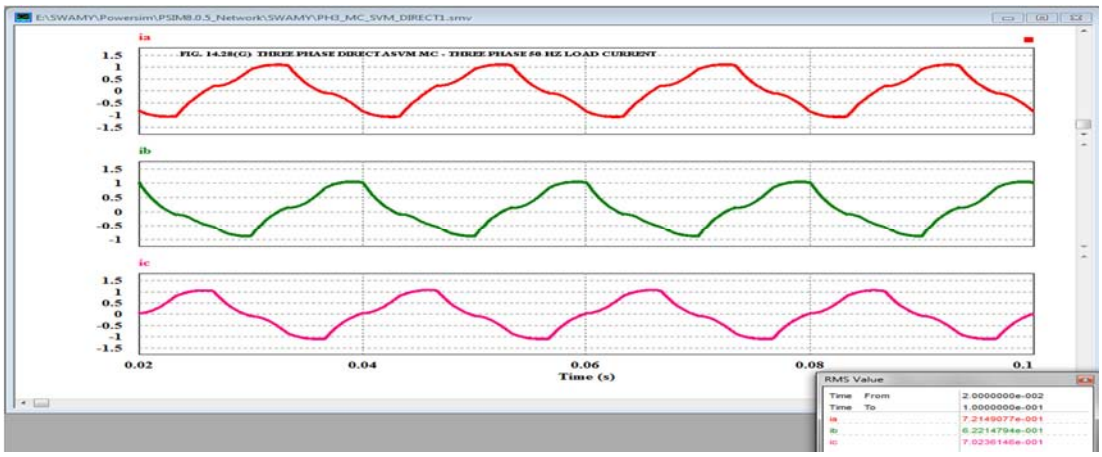


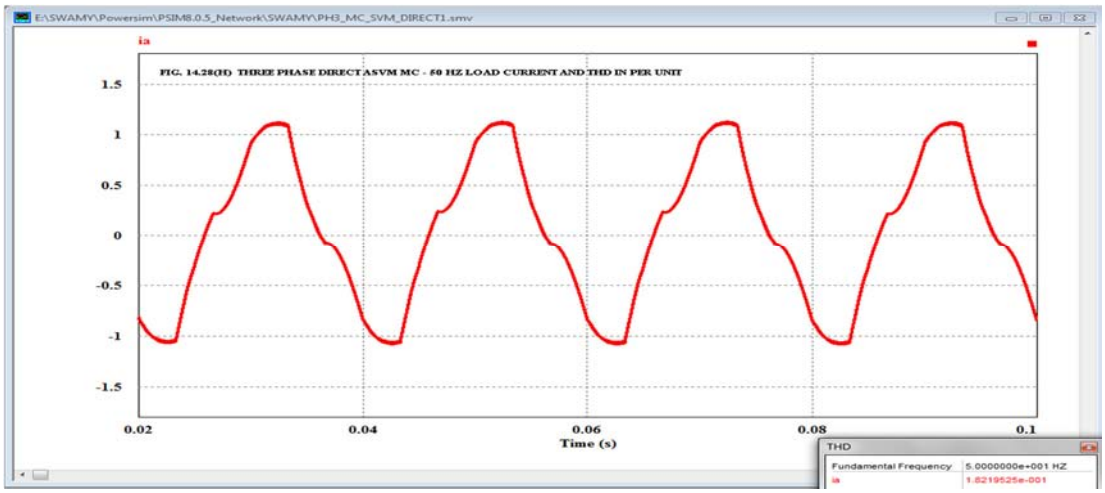
FIG. 14.28(C) THREE PHASE DIRECT ASVM MC - FFT OF 50 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
van
Frequency (Hz)
Measure


FIG. 14.28(D) THREE PHASE DIRECT ASVM MC - THREE PHASE 50 HZ LINE TO LINE OUTPUT VOLTAGE
Vab_LOAD
Vbc_LOAD
Vca_LOAD
Time (s)
RMS Value


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_SVM_DIRECT1.smv
Vab_LOAD
FIG. 14.28(E) THREE PHASE DIRECT ASVM MC - 50 HZ LINE TO LINE OUTPUT VOLTAGE AND THD IN PER UNIT
1000
500
0
-500
-1000
0.02
0.04
0.06
0.08
0.1
Time (s)
THD
Fundamental Frequency
5.0000000e+001 HZ
Vab_LOAD
7.2011045e-001


FFT: E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_SVM_DIRECT1.smv2
Vab_LOAD
FIG. 14.28(F) THREE PHASE DIRECT ASVM MC - FFT OF 50 HZ LINE TO LINE OUTPUT VOLTAGE
350
300
250
200
150
100
50
0
0
5000
10000
15000
20000
25000
30000
35000
40000
45000
Frequency (Hz)
Measure
Frequency
5.0000000e+001
Vab_LOAD
3.0107348e+002


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_SVM_DIRECT1.smv
ia
FIG. 14.28(G) THREE PHASE DIRECT ASVM MC - THREE PHASE 50 HZ LOAD CURRENT
ib
ic
1.5
1
0.5
0
-0.5
-1
-1.5
0.02
0.04
0.06
0.08
0.1
Time (s)
RMS Value
Time From
2.0000000e-002
Time To
1.0000000e-001
7.2149077e-001
6.2214794e-001
7.0236146e-001


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_SVM_DIRECT1.smv
ia
FIG. 14.28(H) THREE PHASE DIRECT ASVM MC - 50 HZ LOAD CURRENT AND THD IN PER UNIT
1.5
1
0.5
0
-0.5
-1
-1.5
0.02
0.04
0.06
0.08
0.1
Time (s)
THD
Fundamental Frequency
5.0000000e+001 HZ
ia
1.8219525e-001

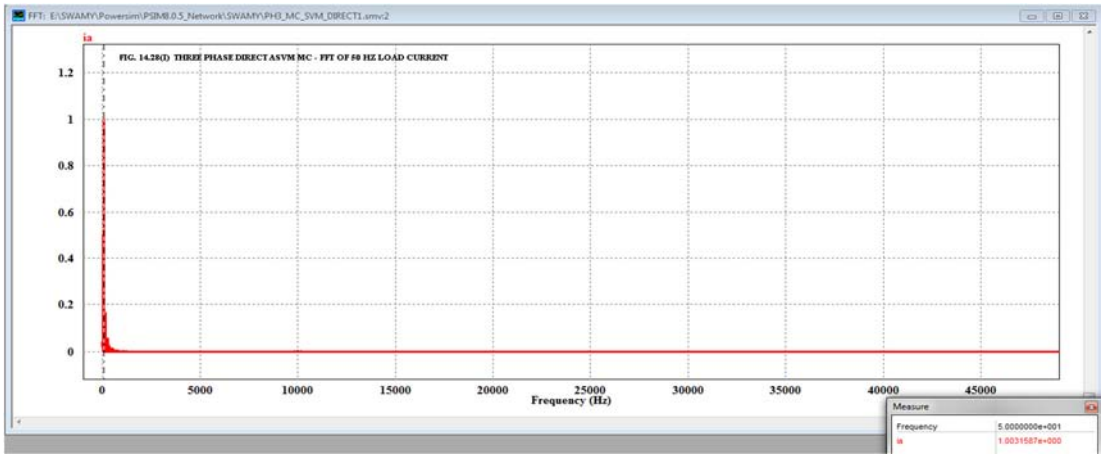


FIG. 14.28(I) THREE PHASE DIRECT ASVM MC - FFT OF 50 HZ LOAD CURRENT
ia
Frequency (Hz)
Measure

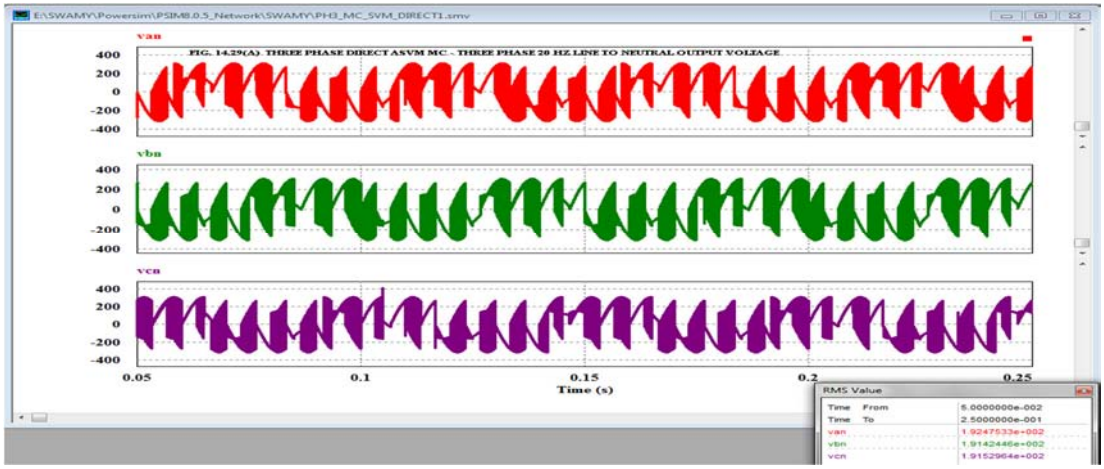


FIG. 14.29(A) THREE PHASE DIRECT ASVM MC - THREE PHASE 20 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
van
vbn
vcn
Time (s)
RMS Value

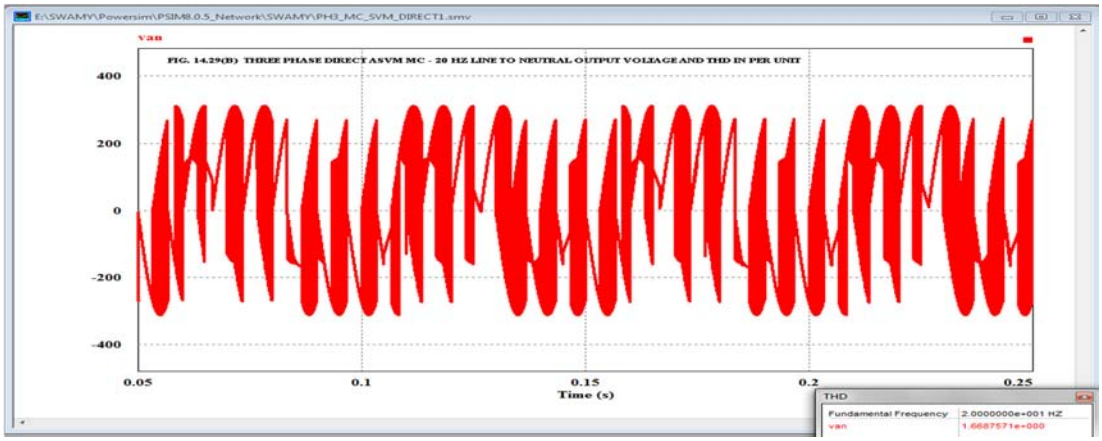


FIG. 14.29(B) THREE PHASE DIRECT ASVM MC - 20 HZ LINE TO NEUTRAL OUTPUT VOLTAGE AND THD IN PER UNIT
van
Time (s)
THD

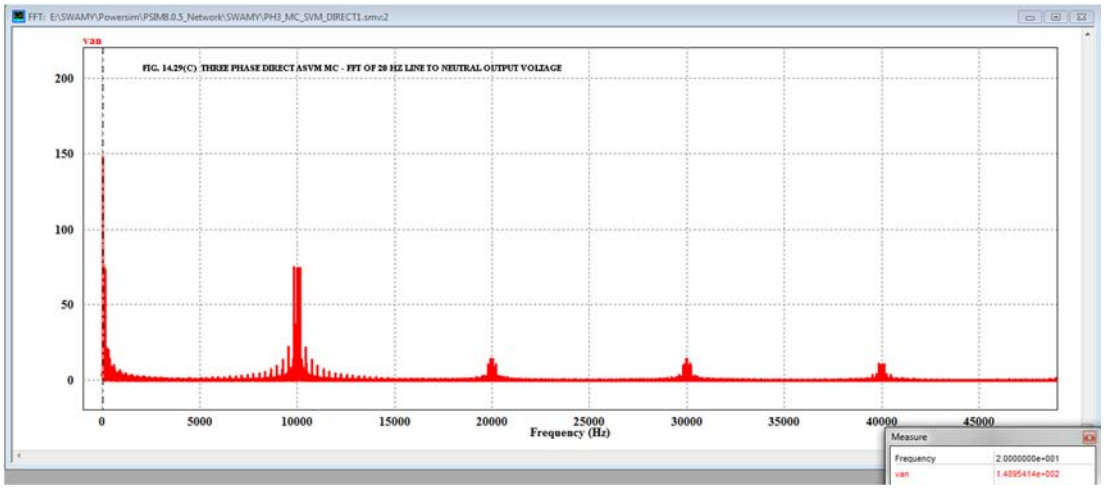
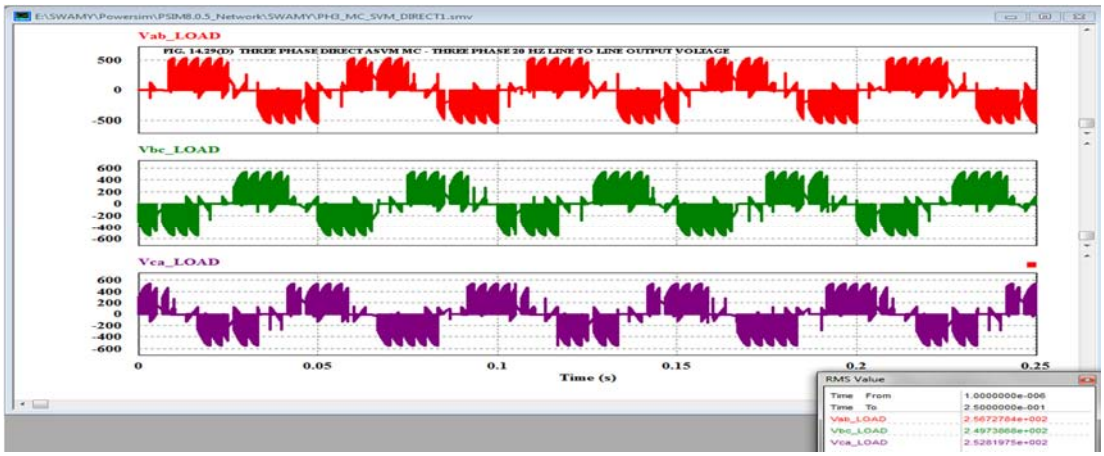
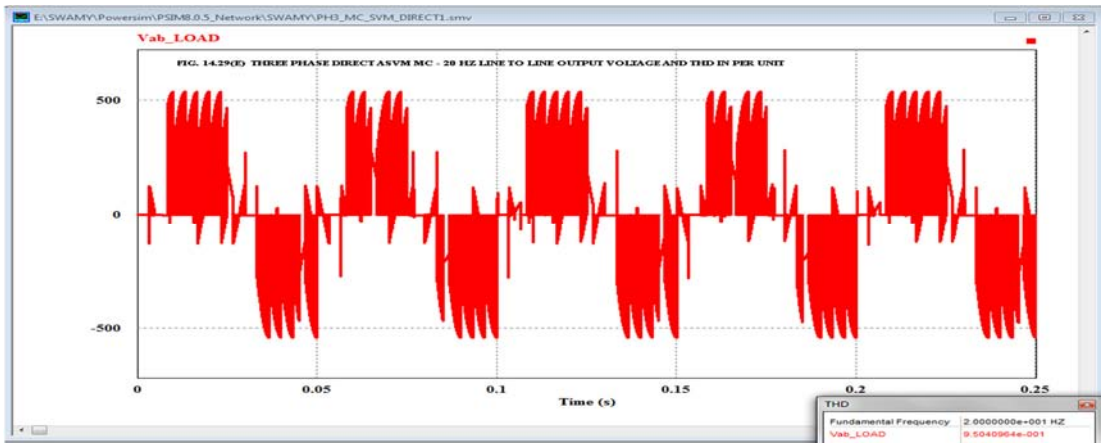
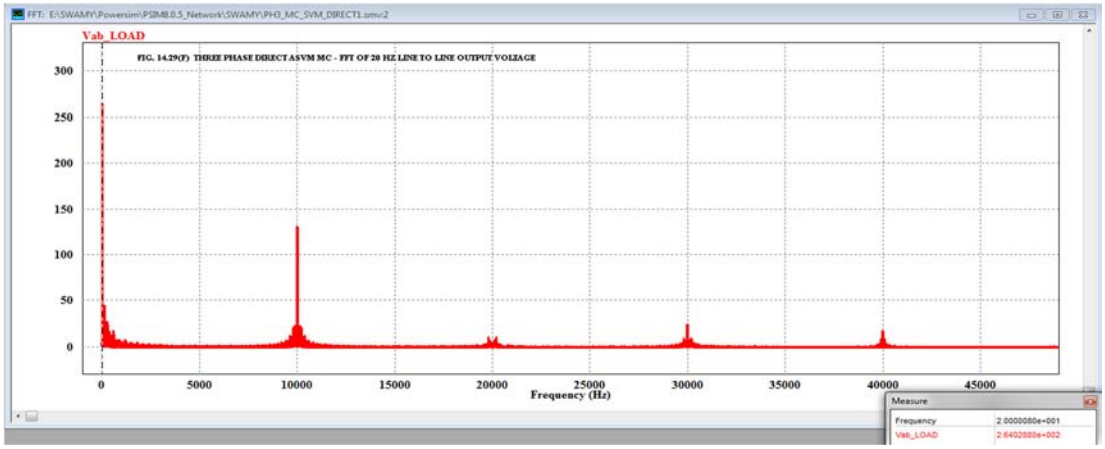
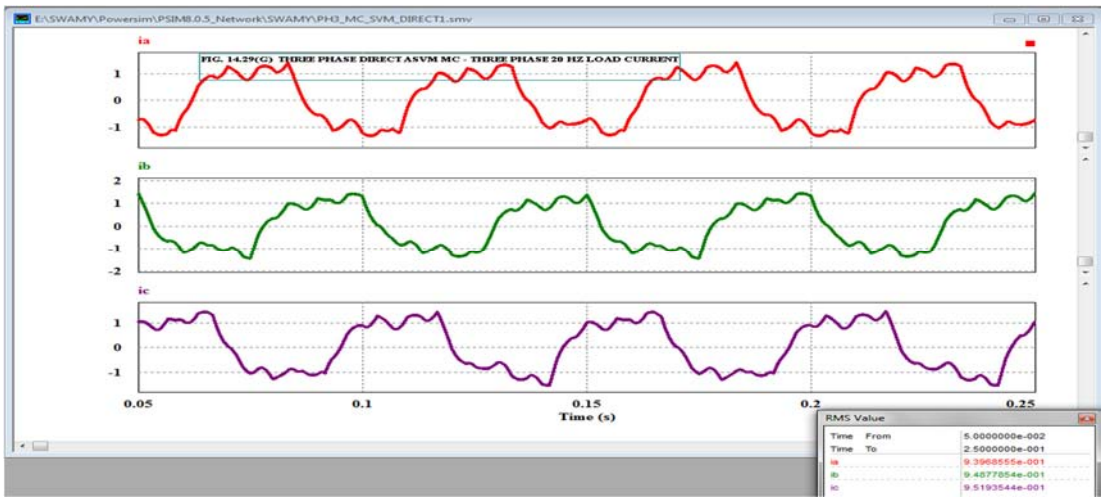


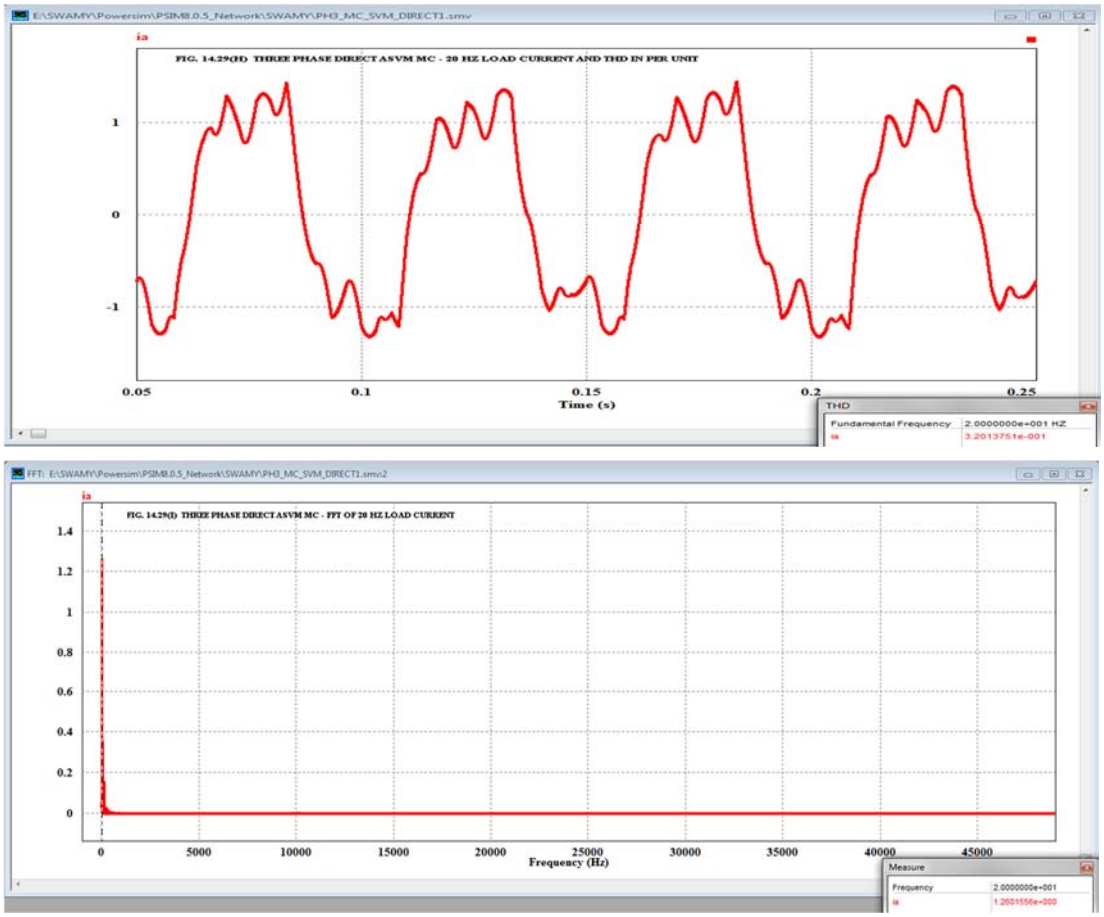
FIG. 14.29(C) THREE PHASE DIRECT ASVM MC - FFT OF 20 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
van
Frequency (Hz)
Measure


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_SVM_DIRECT1.smv
Vab_LOAD
FIG. 14.29(D) THREE PHASE DIRECT ASVM MC - THREE PHASE 20 HZ LINE TO LINE OUTPUT VOLTAGE
500
0
-500
Vbc_LOAD
600
400
200
0
-200
-400
-600
Vca_LOAD
600
400
200
0
-200
-400
-600
0
0.05
0.1
0.15
0.2
0.25
Time (s)
RMS Value
Time From 1.0000000e-006
Time To 2.5000000e-001
Vab_LOAD 2.5672784e+002
Vbc_LOAD 2.4973868e+002
Vca_LOAD 2.5281975e+002


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_SVM_DIRECT1.smv
Vab_LOAD
FIG. 14.29(E) THREE PHASE DIRECT ASVM MC - 20 HZ LINE TO LINE OUTPUT VOLTAGE AND THD IN PER UNIT
500
0
-500
0
0.05
0.1
0.15
0.2
0.25
Time (s)
THD
Fundamental Frequency 2.0000000e+001 HZ
Vab_LOAD 9.5040964e-001


FFT: E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_SVM_DIRECT1.smv:2
Vab_LOAD
FIG. 14.29(F) THREE PHASE DIRECT ASVM MC - FFT OF 20 HZ LINE TO LINE OUTPUT VOLTAGE
300
250
200
150
100
50
0
0
5000
10000
15000
20000
25000
30000
35000
40000
45000
Frequency (Hz)
Measure
Frequency 2.0000000e+001
Vab_LOAD 2.6402880e+002


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_SVM_DIRECT1.smv
ia
FIG. 14.29(G) THREE PHASE DIRECT ASVM MC - THREE PHASE 20 HZ LOAD CURRENT
1
0
-1
ib
2
1
0
-1
-2
ic
1
0
-1
0.05
0.1
0.15
0.2
0.25
Time (s)
RMS Value
Time From 5.0000000e-002
Time To 2.5000000e-001
ia 9.3968555e-001
ib 9.4877854e-001
ic 9.5193544e-001



-36.64, -3.047 and -8.30 respectively.

The simulation of the three phase Indirect SVM of MC for an input and output frequency of 50 Hz gives percentage error of 24.68, 13.88 and 24.04 for the line to neutral, line to line output voltages and load current respectively. For this three phase Indirect SVM MC the values of percentage error for an input and output frequency of 50 Hz and 20 Hz in the above order are -3.39, 12.89 and -30.04 respectively.

The simulation results of the Dual Programmable AC to DC rectifier shown in Table 10.3 of Chapter X closely well agree with the simulation results using PSCAD shown in Table 14.7 above and the discrepancy is negligible. This confirms the success of the discovery of the Dual Programmable AC to DC rectifier using three phase AC to three phase AC MC topology.

The simulation results for the three phase Delta-Sigma modulated MC using Venturini algorithm shows that for an input and output frequency of both 50 Hz, the percentage error for the line to neutral, line to line output voltages, input current and load current are -43.15, -26.56, -444.40 and -239.39 respectively. For the above delta-sigma modulated MC with an input and output frequency of 50 Hz and 20 Hz, the percentage error in the above order are 30.08, 31.87, -497.33 and -520.93 respectively. The simulation results for the three phase Delta-Sigma modulated MC using Ned Mohan algorithm shows that for an input and output frequency of both 50 Hz, the percentage error for

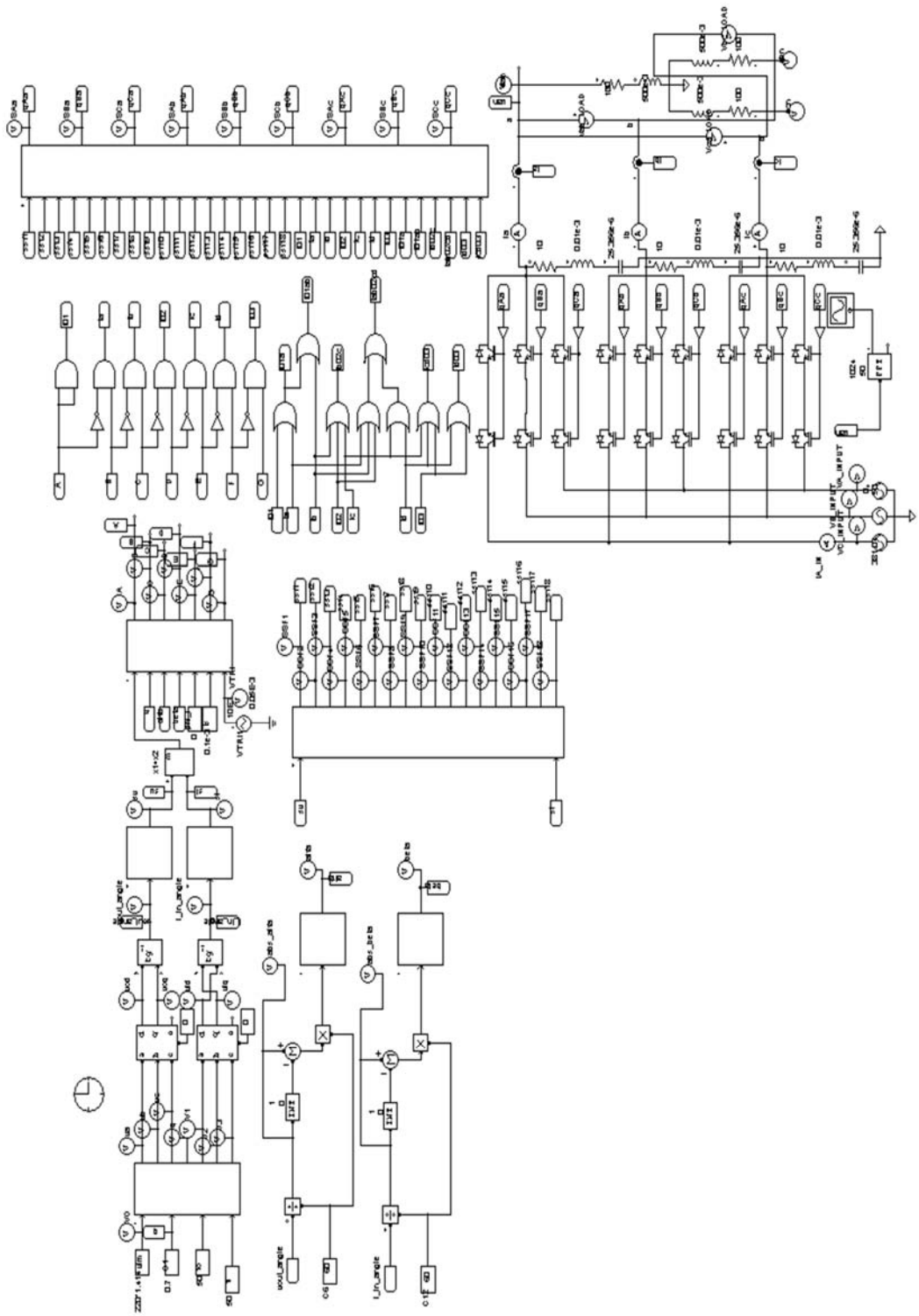
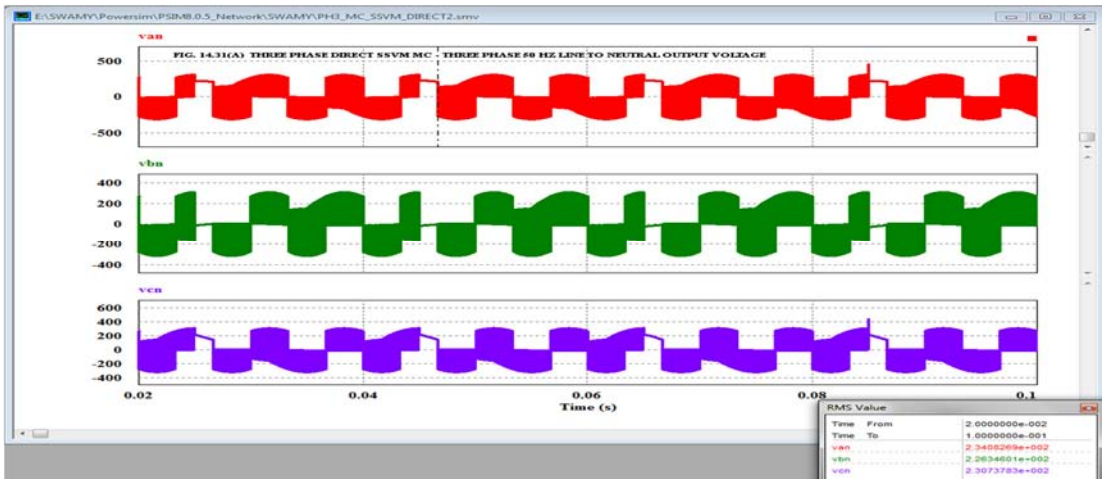
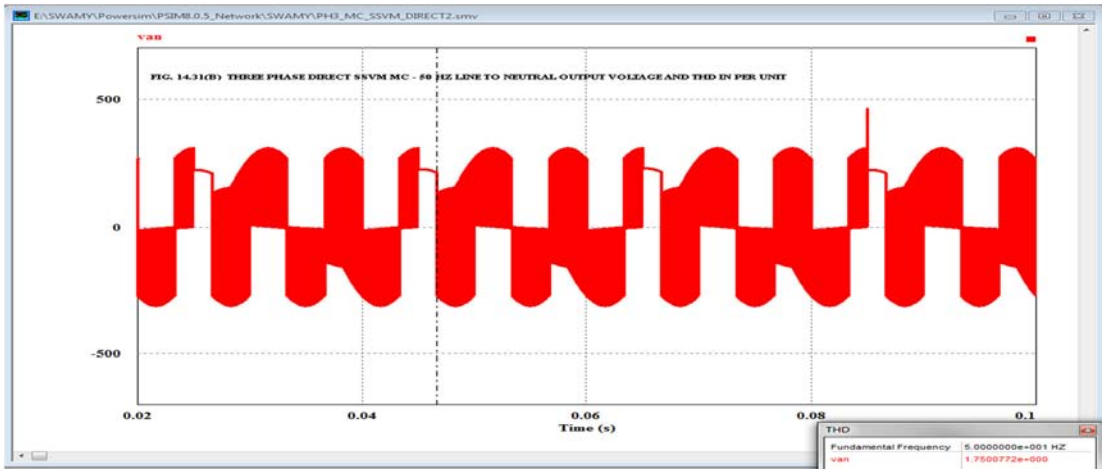
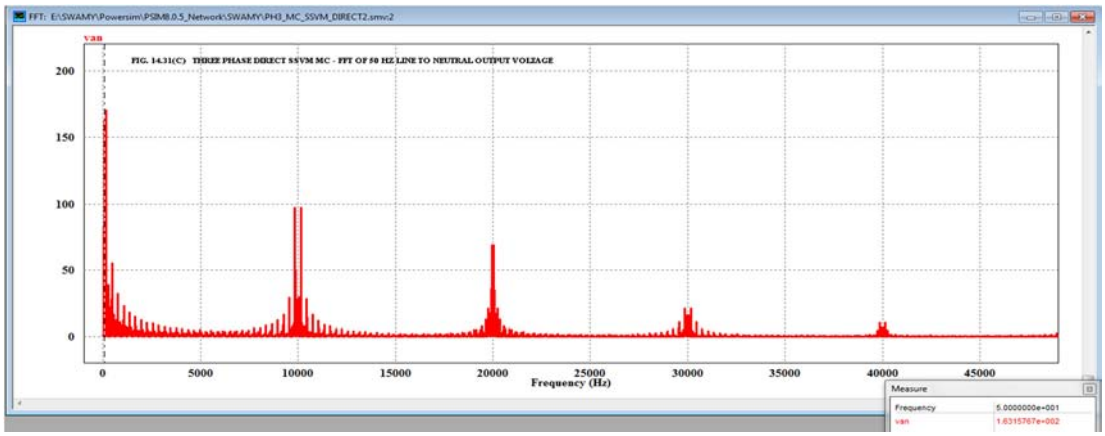
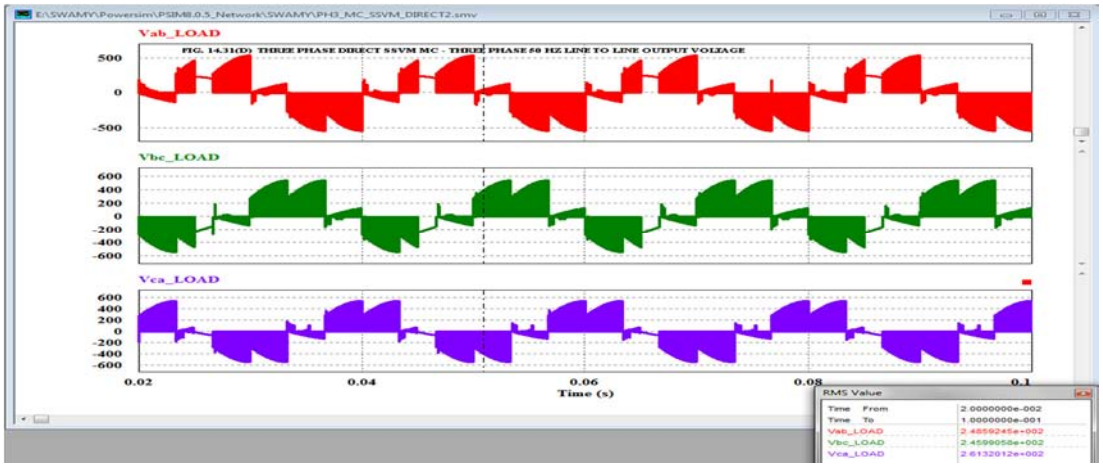


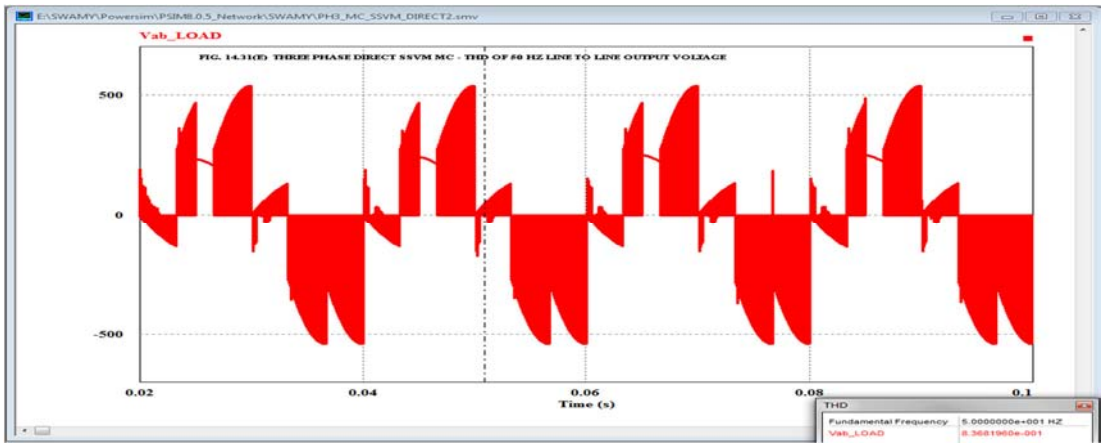
FIG. 14.30 MODEL OF DIRECT SSVM THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER

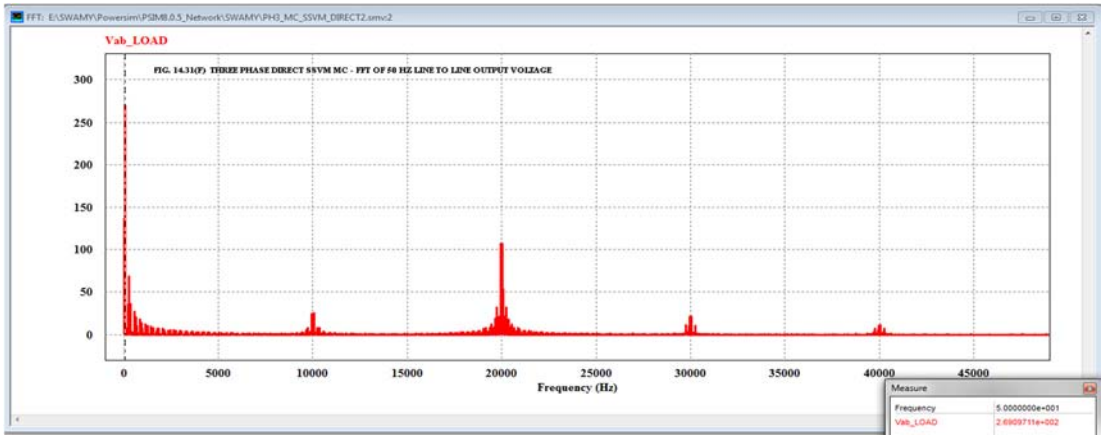

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_SSVM_DIRECT2.smv
van
FIG. 14.31(A) THREE PHASE DIRECT SSVM MC - THREE PHASE 50 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
500
0
-500
vbn
400
200
0
-200
-400
vcn
600
400
200
0
-200
-400
0.02
0.04
0.06
0.08
0.1
Time (s)
RMS Value
Time From 2.0000000e-002
Time To 1.0000000e-001
van 2.3408269e+002
vbn 2.2634601e+002
vcn 2.3073783e+002

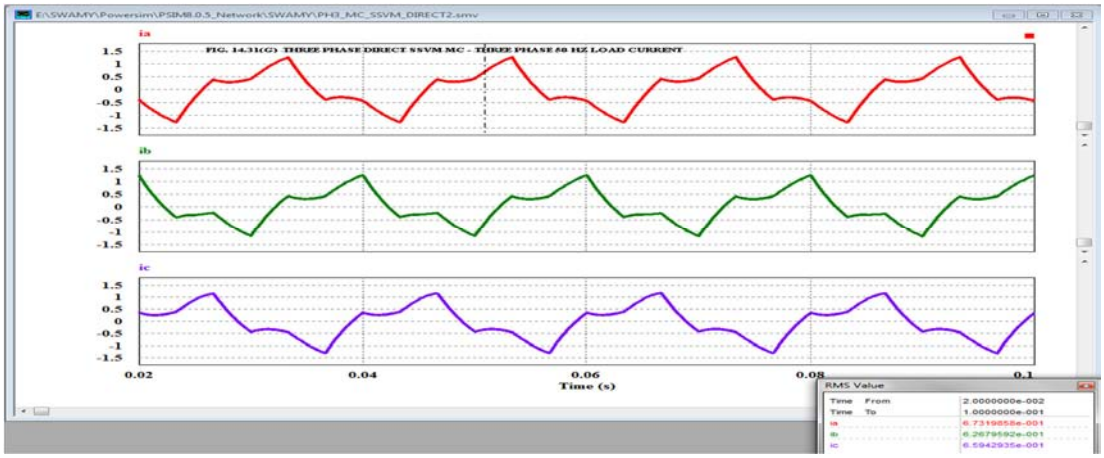

E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_SSVM_DIRECT2.smv
van
FIG. 14.31(B) THREE PHASE DIRECT SSVM MC - 50 HZ LINE TO NEUTRAL OUTPUT VOLTAGE AND THD IN PER UNIT
500
0
-500
0.02
0.04
0.06
0.08
0.1
Time (s)
THD
Fundamental Frequency 5.0000000e+001 HZ
van 1.7500772e+000

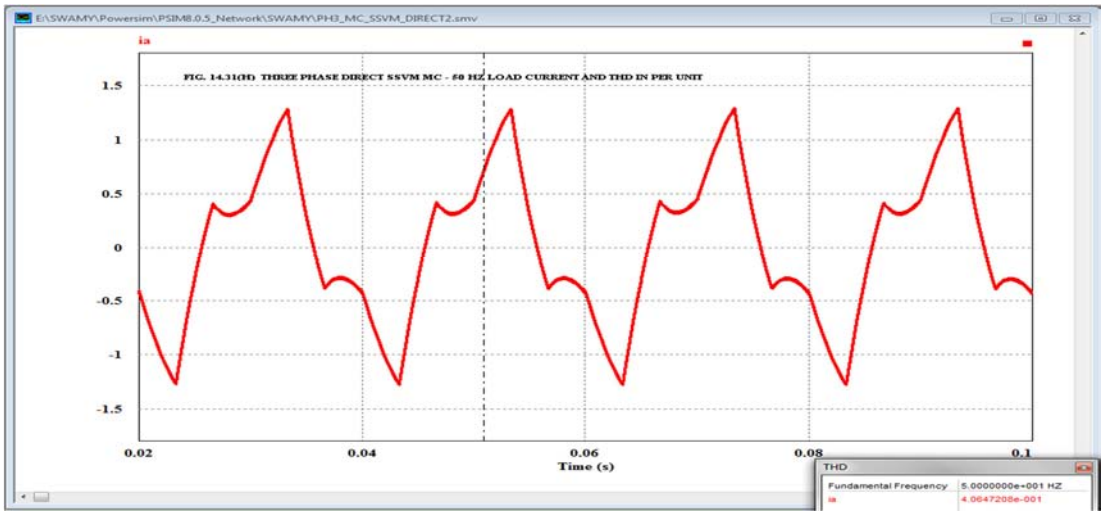

FFT: E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_SSVM_DIRECT2.smv:2
van
FIG. 14.31(C) THREE PHASE DIRECT SSVM MC - FFT OF 50 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
200
150
100
50
0
0
5000
10000
15000
20000
25000
30000
35000
40000
45000
Frequency (Hz)
Measure
Frequency 5.0000000e+001
van 1.6315767e+002


E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_SSVM_DIRECT2.smv
Vab_LOAD
FIG. 14.31(D) THREE PHASE DIRECT SSVM MC - THREE PHASE 50 HZ LINE TO LINE OUTPUT VOLTAGE
500
0
-500
Vbc_LOAD
600
400
200
0
-200
-400
-600
Vca_LOAD
600
400
200
0
-200
-400
-600
0.02
0.04
0.06
0.08
0.1
Time (s)
RMS Value
Time From 2.0000000e-002
Time To 1.0000000e-001
Vab_LOAD 2.4859245e+002
Vbc_LOAD 2.4599058e+002
Vca_LOAD 2.6132012e+002


Vab_LOAD
FIG. 14.31(E) THREE PHASE DIRECT SSVM MC - THD OF 50 HZ LINE TO LINE OUTPUT VOLTAGE
500
0
-500
0.02
0.04
0.06
0.08
0.1
Time (s)
THD
Fundamental Frequency
5.0000000e+001 HZ
Vab_LOAD
8.3681960e-001


FFT: E:\SWAMY\Powersim\PSIM8.0.5_Network\SWAMY\PH3_MC_SSVM_DIRECT2.smv:2
Vab_LOAD
FIG. 14.31(F) THREE PHASE DIRECT SSVM MC - FFT OF 50 HZ LINE TO LINE OUTPUT VOLTAGE
300
250
200
150
100
50
0
0
5000
10000
15000
20000
25000
30000
35000
40000
45000
Frequency (Hz)
Measure
Frequency
5.0000000e+001
Vab_LOAD
2.6909711e+002


ia
FIG. 14.31(G) THREE PHASE DIRECT SSVM MC - THREE PHASE 50 HZ LOAD CURRENT
ib
ic
1.5
1
0.5
0
-0.5
-1
-1.5
0.02
0.04
0.06
0.08
0.1
Time (s)
RMS Value
Time From
2.0000000e-002
Time To
1.0000000e-001
ia
6.7319858e-001
ib
6.2679592e-001
ic
6.5942935e-001


ia
FIG. 14.31(H) THREE PHASE DIRECT SSVM MC - 50 HZ LOAD CURRENT AND THD IN PER UNIT
1.5
1
0.5
0
-0.5
-1
-1.5
0.02
0.04
0.06
0.08
0.1
Time (s)
THD
Fundamental Frequency
5.0000000e+001 HZ
ia
4.0647208e-001

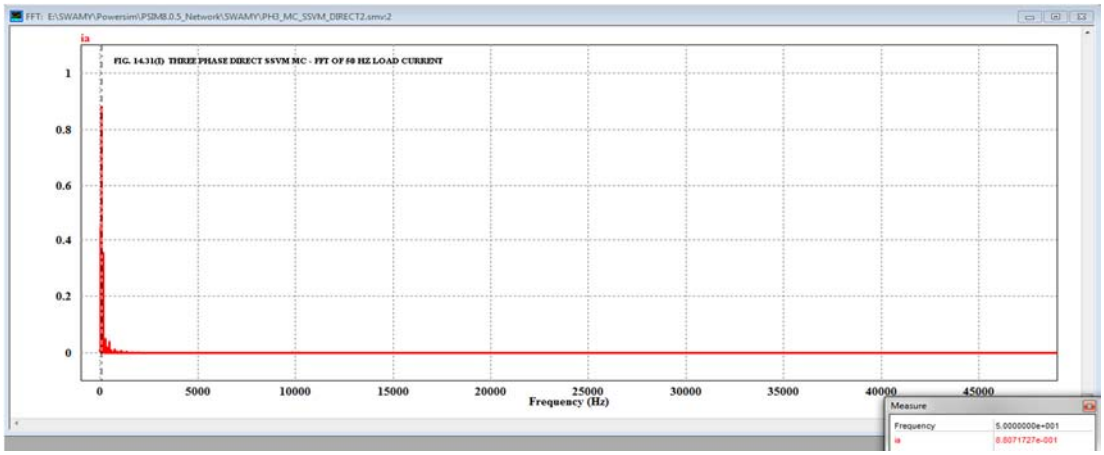


FIG. 14.31(I) THREE PHASE DIRECT SSVM MC - FFT OF 60 HZ LOAD CURRENT
ia
Frequency (Hz)

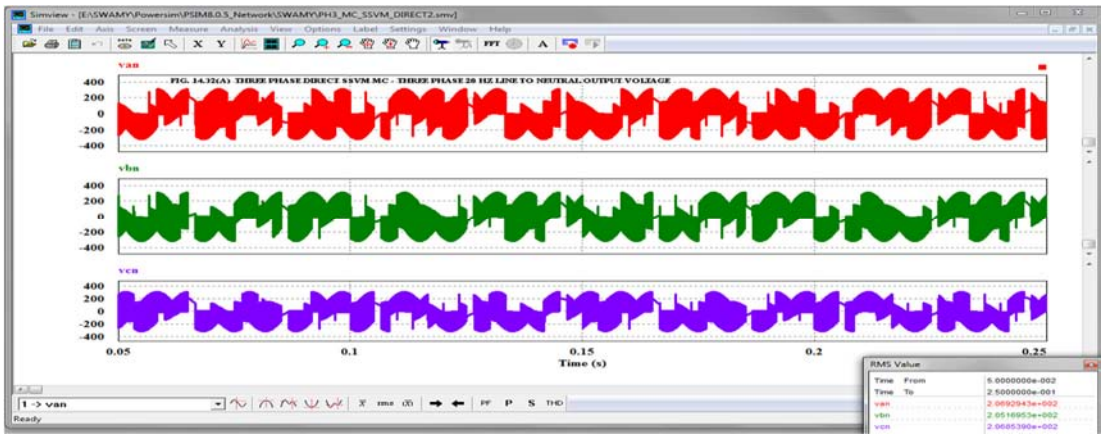


FIG. 14.32(A) THREE PHASE DIRECT SSVM MC - THREE PHASE 20 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
van
vbn
vcn
Time (s)

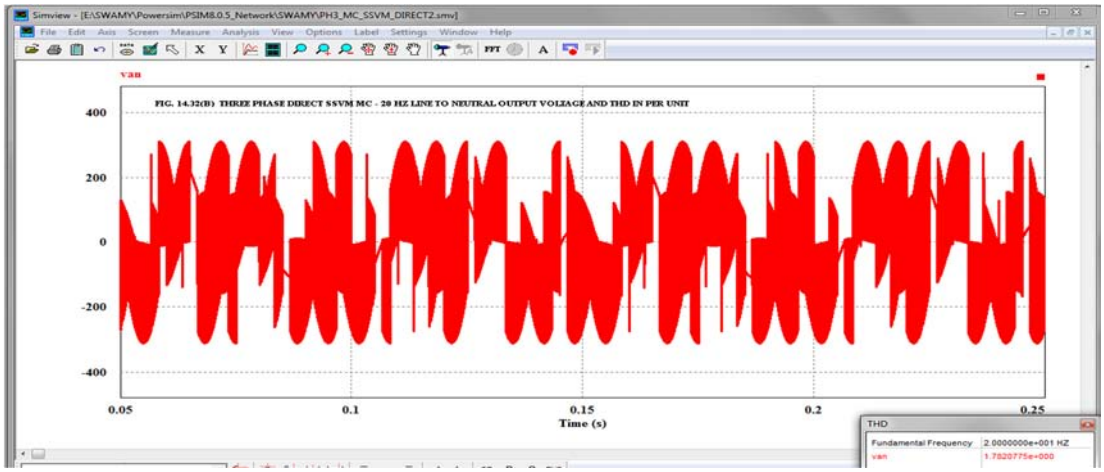


FIG. 14.32(B) THREE PHASE DIRECT SSVM MC - 20 HZ LINE TO NEUTRAL OUTPUT VOLTAGE AND THD IN PER UNIT
van
Time (s)

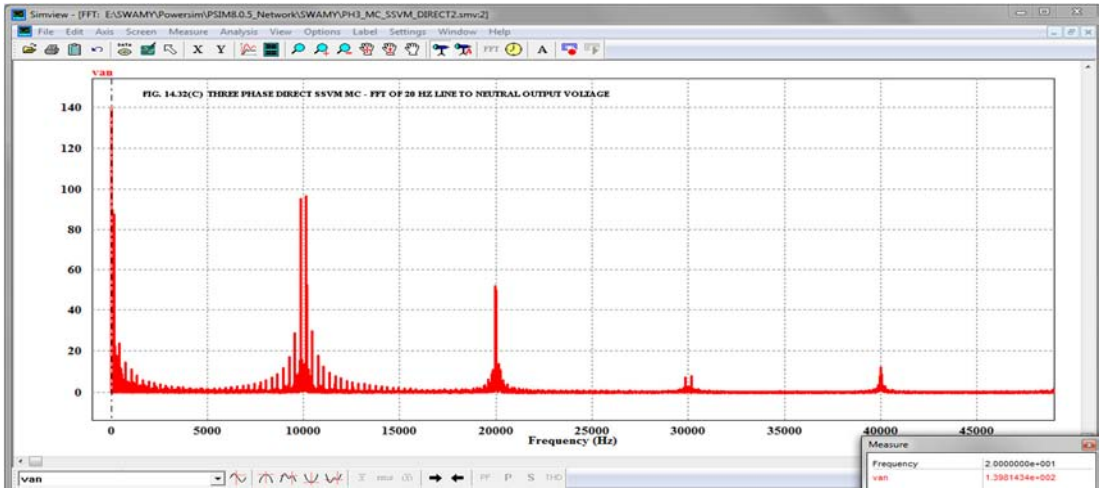
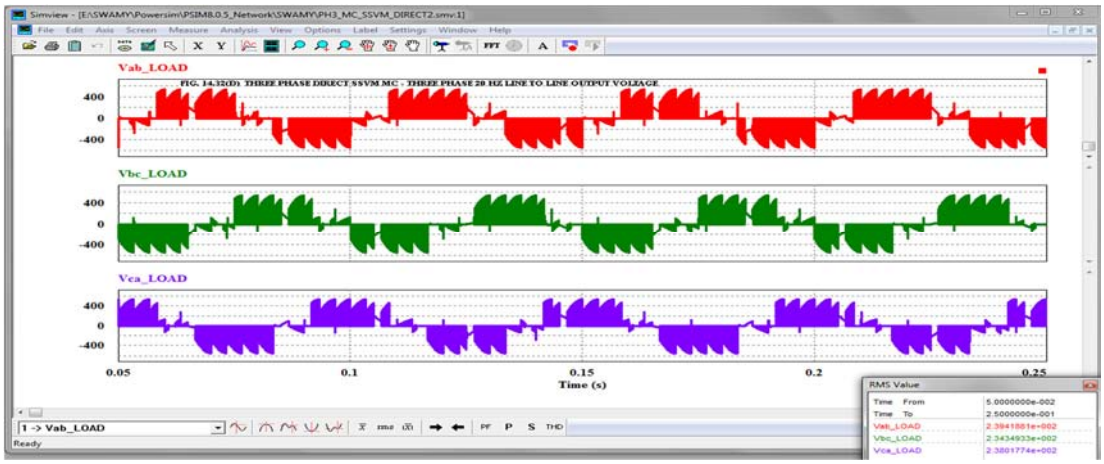
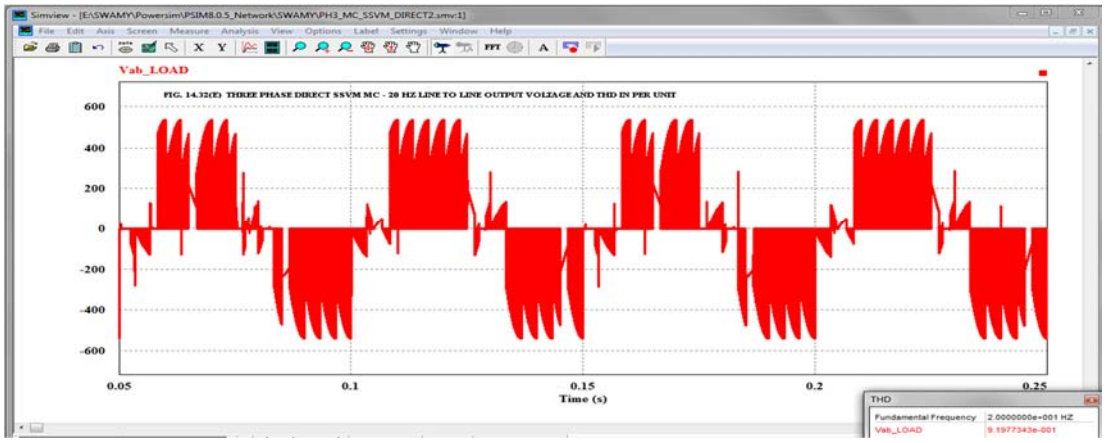
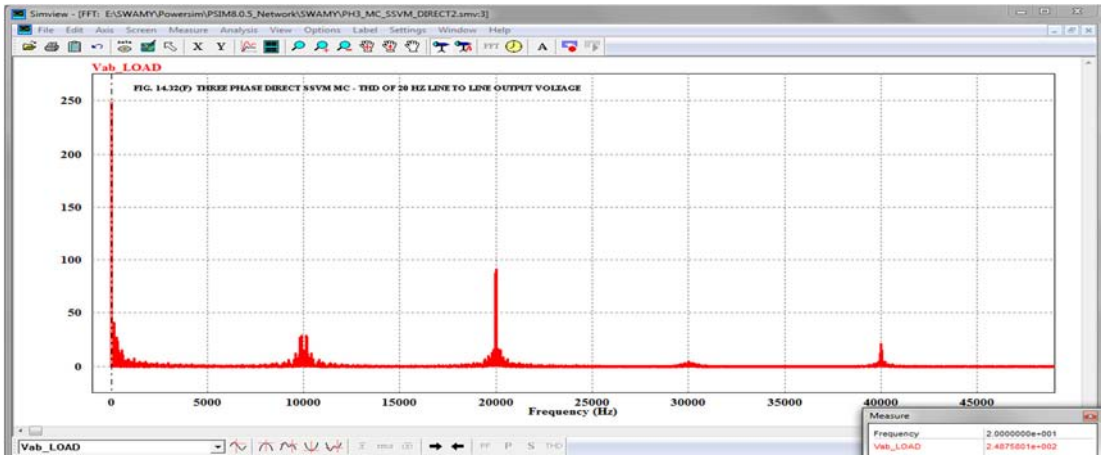
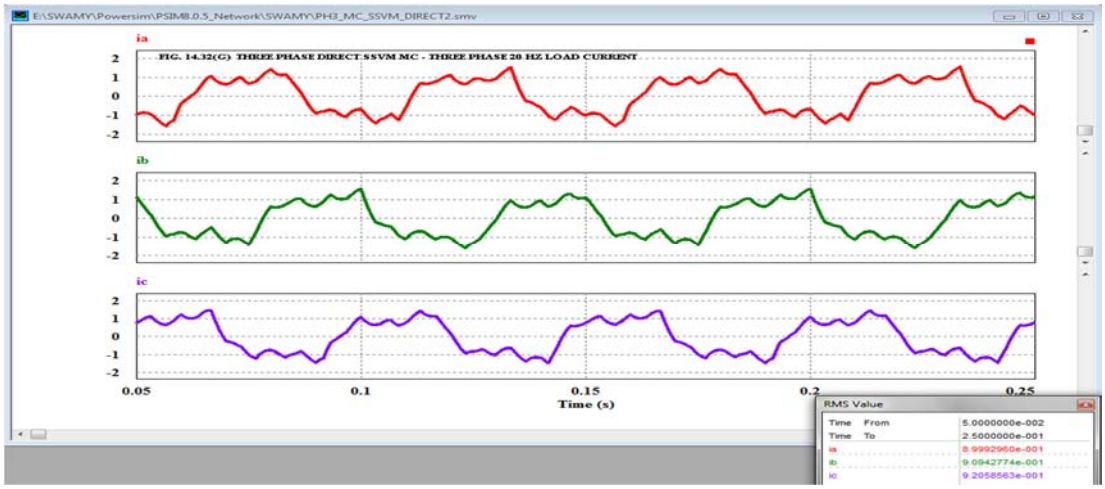


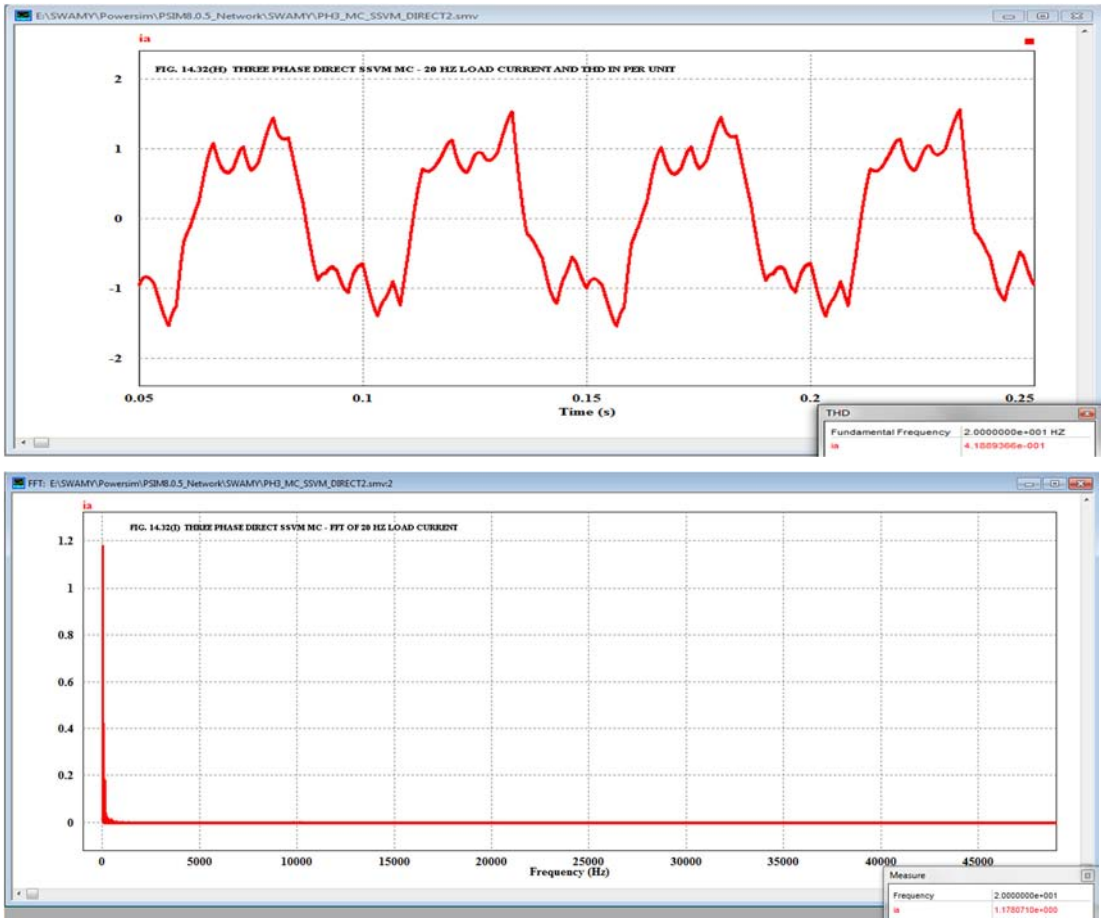
FIG. 14.32(C) THREE PHASE DIRECT SSVM MC - FFT OF 20 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
van
Frequency (Hz)


Vab_LOAD
FIG. 14.32(D) THREE PHASE DIRECT SSVM MC - THREE PHASE 20 HZ LINE TO LINE OUTPUT VOLTAGE
Vbc_LOAD
Vca_LOAD
Time (s)
RMS Value


Vab_LOAD
FIG. 14.32(E) THREE PHASE DIRECT SSVM MC - 20 HZ LINE TO LINE OUTPUT VOLTAGE AND THD IN PER UNIT
Time (s)
THD


Vab_LOAD
FIG. 14.32(F) THREE PHASE DIRECT SSVM MC - THD OF 20 HZ LINE TO LINE OUTPUT VOLTAGE
Frequency (Hz)
Measure


ia
FIG. 14.32(G) THREE PHASE DIRECT SSVM MC - THREE PHASE 20 HZ LOAD CURRENT
ib
ic
Time (s)
RMS Value



the line to neutral, line to line output voltages, input current and load current are -187.77, -241.06, -645.90 and -222.30 respectively. For the above delta-sigma modulated MC using Ned Mohan algorithm, with an input and output frequency of 50 Hz and 20 Hz, the percentage error in the above order are 63.87, 39.77, -274.26 and 32.96 respectively. Also it is seen that with IM load, for both cases of the algorithm with delta-sigma modulated MC the speed of the IM tries to reach the no load speed. The simulation time used with PSIM and SIMULINK model in Chapter XI are different and hence the rated no load speed of the IM can't be observed with PSIM model.

Comparing the simulation results of the single phase AC to three phase AC MC using SIMULINK in Chapter XII with that of the PSIM model of single phase AC to three phase AC MC, it is seen that with IM load in both cases three phase 50 Hz line to line output voltages are obtained from single phase 50 Hz AC supply and that the IM picks up speed. Also with R-L load, three phase 50 Hz as well as 20 Hz line to line output voltages are obtained in both cases with SIMULINK and PSIM software. The three phase 50 Hz stator current of the IM are NOT well balanced in both cases.

14.15 CONCLUSIONS: This chapter provides a verification of the performance of the selected models using SIMULINK discussed in the previous chapters. Both PSIM and PSCAD softwares are used for verification. Verification of the three phase MC performance using Venturini, Sunter-Clare and Ned Mohan algorithm shows a reasonable value for the error. Model verification for three phase Mutilevel MC with three FC shows reasonable error for the line to neutral and line to line output volt-

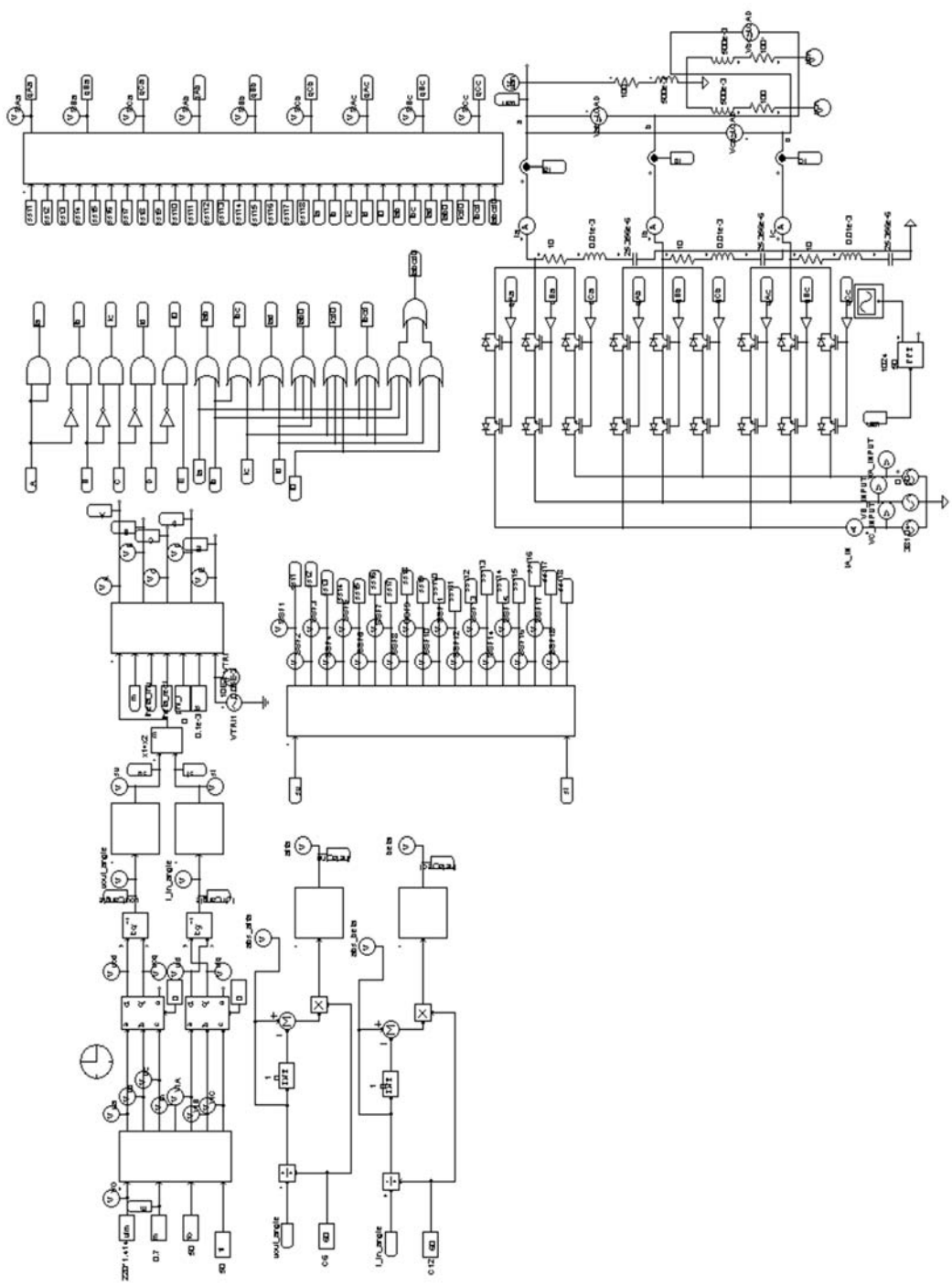


FIG. 14.33 MODEL OF INDIRECT SVM THREE PHASE AC TO THREE PHASE AC MATRIX CONVERTER

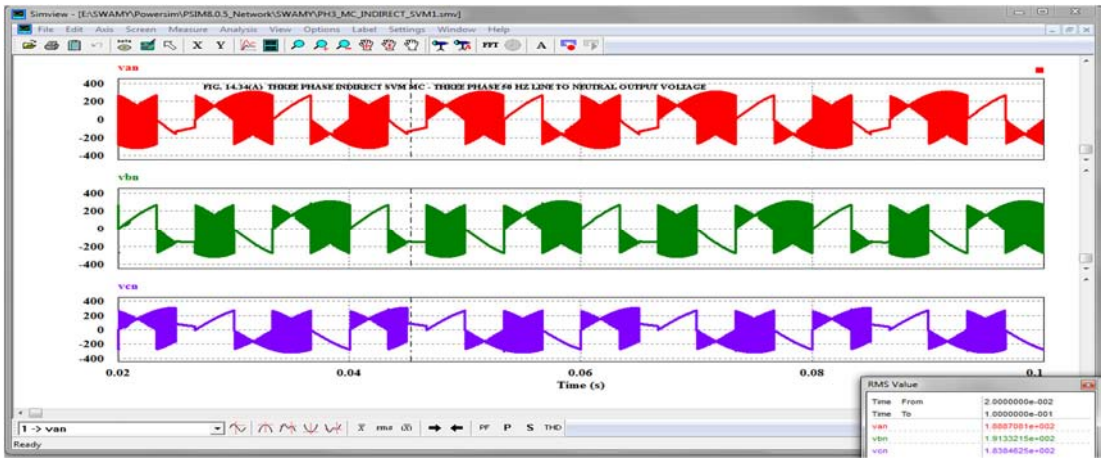


FIG. 14.34(A) THREE PHASE INDIRECT SVM MC - THREE PHASE 60 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
van
vbn
vcn
Time (s)
RMS Value

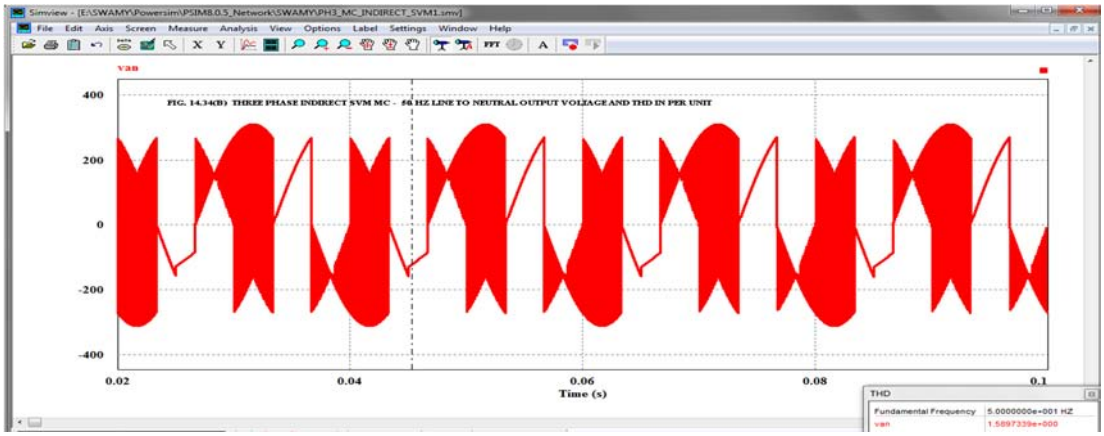


FIG. 14.34(B) THREE PHASE INDIRECT SVM MC - 60 HZ LINE TO NEUTRAL OUTPUT VOLTAGE AND THD IN PER UNIT
van
Time (s)
THD

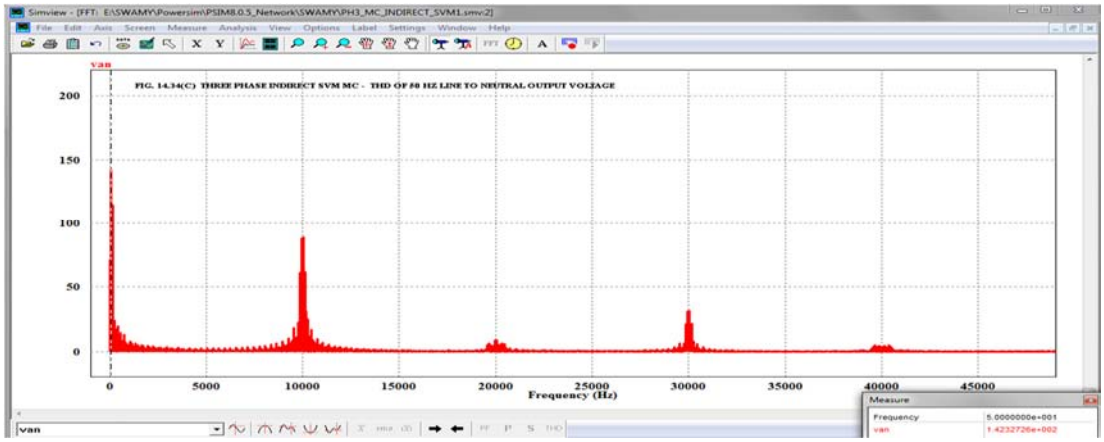


FIG. 14.34(C) THREE PHASE INDIRECT SVM MC - THD OF 60 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
van
Frequency (Hz)
Measure

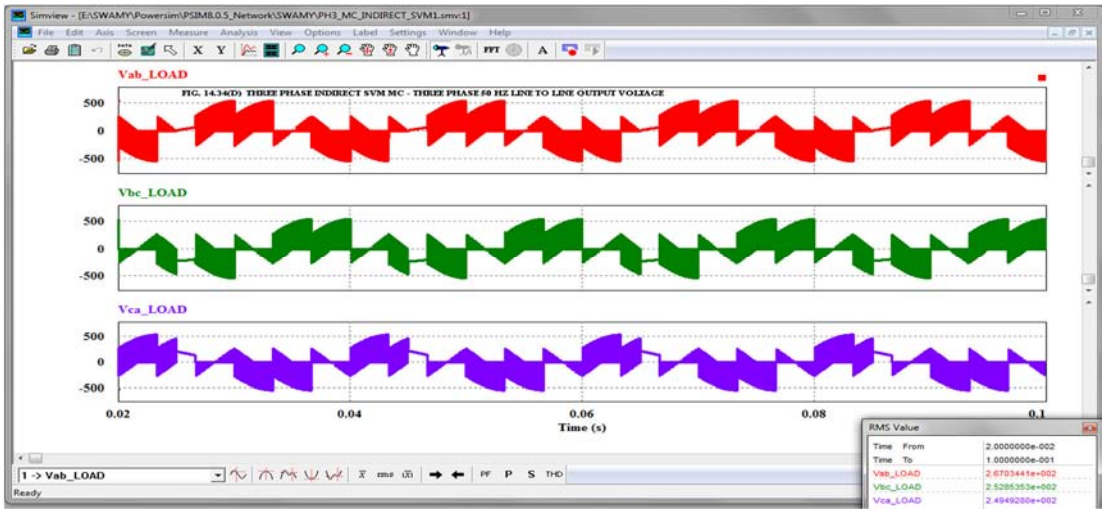
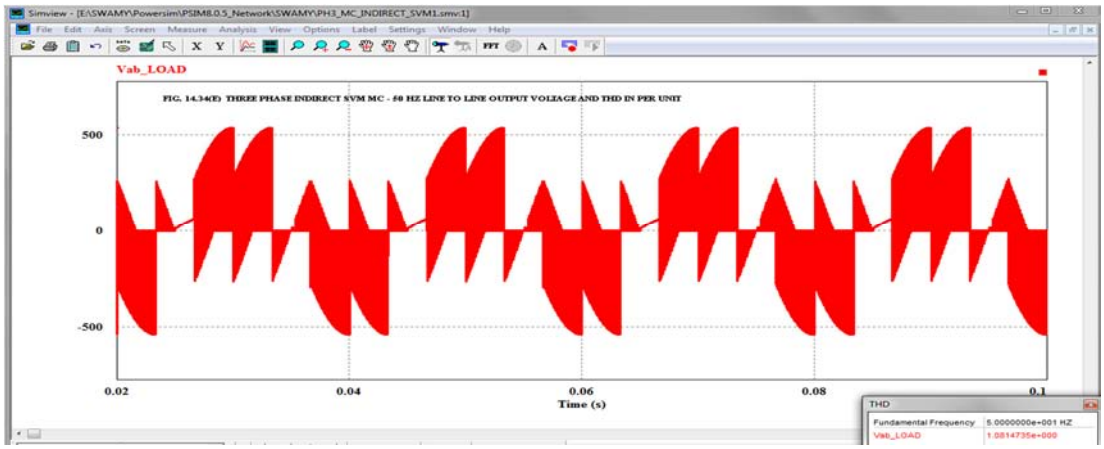
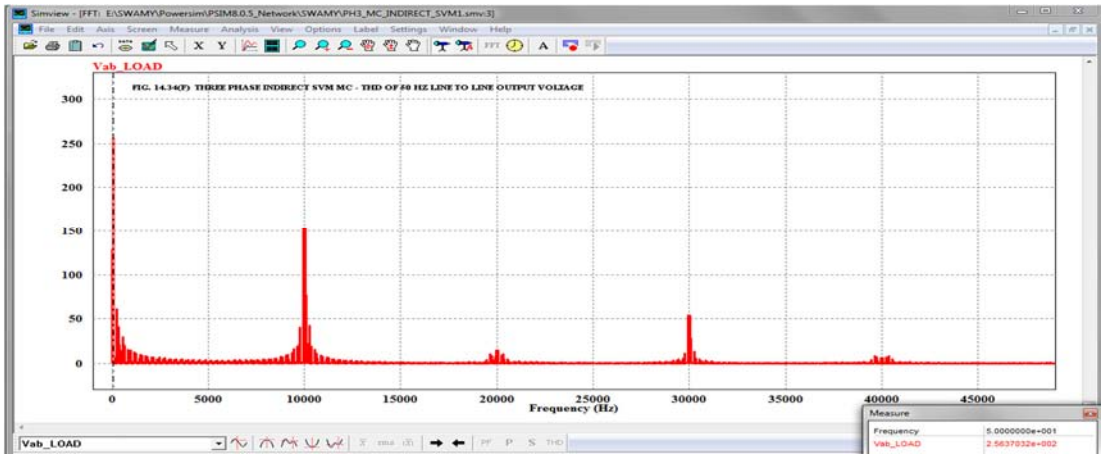
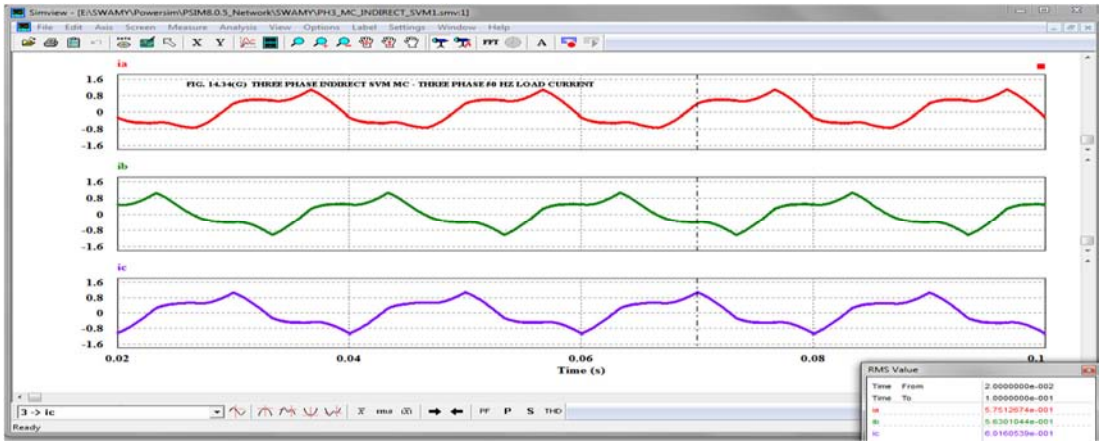
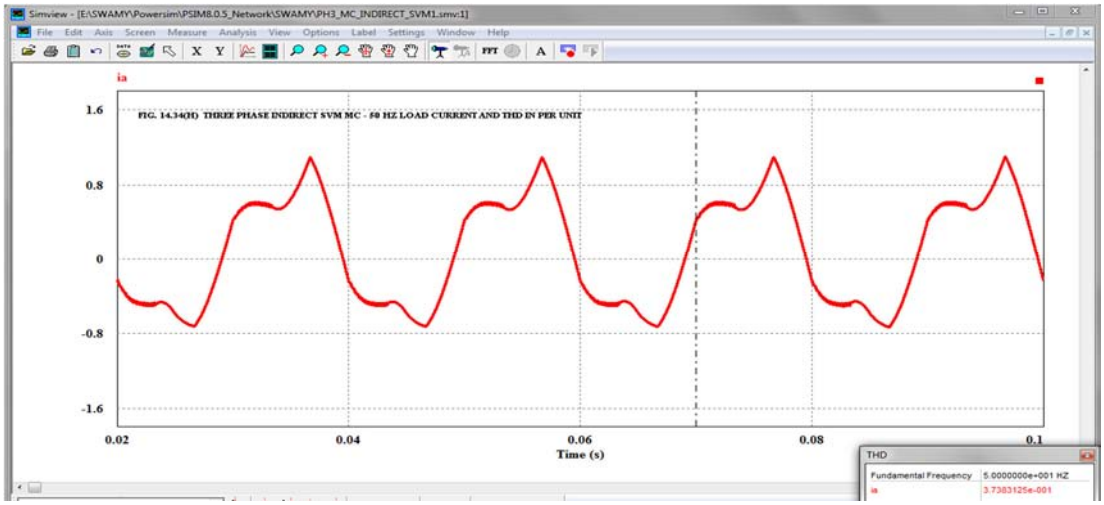


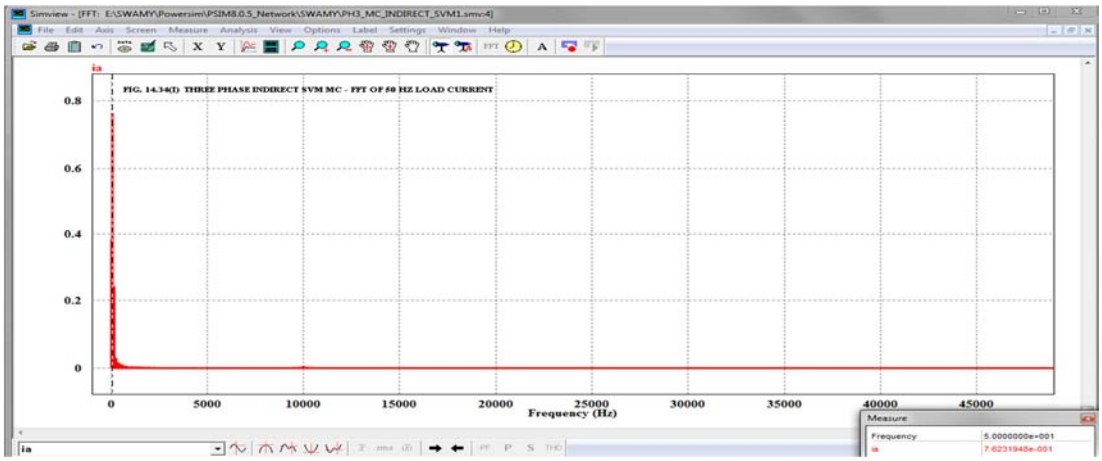
FIG. 14.34(D) THREE PHASE INDIRECT SVM MC - THREE PHASE 60 HZ LINE TO LINE OUTPUT VOLTAGE
Vab_LOAD
Vbc_LOAD
Vca_LOAD
Time (s)
RMS Value

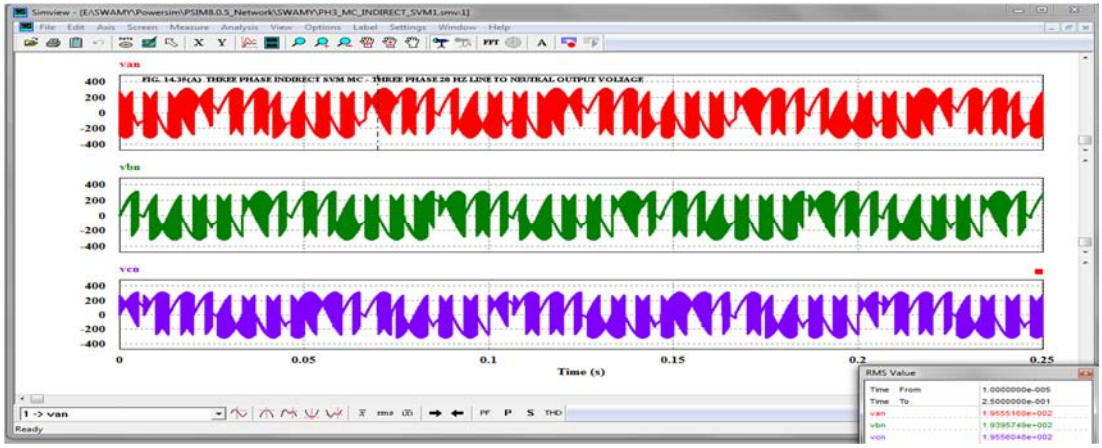

Vab_LOAD
FIG. 14.34(E) THREE PHASE INDIRECT SVM MC - 50 HZ LINE TO LINE OUTPUT VOLTAGE AND THD IN PER UNIT
500
0
-500
0.02
0.04
0.06
0.08
0.1
Time (s)
THD
Fundamental Frequency
5.0000000e+001 HZ
Vab_LOAD
1.0814735e+000

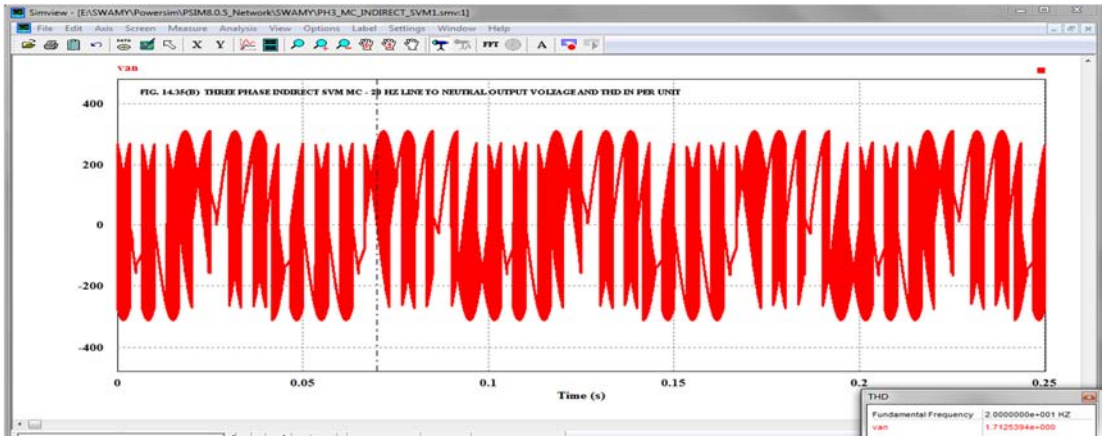

Vab_LOAD
FIG. 14.34(F) THREE PHASE INDIRECT SVM MC - THD OF 50 HZ LINE TO LINE OUTPUT VOLTAGE
300
250
200
150
100
50
0
0
5000
10000
15000
20000
25000
30000
35000
40000
45000
Frequency (Hz)
Measure
Frequency
5.0000000e+001
Vab_LOAD
2.5637032e+002
Vab_LOAD

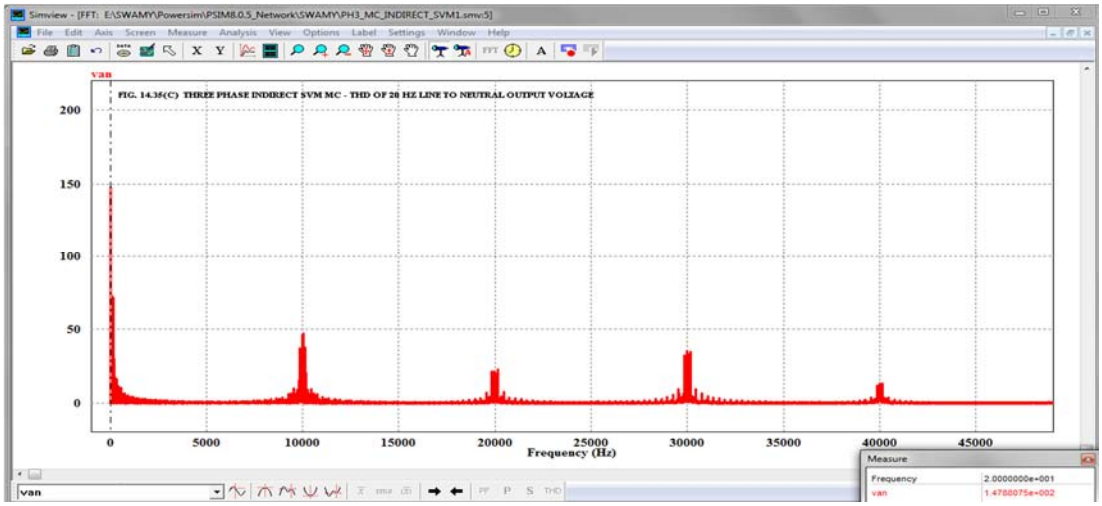

ia
FIG. 14.34(G) THREE PHASE INDIRECT SVM MC - THREE PHASE 50 HZ LOAD CURRENT
ib
ic
1.6
0.8
0
-0.8
-1.6
0.02
0.04
0.06
0.08
0.1
Time (s)
RMS Value
Time From
2.0000000e-002
Time To
1.0000000e-001
3 -> ic
Ready

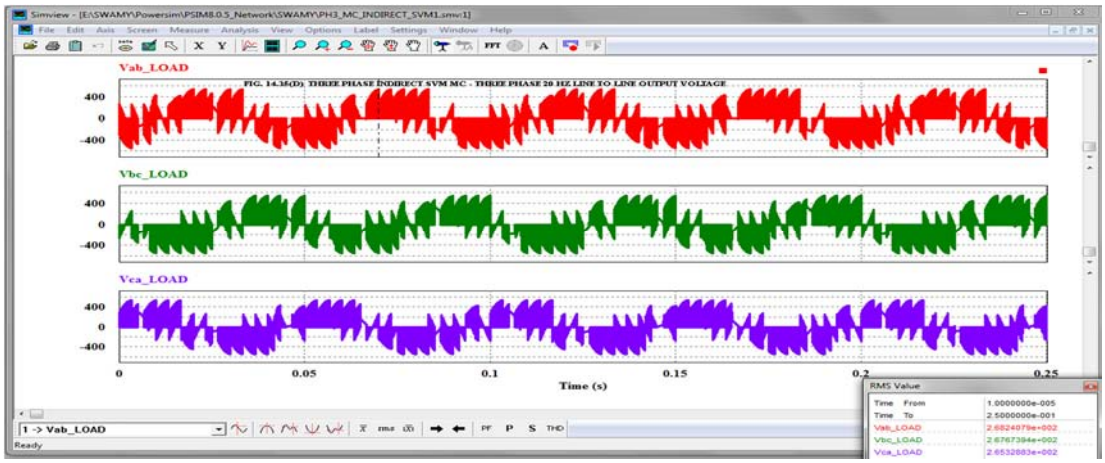

ia
FIG. 14.34(H) THREE PHASE INDIRECT SVM MC - 50 HZ LOAD CURRENT AND THD IN PER UNIT
1.6
0.8
0
-0.8
-1.6
0.02
0.04
0.06
0.08
0.1
Time (s)
THD
Fundamental Frequency
5.0000000e+001 HZ
3.7383125e-001

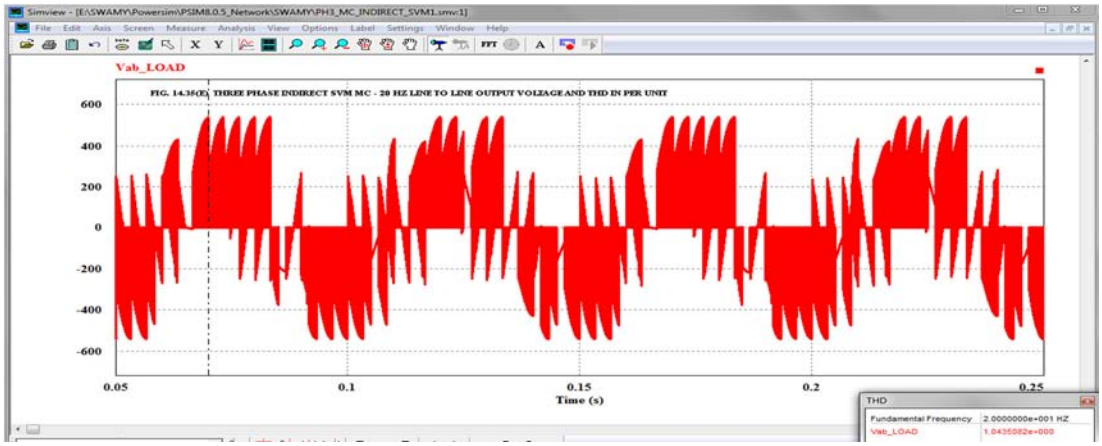

ia
FIG. 14.34(I) THREE PHASE INDIRECT SVM MC - FFT OF 60 HZ LOAD CURRENT
0.8
0.6
0.4
0.2
0
0
5000
10000
15000
20000
25000
30000
35000
40000
45000
Frequency (Hz)
Measure
Frequency
5.0000000e-001
ia
7.6231948e-001

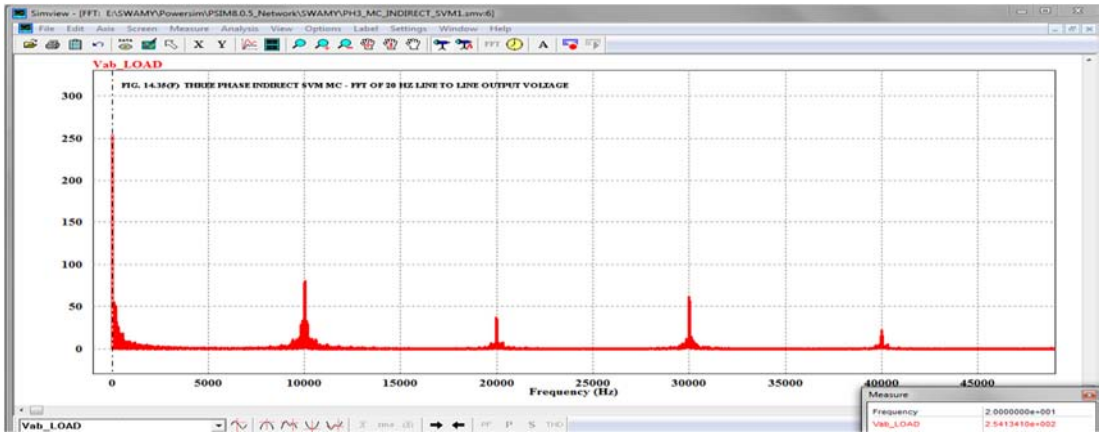

van
FIG. 14.3J(A) THREE PHASE INDIRECT SVM MC - THREE PHASE 20 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
400
200
0
-200
-400
vbn
vcn
0
0.05
0.1
0.15
0.2
0.25
Time (s)
1 -> van
Ready
RMS Value
Time From
1.0000000e-005
Time To
2.5000000e-001
van
1.9555160e+002
vbn
1.9395749e+002
vcn
1.9556045e+002

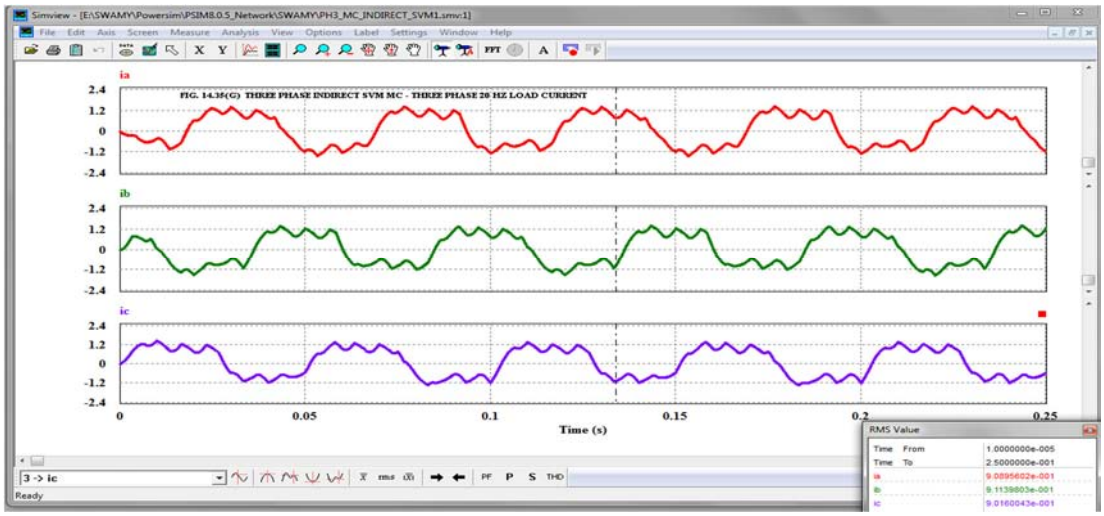

van
FIG. 14.3J(B) THREE PHASE INDIRECT SVM MC - 20 HZ LINE TO NEUTRAL OUTPUT VOLTAGE AND THD IN PER UNIT
400
200
0
-200
-400
0
0.05
0.1
0.15
0.2
0.25
Time (s)
THD
Fundamental Frequency
2.0000000e+001 HZ
van
1.7125394e+000

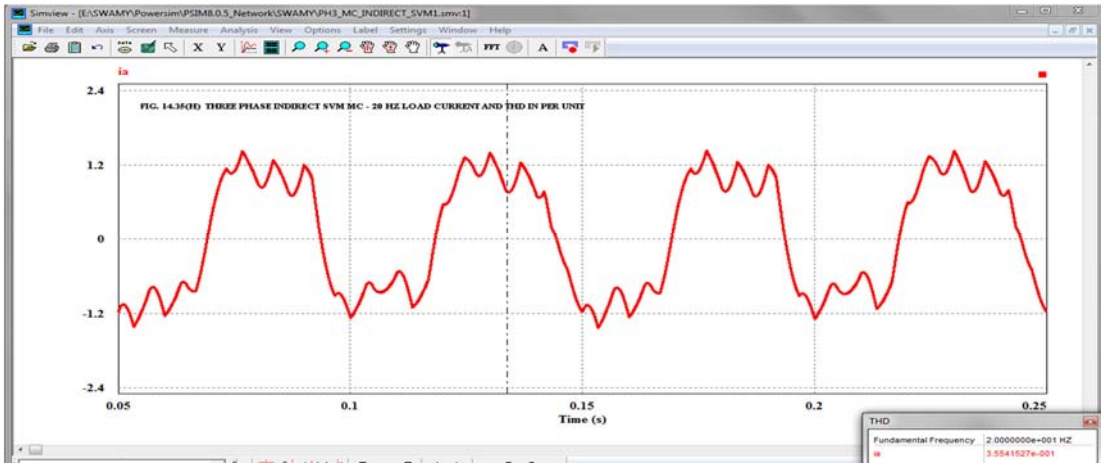

van
FIG. 14.3J(C) THREE PHASE INDIRECT SVM MC - THD OF 20 HZ LINE TO NEUTRAL OUTPUT VOLTAGE
200
150
100
50
0
0
5000
10000
15000
20000
25000
30000
35000
40000
45000
Frequency (Hz)
Measure
Frequency
2.0000000e+001
van
1.4788075e+002

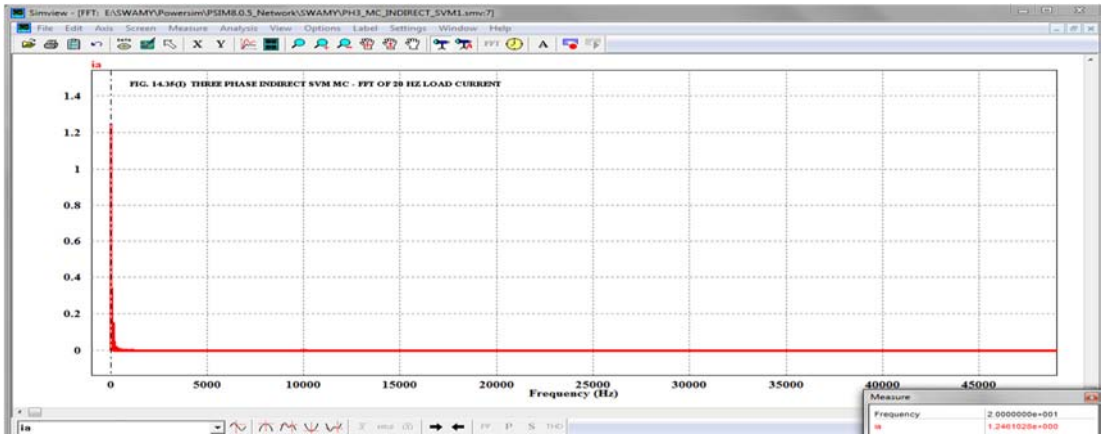

Vab_LOAD
FIG. 14.36(D) THREE PHASE INDIRECT SVM MC - THREE PHASE 20 HZ LINE TO LINE OUTPUT VOLTAGE
Vbc_LOAD
Vca_LOAD
Time (s)
RMS Value


Vab_LOAD
FIG. 14.36(E) THREE PHASE INDIRECT SVM MC - 20 HZ LINE TO LINE OUTPUT VOLTAGE AND THD IN PER UNIT
Time (s)
THD


Vab_LOAD
FIG. 14.36(F) THREE PHASE INDIRECT SVM MC - FFT OF 20 HZ LINE TO LINE OUTPUT VOLTAGE
Frequency (Hz)
Measure


ia
FIG. 14.36(G) THREE PHASE INDIRECT SVM MC - THREE PHASE 20 HZ LOAD CURRENT
ib
ic
Time (s)
RMS Value





ages and a large value of error for the input current. The SIMULINK models for three phase MMC with three and six FC have been replaced by software PSCAD and the results verified by PSIM and found to have error within reasonable limit. The three phase MMC with six FC is a novel contribution. In the case of three phase Direct ASVM, SSVM and Indirect SVM of MC, reasonable errors are found for the line to neutral output voltage, line to line output voltage and load current. In the case of three phase delta-sigma modulated MC using both Venturini and Ned Mohan algorithm, it is seen that unreasonably large values of errors are observed for three phase input current and load current by model verification using PSIM. One of the greatest achievements of this research project is the discovery of the Dual Programmable AC to DC rectifier using three phase AC to three phase AC MC topology and the model verification using PSCAD results in close agreement with the performance using SIMULINK model. This opens up a new path way for the development of Hybrid Electric Vehicle and Electric Traction and associated control using dSPACE which can be used to drive separately excited DC motor and Permanent Magnet DC Motor. Also model verification using PSIM reveals possibility of generating three phase AC from single phase AC directly using MC without the need for AC to DC rectification and then DC to AC inversion.

Chapter XV
Conclusions

15.1 INTRODUCTION: This chapter provides the summary of contributions and conclusions drawn from the simulation results or performance of the three phase Matrix Converter (MC) models discussed in the previous chapters.

15.2 SUMMARY OF CONTRIBUTIONS AND DERIVED CONCLUSIONS: This thesis presents the modelling of three phase AC to three Phase AC Matrix Converter (MC) starting from the fundamental Venturini, Optimum Venturini algorithms [1-5] to the recent algorithms proposed by Sunter-Clare [11-12] and the one by Ned Mohan [13-14, 16-17] for switching three phase AC to three phase AC MC.

The application of the above mentioned algorithms for switching three phase AC to three phase AC MC driving Vector Controlled Induction Motor (IM) drive [15] is also successfully presented in this thesis. Simulation results indicate that accurate speed control of three phase vector controlled IM drive is possible with the rotor speed reaching the set point value in spite of mechanical load variation.

Real time control of a three phase AC to single phase AC MC hardware assembled using IGBT bidirectional switches, switched by gate pulses from model of the above MC using SIMULINK and dSPACE blockset interfaced to dSPACE DS1104 hardware controller board is successfully presented and the experimental result obtained is compared with model performance.

Three Phase AC to Three Phase AC Multilevel Matrix Converters (MMCs) with two and three Flying Capacitors (FCs) have been proposed in the literature to improve the harmonic performance of the three phase MC [18-19]. In this thesis models have been developed for three phase MMC with three and six FCs. The model of **three phase MMC with six FC** is a novel and an **original** contribution in this thesis. It is found by model simulation that the harmonic performance of three phase MMC with three and six FCs are found to be superior to that of the conventional three phase MC. Another special feature of this thesis and an **original** contribution is that for **three phase MMC with three FC, modelling equations for three phase output voltage and input current are presented in matrix form as a Boolean logic expression in terms of the MC switch states** such as whether a MC switch state is ON (logic 1) or OFF (logic 0).

Based on the method presented for the Direct Asymmetrical and Direct Symmetrical Space Vector Modulation of three phase AC to three phase AC MC in the literature [31-38] references, models have been presented in this thesis for the direct Asymmetrical Space Vector Modulation (ASVM) and also for the direct Symmetrical Space Vector Modulation (SSVM) of three phase AC to three phase AC MC. A notable **original** contribution in this thesis is the development of the model for the **direct**

Asymmetrical Centre Zero Space Vector Modulation (CZSVM) which shows how the location of the zero output voltage vector can be relocated. Various locations for the zero output voltage vector can be tried for optimum performance of the MC.

The Indirect Space Vector Modulation (ISVM) assumes a three phase AC to three Phase AC MC consisting of a three phase AC to DC rectifier and a DC to three phase AC Inverter [25-30]. In this thesis models have been successfully developed for three phase AC to three phase AC ISVM MC.

Dual fixed AC to DC rectifier using three phase AC to three phase AC MC topology is available in the literature [43-45]. One of the greatest achievements of this research thesis is the **discovery** of the model for **Dual Programmable AC to DC rectifier using three phase AC to three phase AC MC topology and the mathematical derivation based on phasor diagram for the performance of the above Dual programmable AC to DC rectifier.** This is a highly **original** contribution in this thesis which is **NOT** hitherto reported in the literature references. Model performance is verified by theoretical calculations using derived equations and found to be successful. This **dual programmable AC to DC rectifier applications in the speed control and brake by plugging of separately excited DC motor and Permanent Magnet DC Motor is also presented and its real time applications using dSPACE** in Hybrid Electric Vehicle and electric traction are highlighted which is also an **original** contribution in this thesis..

Sample time based modulation also known as Delta-Sigma modulation applied to three phase AC to three phase AC MC is reported in the literature [46-48]. In this thesis, models have been presented for Delta-Sigma modulated three phase AC to three phase AC MC using both Venturini algorithm [1-5] and Advanced Modulation algorithm proposed by Ned Mohan [13-14, 16-17]. The **Delta-Sigma Modulated three phase AC to three phase AC MC using Advanced Modulation algorithm** is an **original** contribution in this thesis.

Direct conversion of Single phase fixed frequency AC voltage to three phase variable frequency AC voltage using MC without an intermediate capacitor storage element is reported in the literature [50]. Based on this literature reference, model has been developed for single phase AC to three phase AC MC and the performance of the model successfully tested for two different output frequencies with both R-L load and three phase IM load.

A Novel Pulse Width Modulated AC to AC Converter using a DC link is a new idea developed by the author of this thesis. In this, **single phase as well as three phase supply frequency AC to single phase as well as three phase variable frequency AC using NMOSFET-PMOSFET pair combination and bidirectional switches using IGBTs** are presented along with successful simulation results using hardware components for the gate drive. The author of this thesis presumes that this is an **original** contribution.

Above all, selected SIMULINK models from all the previous chapters have been verified for performance using either PSCAD or PSIM software and this verification report is presented.

Three appendices are presented. The first appendix gives the application of PIC microcontroller for saw-tooth carrier waveform generation and switching novel three phase AC to three phase AC converter using a DC link. The second appendix provides the model for speed control and brake by plugging of three phase IM fed by matrix converter, scheme for real time implementation of this model using dSPACE DS1104 hardware controller board and possible applications of this model for Hybrid Electric Vehicles and Electric traction. This model of three phase IM fed by MC with ability to control the speed and **brake by reversing the phase sequence of the three phase applied voltage** to the terminals of the IM and **the scheme for real time implementation using dSPACE** are **original** contribution in this thesis. The third appendix provides the list of publications from this thesis.

15.3 SUGGESTION FOR FURTHER WORK: A lot of further research work is possible in the following areas:

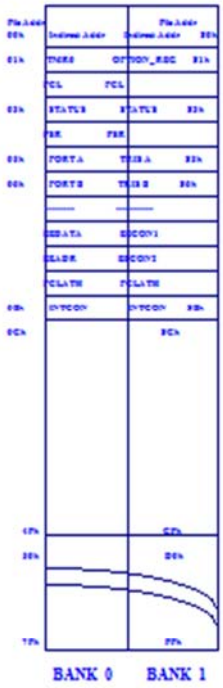
1) Dual Programmable AC to DC rectifier using Three Phase AC to Three Phase AC MC topology and real time speed control and brake by plugging of separately excited and Permanent Magnet DC motors using dSPACE hardware controller board.
2) Speed control and brake by plugging of three phase IM fed by MC in real time using dSPACE hardware controller board.
3) Delta-sigma modulation of three phase AC to three phase AC MC in real time using dSPACE hardware controller board.
4) Three Phase AC to Three Phase AC Multilevel MC and its real time implementation using dSPACE hardware controller board.
5) Implementation of Direct and Indirect Space Vector Modulation of three phase AC to three phase AC MC in real time using dSPACE hardware controller board.
6) Implementation of three phase Vector Controlled IM drive fed by MC in real time using dSPACE hardware controller board.
7) Implementation of single phase AC to three phase AC MC in real time using dSPACE hardware controller board.

Appendix I

PIC Microcontroller Applications

AI.1 INTRODUCTION: This appendix provides the PIC microcontroller approach for a) Designing the 2 kHZ saw-tooth carrier generator and b) Designing a gate drive for a 10 kHZ three phase inverter which can also be used as gate drive for the novel three phase AC to three phase AC converter using a DC link. The former one can be used to replace the 2 kHZ saw-tooth carrier generator using IC NE555 discussed in Chapter X of this thesis. The later one can be used to replace the modulo six counter and multiplexer used for switching the bidirectional switches of the AC to AC converter using a DC link discussed in Chapter XIII of this thesis.

AI.2 OVERVIEW OF PIC MICROCONTROLLER PIC 16F84A: The details of the PIC microcontroller PIC16F84A is available in the data sheet given in reference AI.6[1] below. Nevertheless for the purpose of systematically designing the above mentioned saw-tooth carrier and the three phase inverter gate drive, this data sheet is briefly reviewed here. The pin layout, register file map, STATUS register, OPTION register and INTCON register are briefly shown here in Fig. AI.1. Only essential Information required for this design are given in Fig. AI.1.



STATUS REGISTER (03h, 83h)

		RP0					

BIT 7 BIT 0

BIT 5 RP0 Register Bank Select Bits
01 = BANK 1
00 = BANK 0

OPTION REGISTER (81h)

		T0CS	T0SE	PSA	PS2	PS1	PS0

BIT 7 BIT 0

bit 5 T0CS: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 T0SE: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 PSA: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 PS2:PS0: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8
100	1:32	1:16
101	1:64	1:32
110	1:128	1:64
111	1:256	1:128

INTCON REGISTER (0Bh, 8Bh)

GIE		T0IE			T0IF		

BIT 7 BIT 0

bit 7 GIE: Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 5 T0IE: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 2 T0IF: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

FIG. AI.1 PIC 16F84A PIN LAYOUT, REGISTER FILE MAP, STATUS, OPTION AND INTCON REGISTER

AI.3 DESIGN OF A 2 KHz SAW-TOOTH CARRIER GENERATOR: The saw-tooth carrier generator is designed in the same way as given in chapter X of this thesis. Here IC NE555 is replaced by a PIC microcontroller PIC16F84A to generate a 2 kHz square pulse with an ON time of 494E-6 seconds and an OFF time of 6E-6 seconds.

The program is developed here using TMR0 as a timer to generate time delays of 494 and 6 microseconds respectively. A 4 MHz external clock source is used which is connected to RA4/TOCKI pin of PIC16F84A. A divide by eight prescaler is chosen. The following calculations are made to preset the count in TMR0 register to create the above time delays.

$$Clock\quad Frequency = \frac{4*10^{6}}{8} = 0.5*10^{6}\ Hz \qquad (AI.1)$$

$$Clock\quad Period = \frac{1}{0.5*10^{6}} = 2*10^{-6}\ Seconds \qquad (AI.2)$$

$$For\quad 494E-6\ Seconds\quad time\quad delay$$

$$2*10^{-6} * clock\,cycle1 = 494*10^{-6}$$

$$Clcock\,cycle1 = 247 \qquad (AI.3)$$

$$For\quad 6E-6\ Seconds\quad time\quad delay$$

$$2*10^{-6} * clock\,cycle2 = 6*10^{-6}$$

$$Clcock\,cycle2 = 3 \qquad (AI.4)$$

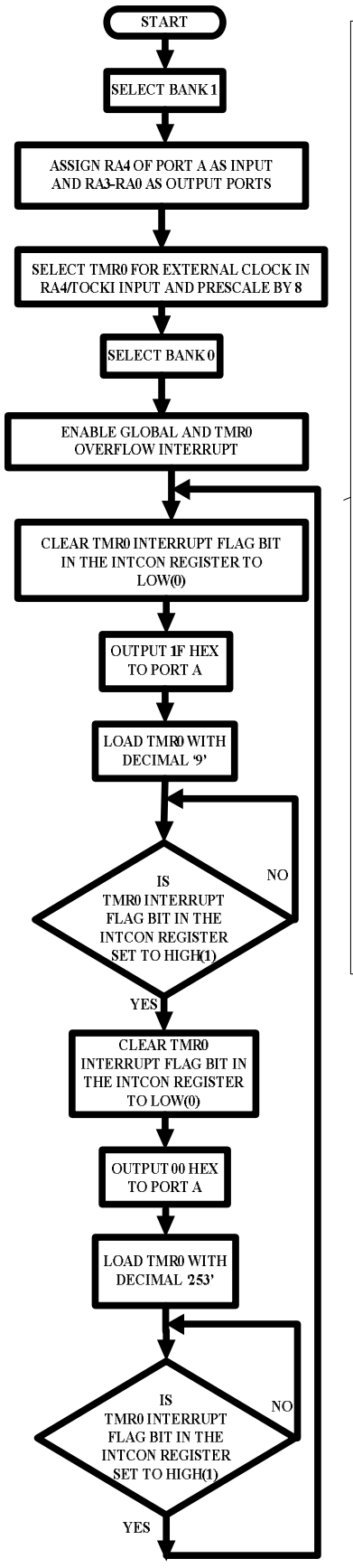
$$Preset\quad TMR0\quad for\quad a\quad delay\quad of\quad 494e-6seconds = (256-247) = 9 \qquad (AI.5)$$

$$Preset\quad TMR0\quad for\quad a\quad delay\quad of\quad 6e-6seconds = (256-3) = 253 \qquad (AI.6)$$

TMR0 is an eight bit register and the maximum count is FF hex which is 255. At 256th count TMR0 register overflows and the TMR0 overflow interrupt flag in the INTCON register set HIGH. Thus TMR0 is preset to count 9 and count 253 to create delays of 494e-6 seconds and 6e-6 seconds respectively. The flow-chart and source code for generating the square pulse with the above ON and OFF time using PIC16F84A is shown in Fig. AI.2. The 2 kHZ saw-tooth carrier generator using PIC16F84A is shown in Fig. AI.3.

AI.4 DESIGN OF A GATE DRIVE FOR A THREE PHASE AC TO THREE PHASE AC CONVERTER USING A DC LINK: The design of the three phase AC to three phase AC converter using a DC link is shown in Fig. 13.10 of Chapter XIII where a modulo six counter and a multiplexer is used to generate the variable frequency 50% duty-cycle three phase clock generator. In this section same variable frequency 50% duty-cycle clock generator is developed using PIC16F84A microcontroller. The Pulse width modulation has to be added as shown in Fig. 13.10 and 13.11 of Chapter XIII. Here the frequency chosen for the variable frequency 50% duty-cycle three phase clock generator is 10 kHz. The design procedure is the same as that for a conventional three phase two level inverter. Therefor for the purpose of clarity, the bidirectional switches in Fig. 13.11 of Chapter XIII is replaced by conventional switches in a three phase two level inverter. The design is illustrated below:

The three phase inverter using conventional switches is shown in Fig. AI.4 and the gate drive waveform is shown in Fig. AI.5. Table AI.1 shows the method of connecting the port B of the micro-




```
;The PIC16F84A source code is given below to generate clock pulse with 494
;microseconds ON time and 6 microseconds OFF time.
;Narayanaswamy. P.R. Iyer
#include pic16F84A.inc
;port A RA4 input port
;RA4/TOCKI pin 4 MHz clock
;port B NOT used
;port A RA3-RA0 are output ports
status  equ  03
porta  equ  05
trisa  equ  85
intcon  equ  0B
option_reg  equ  81
tmr0  equ  01
org  00
bsf  status, 5  ;select bank 1
movlw  B'00010000'
movwf  trisa  ;RA4 is input and RA3-RA0 are output ports
movlw  B'00110010'
movwf  option_reg  ;TMR0 external clock input and divide by eight prescale
bcf  status, 5  ;select bank 0
bsf  intcon, 7  ;Enable global interrupt
bsf  intcon, 5  ; Enable timer0 overflow interrupt
;introduce delay of 494 microseconds
dealy494  bcf  intcon,2  ;clear TMR0 interrupt flag
movlw  B'00011111'
movwf  porta  ;porta RA0 is HIGH for 494e-6 seconds
movlw  D'9'
movwf  tmr0  ; Load decimal 9 to TMR0 to start counting 494 e-6 seconds
loop1  btfss  intcon, 2
goto  loop1
bcf  intcon, 2
movlw  B'00000000'
movwf  porta;port a RA0 is LOW  for 6e-6 seconds
movlw  D'253'
movwf  tmr0
loop2  btfss  intcon, 2
goto  loop2
goto  delay494
end
```

FIG. AI.2: FLOW-CHART AND SOURCE CODE FOR SAW-TOOTH WAVEFORM GENERATOR

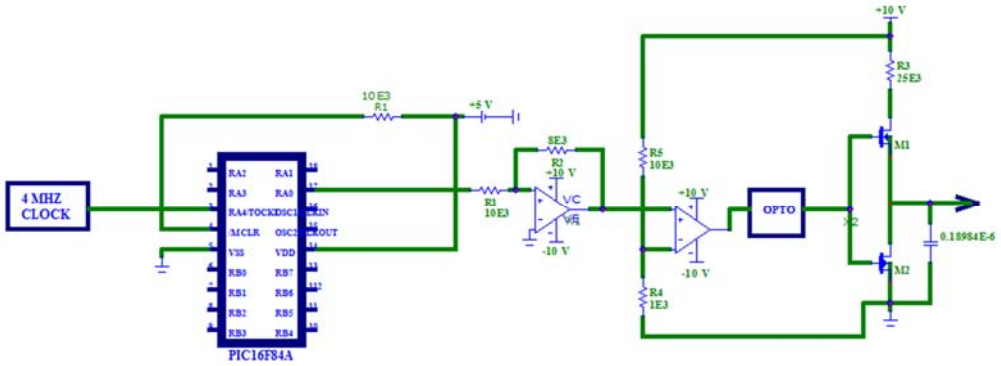


FIG. AI.3 A 2 kHZ SAW-TOOTH CARIER WAVEFORM GENERATOR USING PIC16F84A

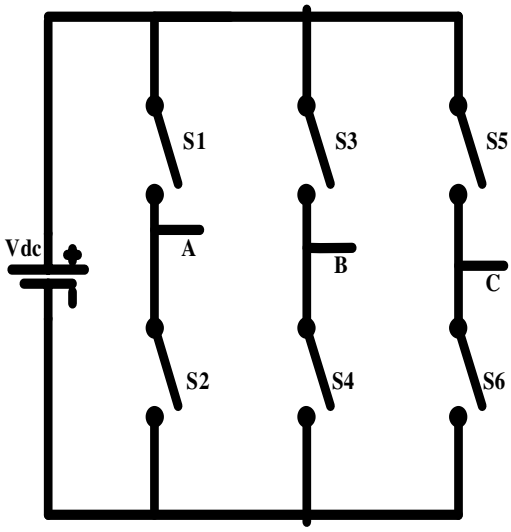


FIG. AI.4: Three Phase Inverter

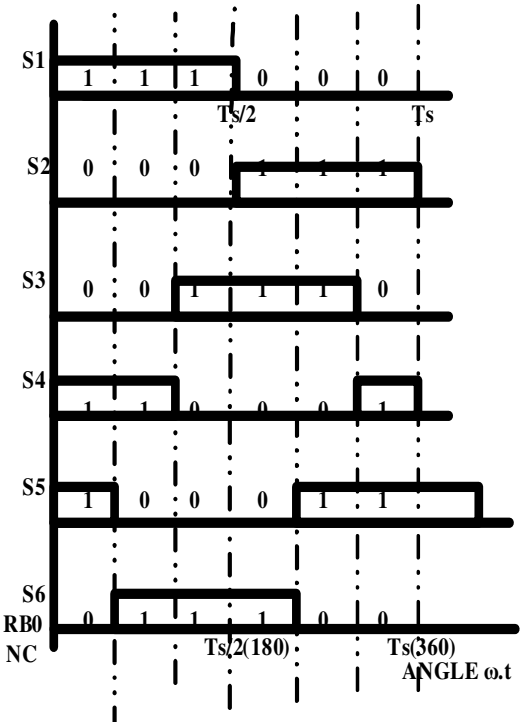


FIG. AI.5: Three Phase Inverter Gate Drive Waveform

TABLE AI.1

PORT B:	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
SWITCH:	S1	S2	S3	S4	S5	S6	NC	NC

TABLE AI.2 BIT PATTERN

ANGLE:	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
0 – 60	1	0	0	1	1	0	0	0
60 – 120	1	0	0	1	0	1	0	0
120 – 180	1	0	1	0	0	1	0	0
180 – 240	0	1	1	0	0	1	0	0
240 – 300	0	1	1	0	1	0	0	0
300 – 360	0	1	0	1	1	0	0	0

controller to the three phase inverter gate drive. Table AI.2 shows the bit pattern obtained from Fig. AI.5. Here an output frequency of 10 kHz is assumed. Therefor period of the inverter output frequency is 100e-6 seconds and 60 degree time interval correspond to 16.6667e-6 seconds. Assume that the external clock connected to RA4/TOCKI pin of PIC16F84A has a frequency of 4 MHz and that a prescale of divide by two is used. The TMR0 register is used to create a time delay of 16.6667e-6 seconds. The TMR0 count preset is calculated below:

$$Clock \quad Frequency = \quad 2MHz$$

$$Clock \quad Period = \quad \frac{1}{2 * 10^{6}} = \quad 0.5 * 10^{-6} \ seconds \qquad (AI.7)$$

$$0.5 * 10^{-6} * N1 \, clock \quad cycle = \quad 16.6667 * 10^{-6}$$

$$N1 = \quad 33$$

$$Preset \ \ TMR0 \quad for \, 16.6667e-6 \ seconds \quad time \ \ delay \quad = (256 - 33) = \quad 223 \qquad (AI.8)$$

The source code for generating the 10 kHz three phase inverter gate drive is shown in Fig. AI.6. By varying the TMR0 count preset, any required output frequency for the three phase inverter can be obtained. The 10 kHz three phase inverter gate drive using PIC16F84A is shown in Fig. AI.7. The gate drive for switches S1 to S6 in Fig. AI.7 correspond to the gate drive for the bidirectional IGBT switches from top to bottom in order shown in Fig. 13.11 in Chapter XIII.

```
;The PIC16F84A source code is given below for 10 kHz three phase inverter
;Narayanaswamy. P.R. Iyer
#include pic16F84A.inc
;port A RA4 input port
;RA4/TOCKI pin 4 MHz clock
;port B output port
;port A RA3-RA0 are output ports
status  equ  03
porta  equ  05
portb  equ  06
trisa  equ  85
trisb  equ  86
intcon  equ  0B
option_reg  equ  81
tmr0  equ  01
org  00
bsf  status, 5  ;select bank 1
movlw  B'00010000'
movwf  trisa  ;RA4 is input and RA3-RA0 are output ports
movlw  B'00000000'
movwf  trisb  ;All port B pins are output ports
movlw  B'00110000'
movwf  option_reg  ;TMR0 external clock input at RA4/TOCKI and divide by two prescale
bcf  status, 5  ;select bank 0
bsf  intcon, 7  ;Enable global interrupt
bsf  intcon, 5  ;Enable TMR0 overflow interrupt
loop1  movlw  H'98'
movwf  portb
call  delay
movlw  H'94'
movwf  portb
call  delay
movlw  H'A4'
movwf  portb
call  delay
movlw  H'64'
movwf  portb
call  delay
movlw  H'68'
movwf  portb
call  delay
movlw  H'58'
movwf  portb
call  delay
goto  loop1
delay  bcf  intcon,2  ;clear TMR0IF
movlw  D'223'
movwf  tmr0  ;load TMR0 for a dealy of 16.6667e-6 seconds
loop2  btfss  intcon,2
goto  loop2
return
end
```

FIG. AI.6: SOURCE CODE FOR THREE PHASE AC TO AC CONVERTER USING A DC LINK

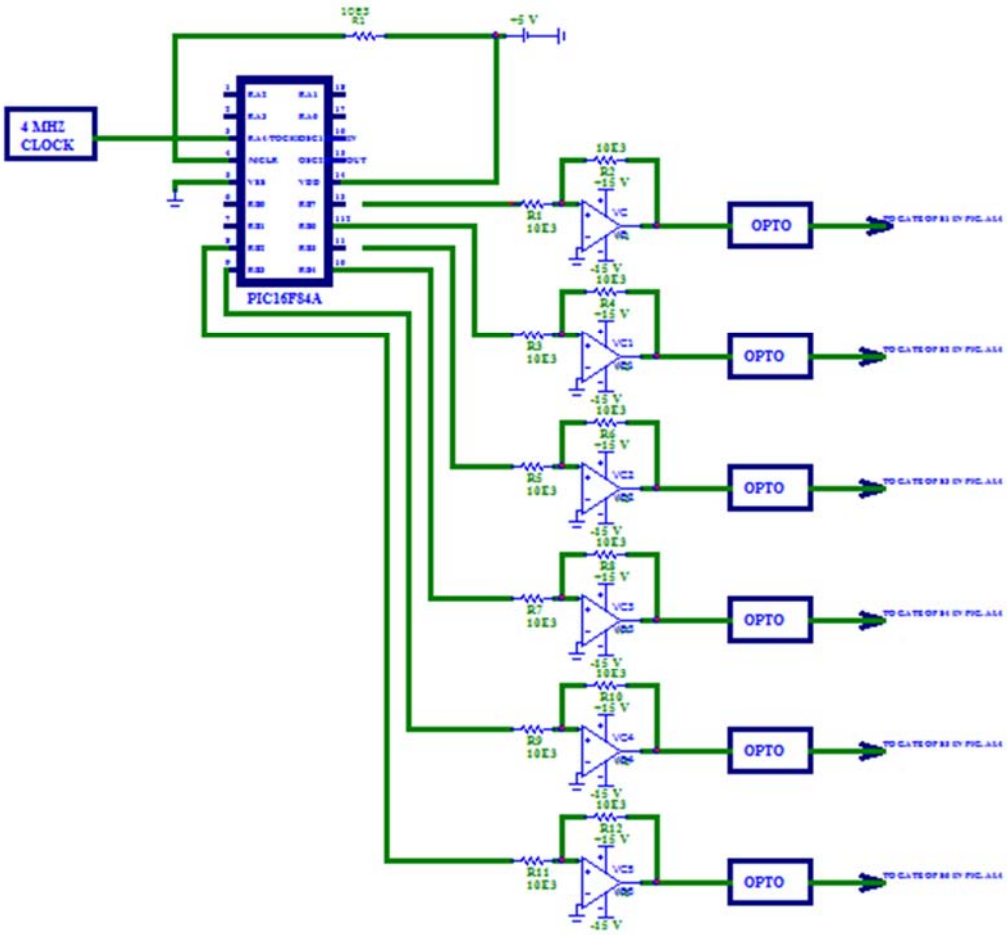


FIG. AI.7 THREE PHASE 10 kHZ INVERTER GATE DRIVE

AI.5 CONCLUSIONS: The present trend is to use microcontrollers in the place of analog and digital ICs for waveform generation and for three phase and single phase inverter gate drive. By assigning suitable value for TMR0 count preset value required time delay and required output frequency can be obtained. Also externally changing the clock frequency within the range allowable for PIC16F84A, required output frequency for the inverter and also for the square pulse waveform ON and OFF time can be obtained. Also by using any neighbouring output gate drive such as the gate drive for S1 and S2 in Fig. AI.7, the same source code and circuit connection in Fig. AI.7 can be used for single phase AC to single phase AC converter using a DC link discussed in Chapter XIII.

AI.6 REFERENCES:

[1] PIC16F84A Data Sheet, MICROCHIP Technology Inc., USA, 2001.

Appendix II

Speed Control and Brake by Plugging of Three Phase Induction Motor Fed by Matrix Converter

AII.1 INTRODUCTION: Three phase induction motor (IM) fed by Matrix Converters (MCs) can be used for speed control and brake by plugging or by reversing the phase sequence of the three phase applied voltage. This can be accomplished in the SIMULINK MC model and can be implemented in dSPACE. Thus three phase IM fed by MC can be used in Hybrid Electric Vehicle and also in electric traction. This section explores this application.

AII.2 MODEL OF THREE PHASE INDUCTION MOTOR FED BY MATRIX CONVERTER: The SIMULINK model of the three phase IM fed by MC with provision for speed control and brake by plugging is shown in Fig. AII.1. Braking of a three phase IM by plugging involves reversing the phase sequence of the three phase applied voltage to the stator terminals of the IM. This is done manually using three pole double throw switch. In the method using SIMULINK model this can be done by varying the model parameter such as the modulation index and the phase of the desired three phase output voltage. The model shown in Fig. AII.1 is developed using Venturini Second method assuming unity input phase displacement factor explained in section 3.4.3 of chapter III. Only relevant changes in the model for speed control and braking is explained below:

Speed control is achieved by varying the magnitude of the three phase output voltage of the MC which is applied to the terminals of the IM. Magnitude variation is possible by changing the modulation index q in the range from 0 to 0.5. In Fig. AII.1, this value of q is varied using a multiport switch. For braking, three phase output voltage phase sequence has to be reversed. Referring to equation 3.11 of chapter III, the phase sequence of output voltage vb and vc can be changed by swapping the phase $2\pi/3$ with proper sign. In Fig. AII.1, this is achieved by using a repeating sequence block. The three phase IM used has the parameter shown in Table 5.1 of chapter V.

AII.3 SIMULATION RESULTS: The simulation of the model shown in Fig. AII.1 is carried out using SIMULINK [51]. The ode15s(Stiff/NDF) solver is used. The simulation results are shown in Fig. AII.2(A) to AII.2(D).

AII.4 REAL TIME IMPLEMENTATION: The real time implementation scheme using SIMULINK model in conjunction with dSPACE hardware controller board is shown in Fig. AII.3(A) to (C). The scheme in Fig. AII.3(A) and (B) are with DC generator and three phase alternator mode respectively. Fig. AII.3(C) is the scheme for dSPACE gate drive for MC. Fig. AII.4 shows the hard-

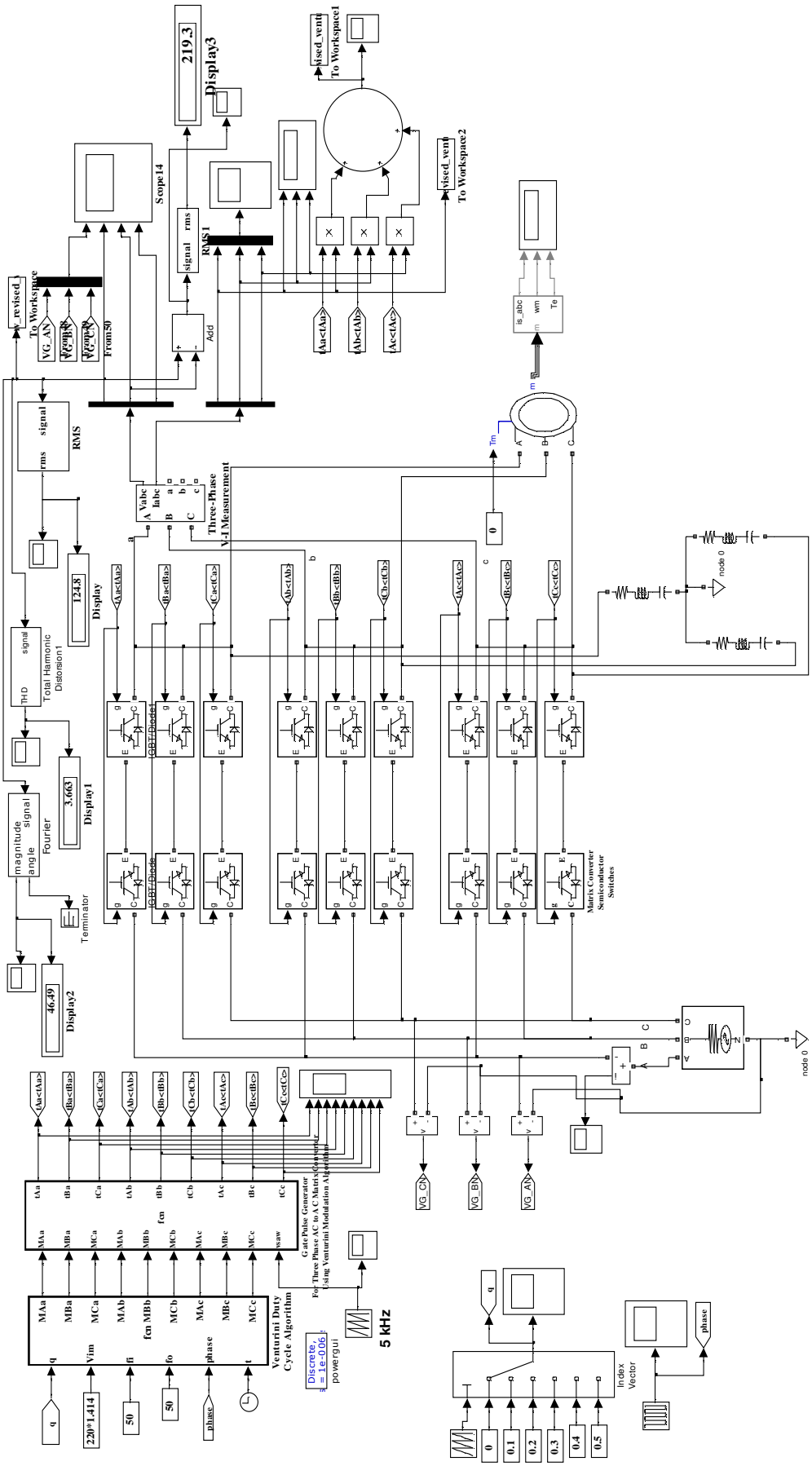
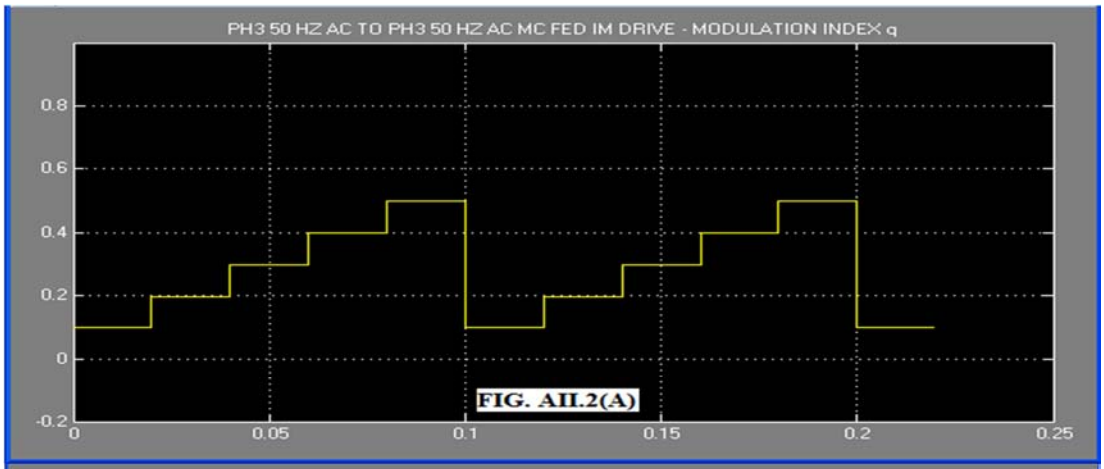
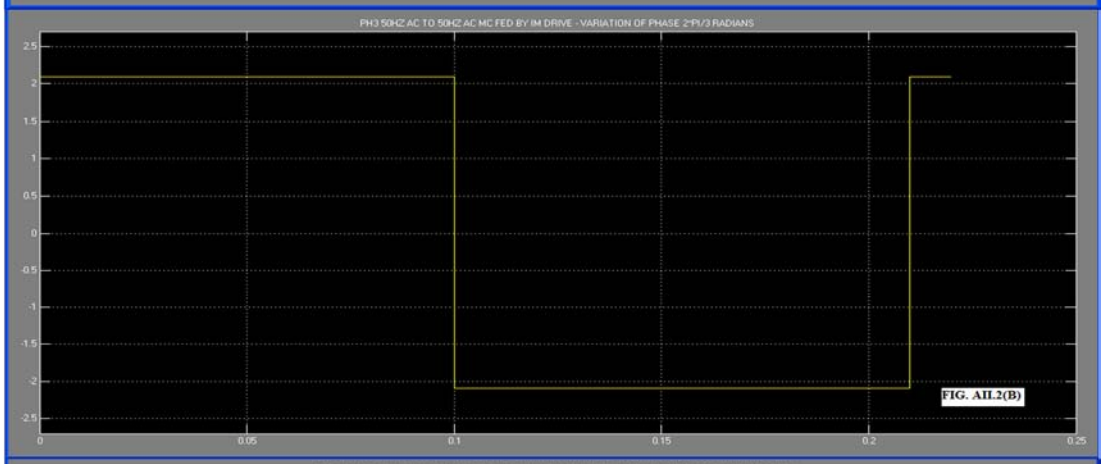
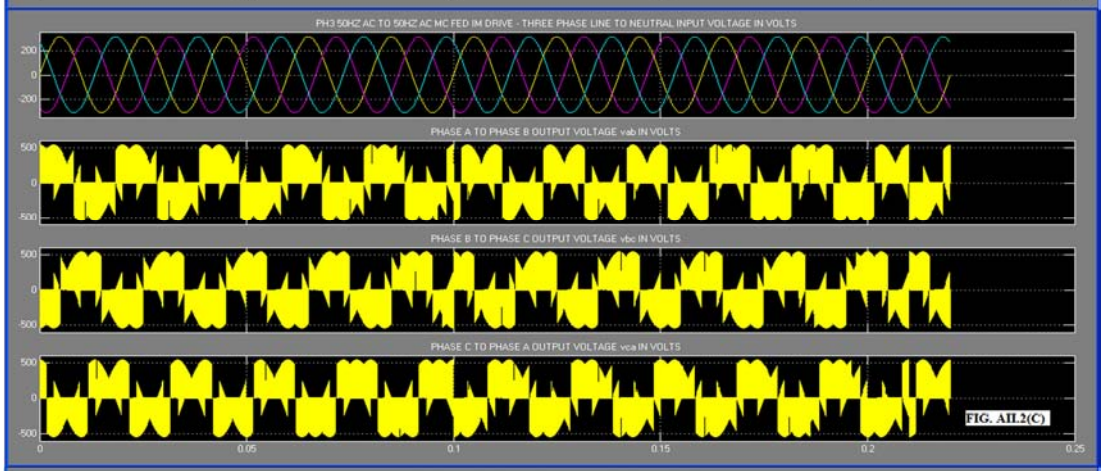
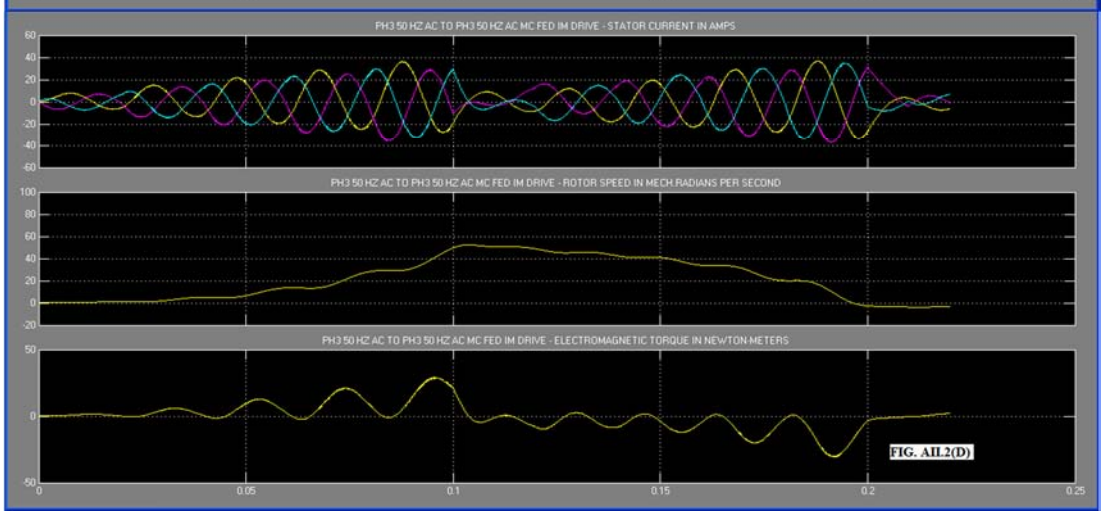


FIG. AII.1: SPEED CONTROL AND BRAKE BY PLUGGING OF THREE PHASE IM FED BY MC


PH3 50 HZ AC TO PH3 50 HZ AC MC FED IM DRIVE - MODULATION INDEX q
FIG. AII.2(A)


PH3 50HZ AC TO 50HZ AC MC FED BY IM DRIVE - VARIATION OF PHASE 2*PI/3 RADIANS
FIG. AII.2(B)


PH3 50HZ AC TO 50HZ AC MC FED IM DRIVE - THREE PHASE LINE TO NEUTRAL INPUT VOLTAGE IN VOLTS
PHASE A TO PHASE B OUTPUT VOLTAGE vab IN VOLTS
PHASE B TO PHASE C OUTPUT VOLTAGE vbc IN VOLTS
PHASE C TO PHASE A OUTPUT VOLTAGE vca IN VOLTS
FIG. AII.2(C)


PH3 50 HZ AC TO PH3 50 HZ AC MC FED IM DRIVE - STATOR CURRENT IN AMPS
PH3 50 HZ AC TO PH3 50 HZ AC MC FED IM DRIVE - ROTOR SPEED IN MECH RADIANS PER SECOND
PH3 50 HZ AC TO PH3 50 HZ AC MC FED IM DRIVE - ELECTROMAGNETIC TORQUE IN NEWTON-METERS
FIG. AII.2(D)

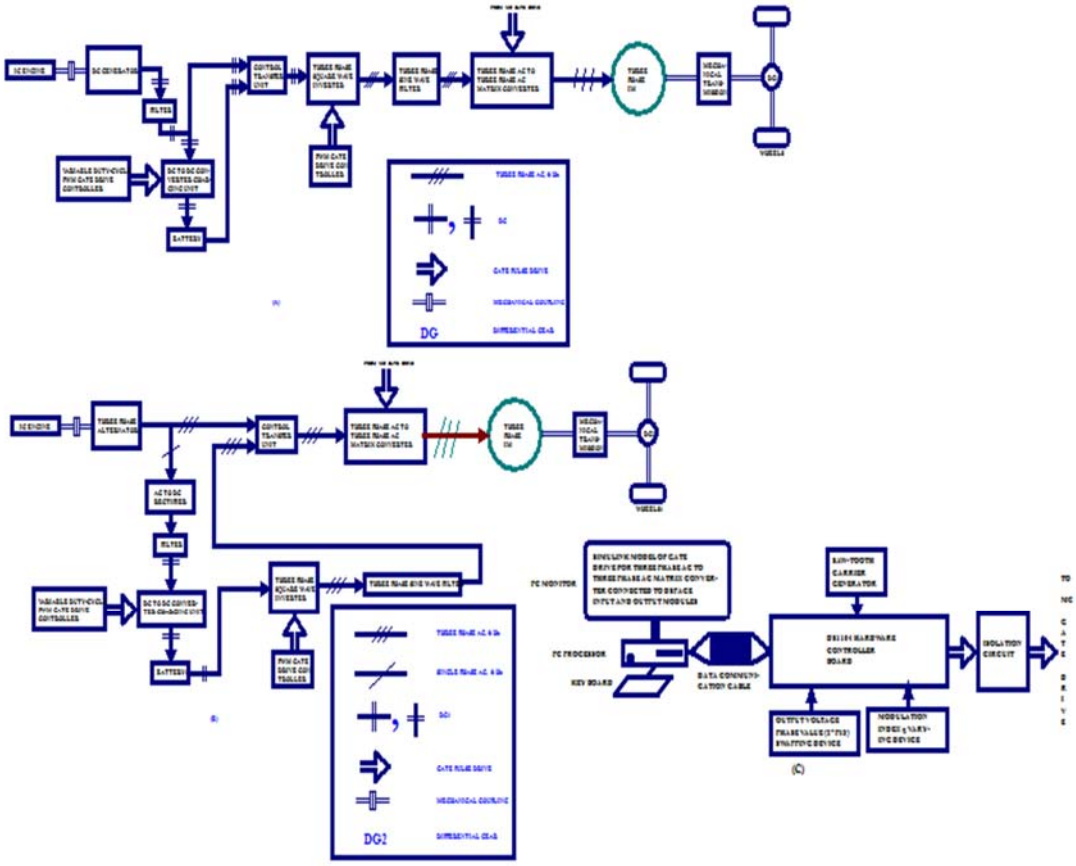


FIG. AII.3

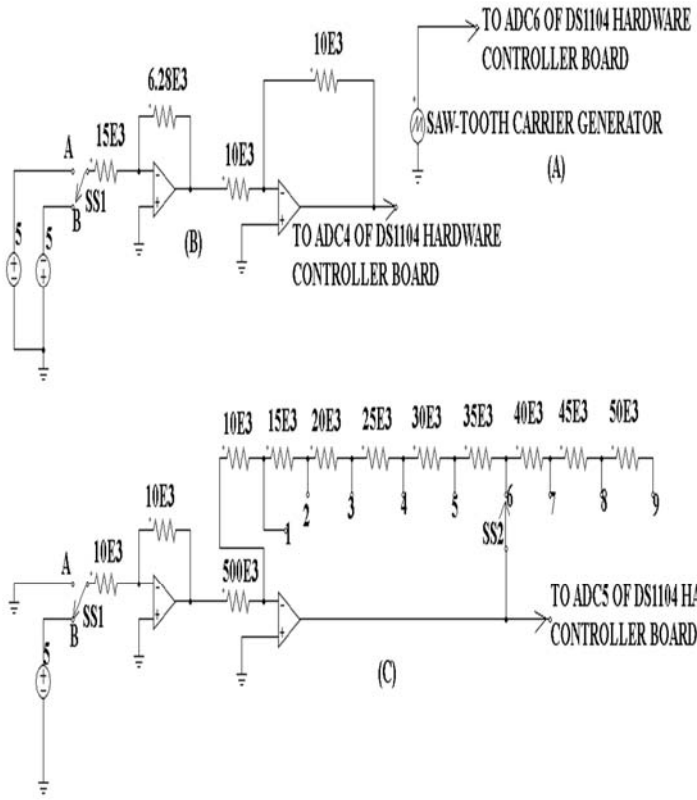


FIG. AII.4 SAW-TOOTH CARRIER GENERATOR (A), OUTPUT VOLTAGE PHASE VALUE SWAPPING DEVICE(B) AND MODULATION INDEX VARYING DEVICE(C)

ware implementation for the saw-tooth carrier generator, output voltage phase value (2*PI/3) swapping device and the modulation index varying device. The hardware realization for saw-tooth carrier generator is already explained in chapter X and also Appendix I. The phase value swapping device and the modulation index varying device use op.amps and resistor network as shown in Fig. AII.4 (B) and (C) respectively.

AII.5 DISCUSSION OF RESULTS: For the purpose of illustration of acceleration, retardation and braking by plugging or phase sequence reversal, the modulation index q is assumed to vary from 0 to 0.5 in steps of 0.1 every 20e-3 seconds in the forward increasing order and then in the reverse decreasing order. At 100e-3 seconds simulation time the phase value changes from $+2\pi/3$ to $-2\pi/3$ radians and similarly at 210e-3 seconds simulation time, this phase value changes from $-2\pi/3$ to $+2\pi/3$ radians respectively. From the rotor speed in Fig. AII.2(D) it is seen that the IM accelerates for the initial 100e-3 seconds, then retards or decelerates and reverses direction of rotation from 100e-3 seconds to 210e-3 seconds. From the stator current and line to line output voltage waveform in Fig. AII.2(D), it is clear that phase sequence reverasal takes place after 100e-3 seconds simulation time. Also in Fig. AII.2(D), the rotor E.M. torque is found to be negative from 100e-3 seconds simulation time. This simulation illustrates the speed control, acceleration, retardation and braking of three phase IM. Fig. AII.3 and AII.4 shows how this method can be implemented in real time using dSPACE DS1104 hardware controller board. The three phase IM fed by three phase AC to three phase AC MC can be used for Hybrid Electric Vehicle (HEV) [63] and Electric Traction applications.

AII.6 CONCLUSIONS: Here one method of speed control and brake by plugging of a three phase IM is illustrated by simulation of the SIMULINK model, by varying the modulation index and by swapping the phase value of the three phase output voltage in the model. A hardware realization scheme for real time application using dSAPCE DS1104 hardware controller board is also presented. This provides a new method of real time speed control and brake by plugging of three phase IM drive suitable for Hybrid Electric Vehicle and electric traction applications.

Appendix II

Speed Control and Brake by Plugging of Three Phase Induction Motor Fed by Matrix Converter

AII.1 INTRODUCTION: Three phase induction motor (IM) fed by Matrix Converters (MCs) can be used for speed control and brake by plugging or by reversing the phase sequence of the three phase applied voltage. This can be accomplished in the SIMULINK MC model and can be implemented in dSPACE. Thus three phase IM fed by MC can be used in Hybrid Electric Vehicle and also in electric traction. This section explores this application.

AII.2 MODEL OF THREE PHASE INDUCTION MOTOR FED BY MATRIX CONVERTER: The SIMULINK model of the three phase IM fed by MC with provision for speed control and brake by plugging is shown in Fig. AII.1. Braking of a three phase IM by plugging involves reversing the phase sequence of the three phase applied voltage to the stator terminals of the IM. This is done manually using three pole double throw switch. In the method using SIMULINK model this can be done by varying the model parameter such as the modulation index and the phase of the desired three phase output voltage. The model shown in Fig. AII.1 is developed using Venturini Second method assuming unity input phase displacement factor explained in Section 3.4.3 of Chapter III. Only relevant changes in the model for speed control and braking is explained below:

Speed control is achieved by varying the magnitude of the three phase output voltage of the MC which is applied to the terminals of the IM. Magnitude variation is possible by changing the modulation index q in the range from 0 to 0.5. In Fig. AII.1, this value of q is varied using a multiport switch. For braking, three phase output voltage phase sequence has to be reversed. Referring to equation 3.11 of Chapter III, the phase sequence of output voltage vb and vc can be changed by swapping the phase $2\pi/3$ with proper sign. In Fig. AII.1, this is achieved by using a repeating sequence block. The three phase IM used has the parameter shown in Table 5.1 of Chapter V.

AII.3 SIMULATION RESULTS: The simulation of the model shown in Fig. AII.1 is carried out using SIMULINK [51]. The ode15s(Stiff/NDF) solver is used. The simulation results are shown in Fig. AII.2(A) to AII.2(D).

AII.4 REAL TIME IMPLEMENTATION: The real time implementation scheme using SIMULINK model in conjunction with dSPACE hardware controller board is shown in Fig. AII.3(A) to (C). The scheme in Fig. AII.3(A) and (B) are with DC generator and three phase alternator mode respectively. Fig. AII.3(C) is the scheme for dSPACE gate drive for MC. Fig. AII.4 shows the hard-

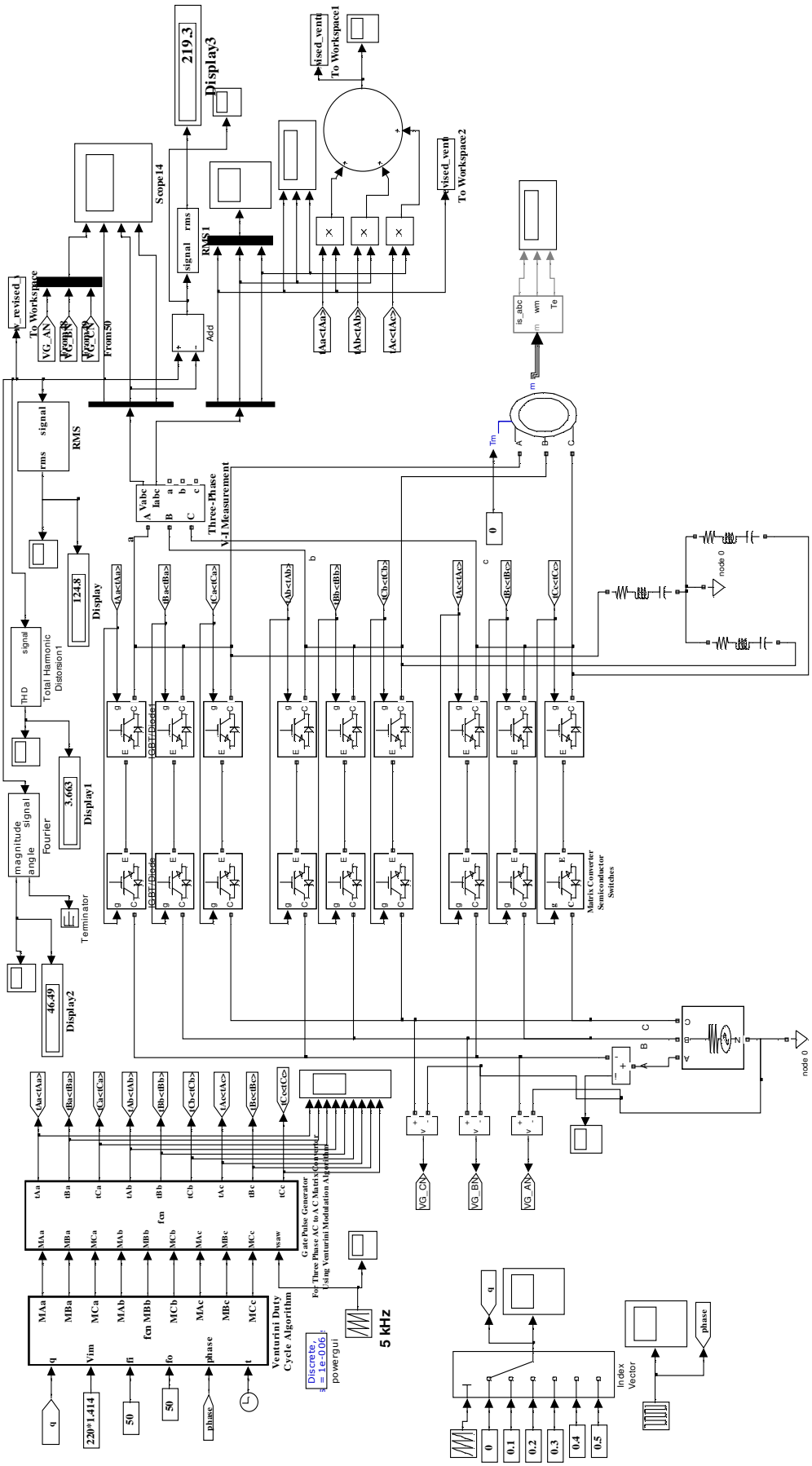
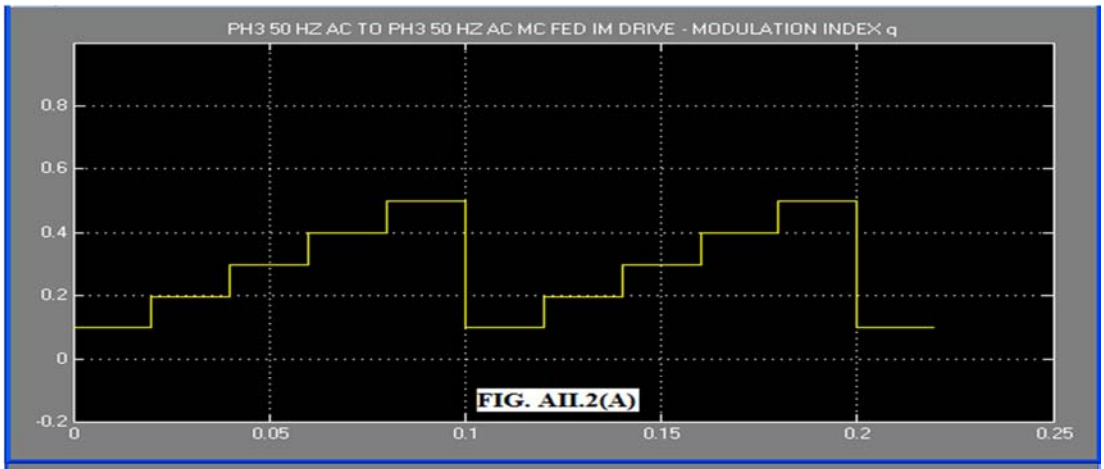
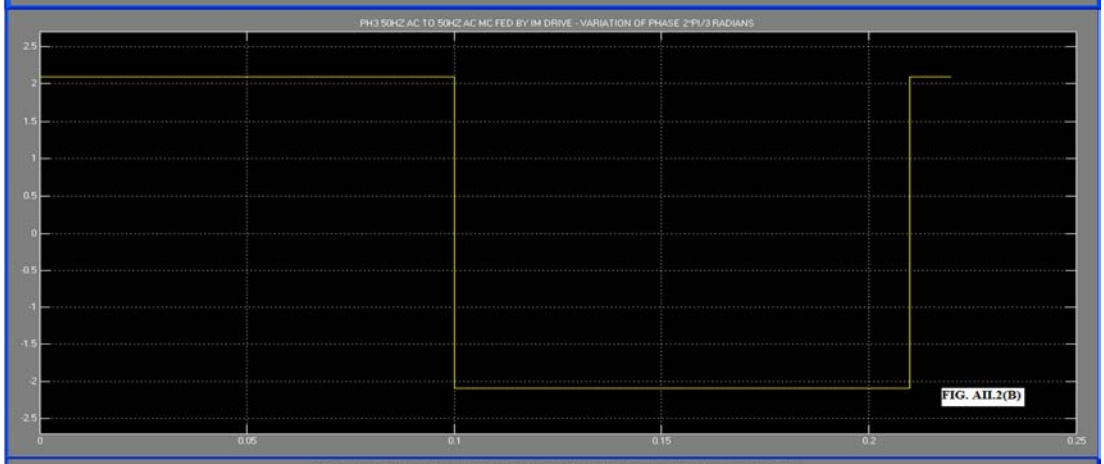
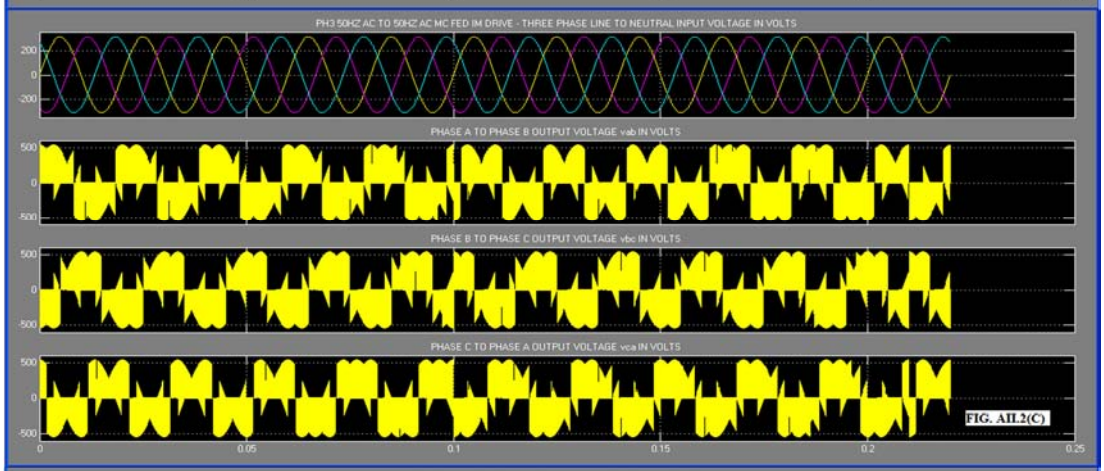
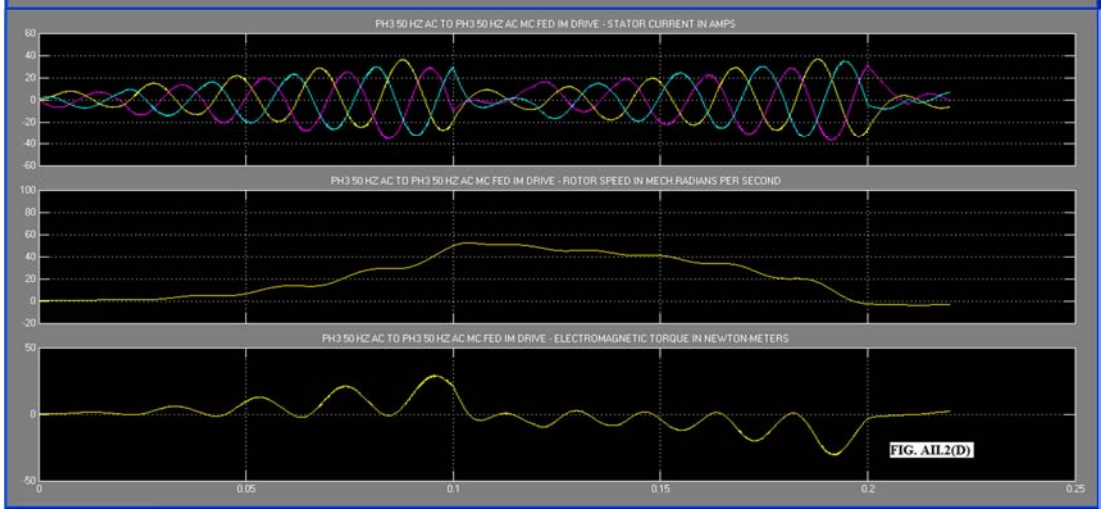


FIG. AII.1: SPEED CONTROL AND BRAKE BY PLUGGING OF THREE PHASE IM FED BY MC


PH3 50 HZ AC TO PH3 50 HZ AC MC FED IM DRIVE - MODULATION INDEX q
0.8
0.6
0.4
0.2
0
-0.2
0
0.05
0.1
0.15
0.2
0.25
FIG. AII.2(A)


PH3 50HZ AC TO 50HZ AC MC FED BY IM DRIVE - VARIATION OF PHASE 2*PI/3 RADIANS
FIG. AII.2(B)


PH3 50HZ AC TO 50HZ AC MC FED IM DRIVE - THREE PHASE LINE TO NEUTRAL INPUT VOLTAGE IN VOLTS
PHASE A TO PHASE B OUTPUT VOLTAGE vab IN VOLTS
PHASE B TO PHASE C OUTPUT VOLTAGE vbc IN VOLTS
PHASE C TO PHASE A OUTPUT VOLTAGE vca IN VOLTS
FIG. AII.2(C)


PH3 50 HZ AC TO PH3 50 HZ AC MC FED IM DRIVE - STATOR CURRENT IN AMPS
PH3 50 HZ AC TO PH3 50 HZ AC MC FED IM DRIVE - ROTOR SPEED IN MECH RADIANS PER SECOND
PH3 50 HZ AC TO PH3 50 HZ AC MC FED IM DRIVE - ELECTROMAGNETIC TORQUE IN NEWTON-METERS
FIG. AII.2(D)

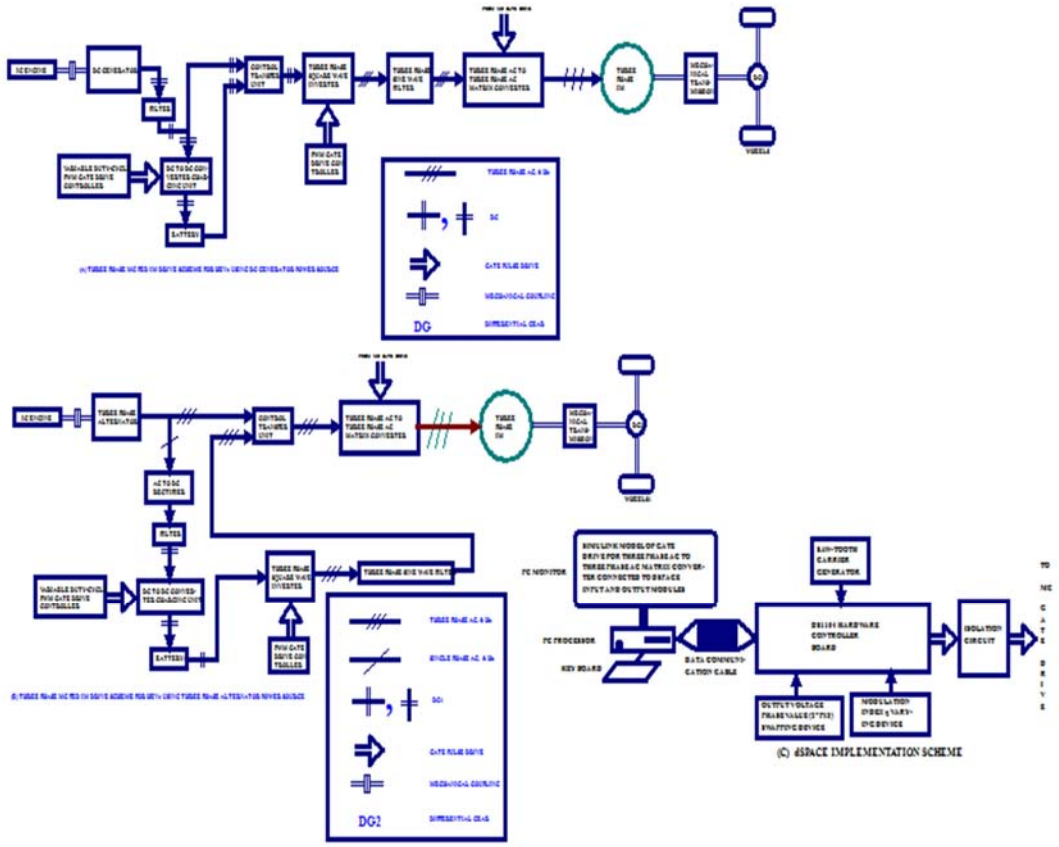


FIG. AII.3: THREE PHASE MC FED IM DRIVE FOR HEVs

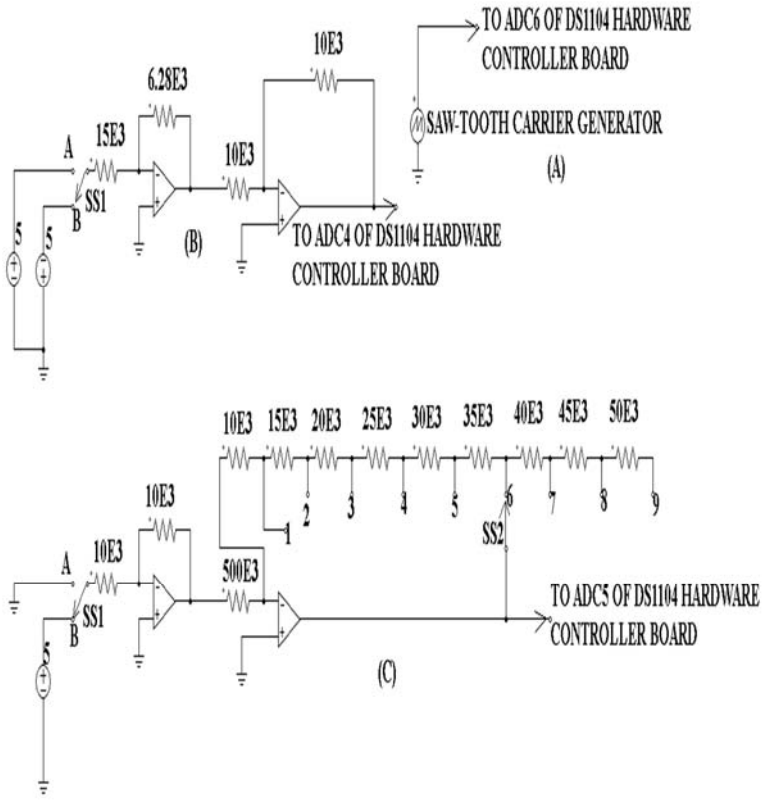


FIG. AII.4 SAW-TOOTH CARRIER GENERATOR (A), OUTPUT VOLTAGE PHASE VALUE SWAPPING DEVICE(B) AND MODULATION INDEX VARYING DEVICE(C)

ware implementation for the saw-tooth carrier generator, output voltage phase value (2*PI/3) swapping device and the modulation index varying device. The hardware realization for saw-tooth carrier generator is already explained in Chapter X and also in Appendix I. The phase value swapping device and the modulation index varying device use op.amps and resistor network as shown in Fig. AII.4 (B) and (C) respectively.

AII.5 DISCUSSION OF RESULTS: For the purpose of illustration of acceleration, retardation and braking by plugging or phase sequence reversal, the modulation index q is assumed to vary from 0 to 0.5 in steps of 0.1 every 20e-3 seconds in the forward increasing order and then in the reverse decreasing order. At 100e-3 seconds simulation time the phase value changes from $+2\pi/3$ to $-2\pi/3$ radians and similarly at 210e-3 seconds simulation time, this phase value changes from $-2\pi/3$ to $+2\pi/3$ radians respectively. From the rotor speed in Fig. AII.2(D) it is seen that the IM accelerates for the initial 100e-3 seconds, then retards or decelerates and reverses direction of rotation from 100e-3 seconds to 210e-3 seconds. From the stator current and line to line output voltage waveform in Fig. AII.2(D), it is clear that phase sequence reverasal takes place after 100e-3 seconds simulation time. Also in Fig. AII.2(D), the rotor E.M. torque is found to be negative from 100e-3 seconds simulation time. This simulation illustrates the speed control, acceleration, retardation and braking of three phase IM. Fig. AII.3 and AII.4 shows how this method can be implemented in real time using dSPACE DS1104 hardware controller board. The three phase IM fed by three phase AC to three phase AC MC can be used for Hybrid Electric Vehicle (HEV) [63] and Electric Traction applications.

AII.6 CONCLUSIONS: Here one method of speed control and brake by plugging of a three phase IM is illustrated by simulation of the SIMULINK model, by varying the modulation index and by swapping the phase value of the three phase output voltage in the model. A hardware realization scheme for real time application using dSAPCE DS1104 hardware controller board is also presented. This provides a new method of real time speed control and brake by plugging of three phase IM drive suitable for Hybrid Electric Vehicle and electric traction applications.

Appendix III
List of Publications

AIII.1 INTRODUCTION: The following are the list of publications from this research work:

AIII.2 LIST OF PUBLICATIONS:

[1] Narayanaswamy. P.R. Iyer: "Carrier Based Modulation Technique for Three Phase Matrix Converters"; Research Seminar, School of Electrical and Information Engineering, The University of Sydney, NSW-2006, Australia, 2 July 2010.

[2] Narayanaswamy. P.R. Iyer: "Carrier Based Modulation Technique for Three Phase Matrix Converters – State of the Art Progress"; IEEE Region 8 SIBIRCON-2010, Irkutsk Listvyanka, Russia, July 11 — 15, 2010; pp. 659 – 664.

[3] Narayanaswamy. P.R. Iyer: "Performance Comparison of a Three Phase Multilevel Matrix Converter with Three Flying Capacitors per output phase with a Three Phase Conventional Matrix Converter"; Research Seminar; Department of Electrical and Computer Engineering; Curtin University of Technology, Perth, WA, Australia; 24th May 2011.

[4] Narayanaswamy. P.R. Iyer and Chem V. Nayar: "Performance Comparison of a Three Phase Multilevel Matrix Converter with Three Flying Capacitors per Output Phase with a Three Phase Conventional Matrix Converter"; Manuscript ID: PEL-2011-0372; Journal of IET Power Electronics; United Kingdom; 03-Oct-2011.

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[3] A. Alesina and M. Venturini: "Analysis and Design of Optimum Amplitude Nine-Switch Direct AC-AC Converters", IEEE Transactions on Power Electronics, Vol.4, January 1989, pp. 101 – 112.

[4] Patrick Wheeler, Jose Rodriguez, J.C. Clare, Lee Empringham and A. Weinstein: "Matrix Converters – A Technology Review", IEEE Transactions on Industrial Electronics, Vol. 49, No.2, April 2002, pp. 276 – 288.

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